












	--	C:\Documents and Settings\Administrator\My Documents\SAM2002contest\L			
	--	C:\Documents and Settings\Administrator\My Documents\SAM2002contest\L			
—	Test MSCs		3		
	Demo_TestCaseA		4	rw	Demo_TestCaseA.msc
	Demo_TestCaseC		6	rw	Demo_TestCaseC.msc
	Demo_TestCaseE		12	rw	Demo_TestCaseE.msc
	Demo_TestCaseF_Strategy3		18	rw	Demo_TestCaseF_Strategy3.msc
	CompleteMSC_TestCaseA		24	rw	CompleteMSC_TestCaseA.msc
	CompleteMSC_TestCaseC		51	rw	CompleteMSC_TestCaseC.msc
	CompleteMSC_TestCaseD_Strategy2		75	rw	CompleteMSC_TestCaseD_Strategy2.msc
	CompleteMSC_TestCaseD_Strategy3		132	rw	CompleteMSC_TestCaseD_Strategy3.msc
	CompleteMSC_TestCaseD_Strategy4		198	rw	CompleteMSC_TestCaseD_Strategy4.msc
	CompleteMSC_TestCaseE		270	rw	CompleteMSC_TestCaseE.msc
	CompleteMSC_TestCaseF_Strategy3		306	rw	CompleteMSC_TestCaseF_Strategy3.msc
	CompleteMSC_TestCaseF_Strategy4		342	rw	CompleteMSC_TestCaseF_Strategy4.msc

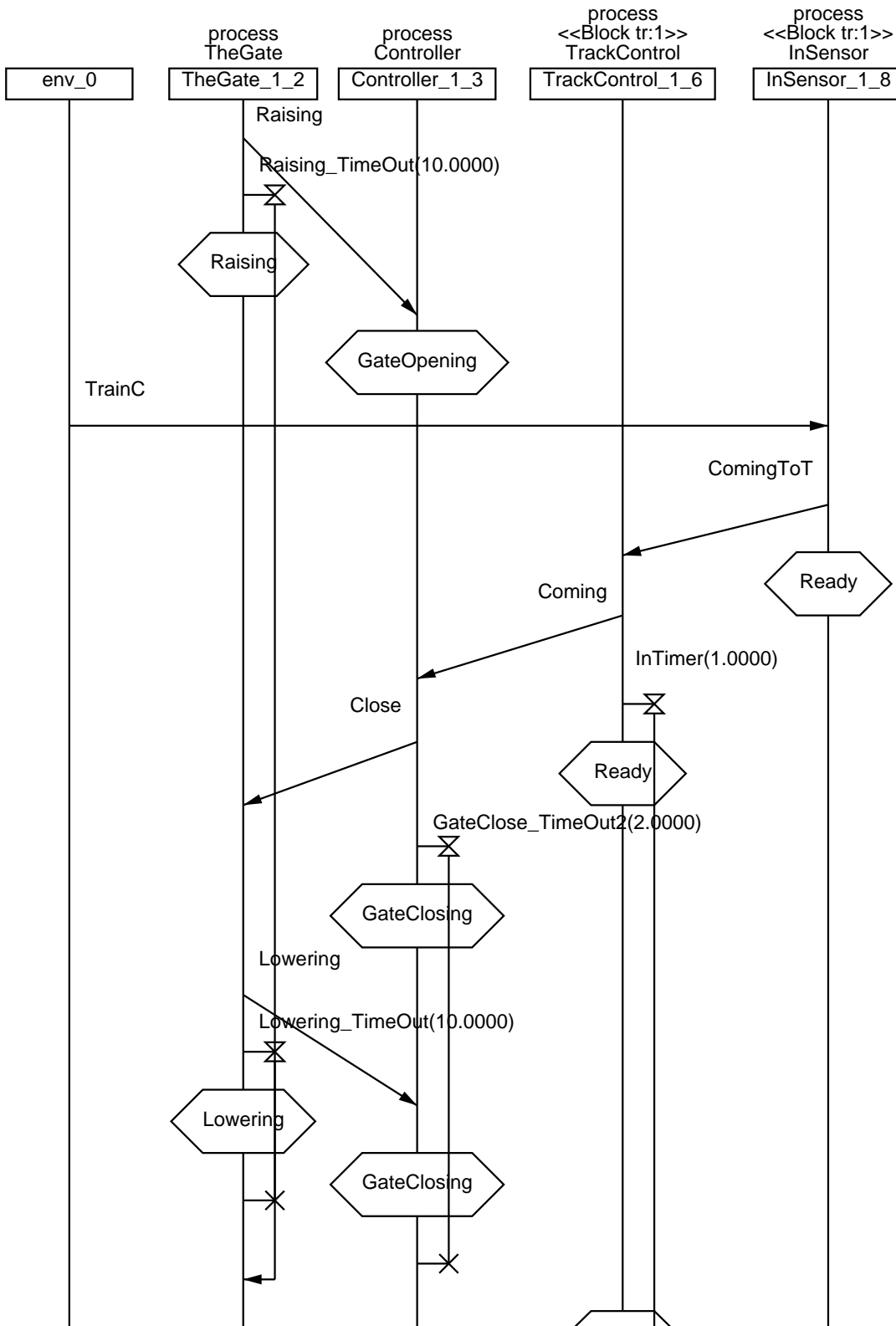
i_probert_williams\testcases.sdt

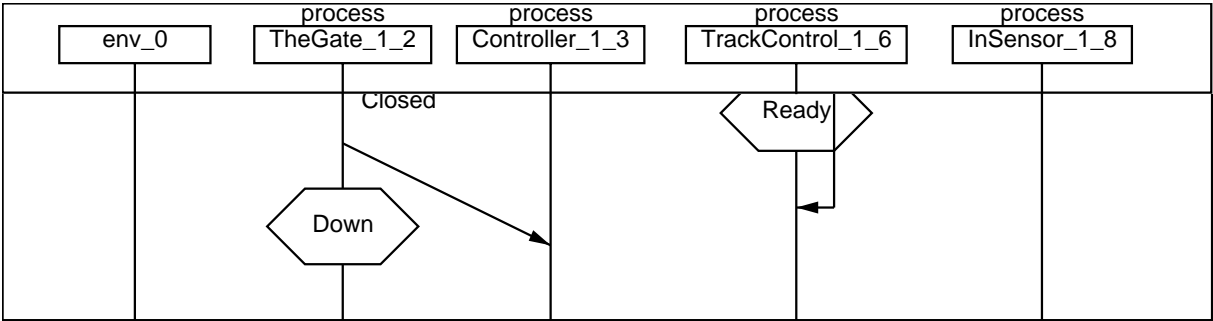
i_probert_williams

Chapter Test MSCs

MSC Demo_TestCaseA

Simplified MSC from Simulation trace generated by SDL Simulator 4.3

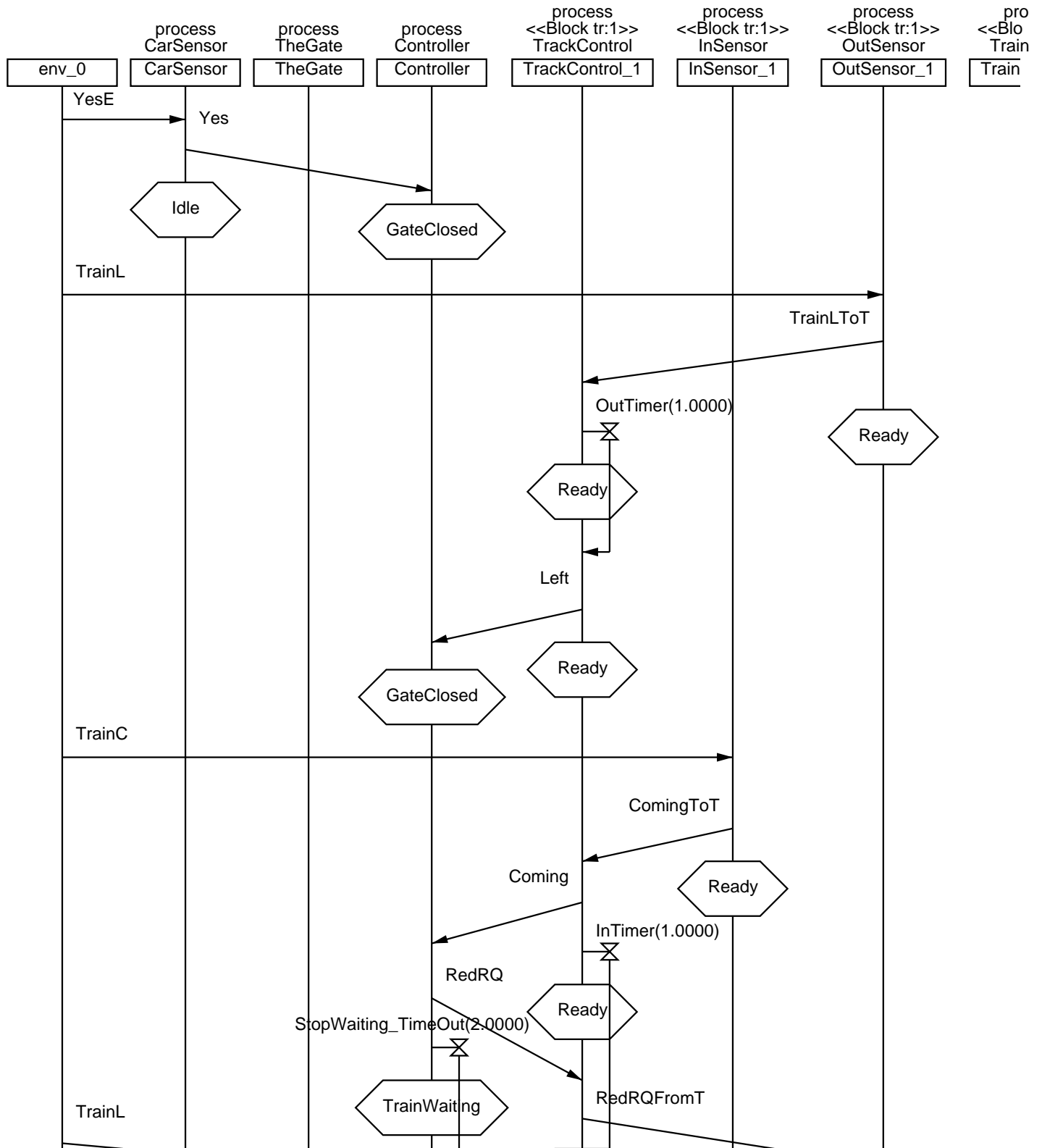


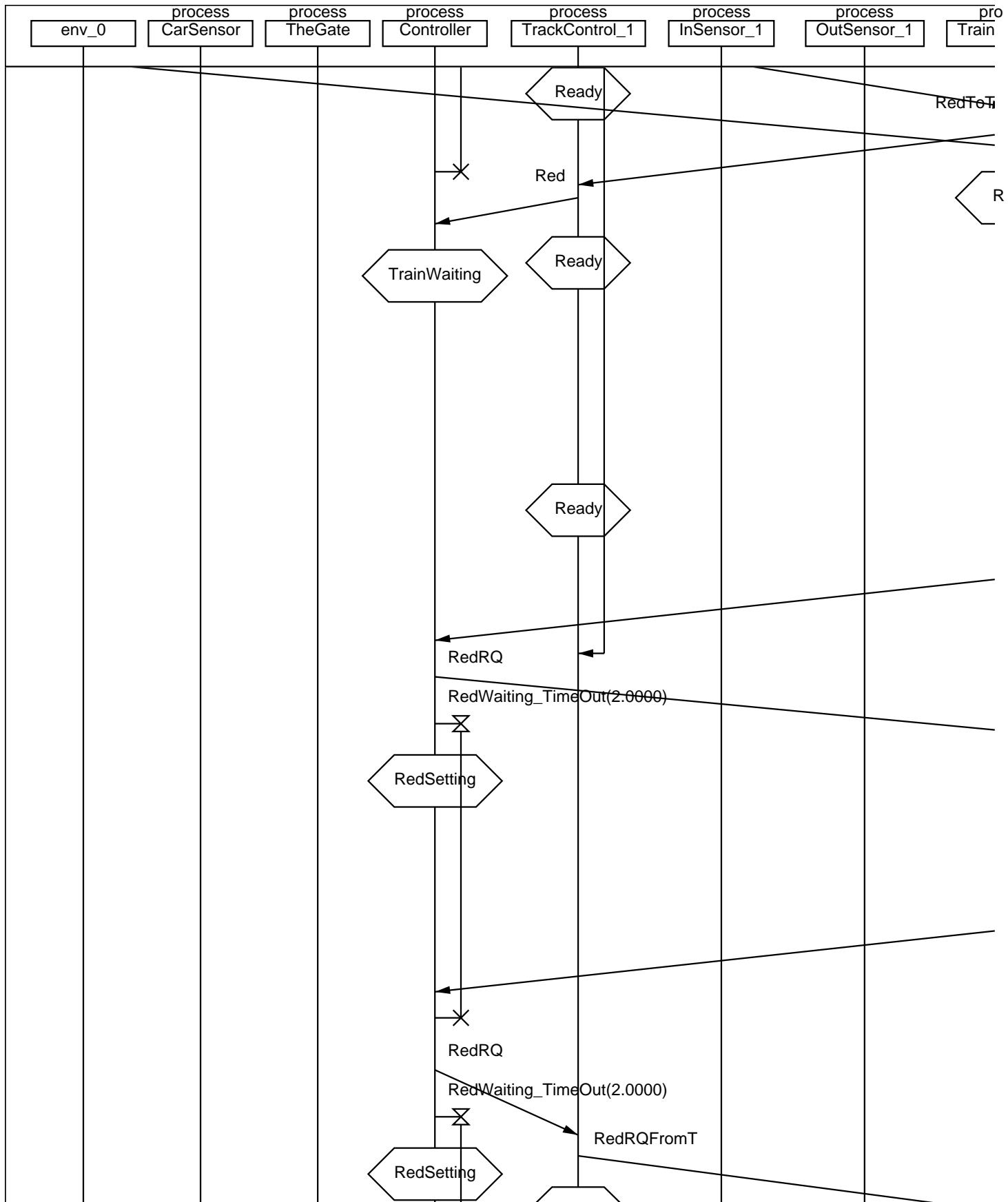


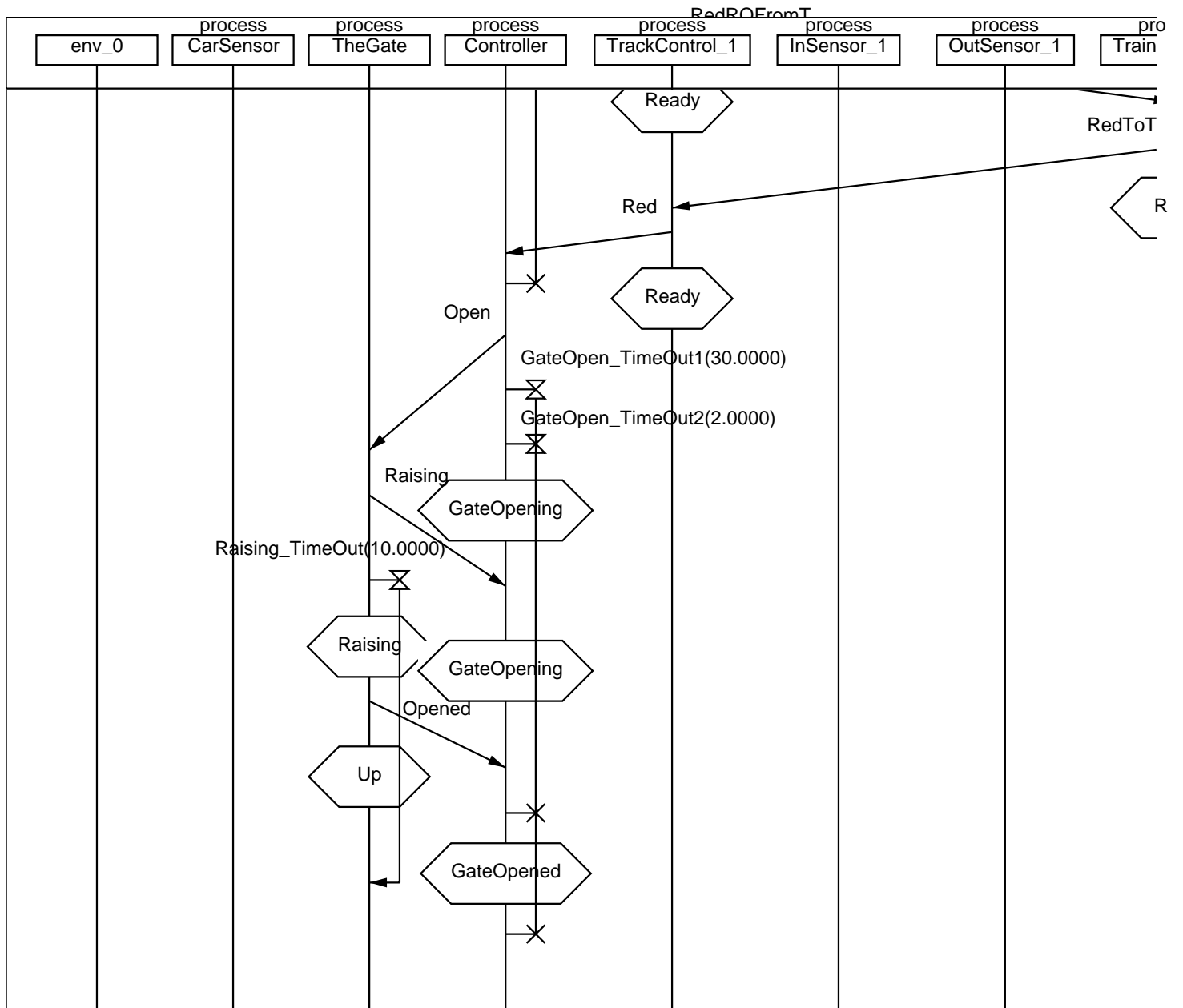
MSC Demo_TestCaseC

Simplified MSC from Simulation trace generated by SDL Simulator 4.3

Track Layout:
There are two tracks:
Track 1 is a fast track, and tTrack 2 is a s







low track

Preamble:
There is one train on each track

process
ck tr:1>>
Signal

Signal_1

process
<<Block tr:2>>
TrackControl

TrackControl_2

process
<<Block tr:2>>
InSensor

InSensor_2

process
<<Block tr:2>>
OutSensor

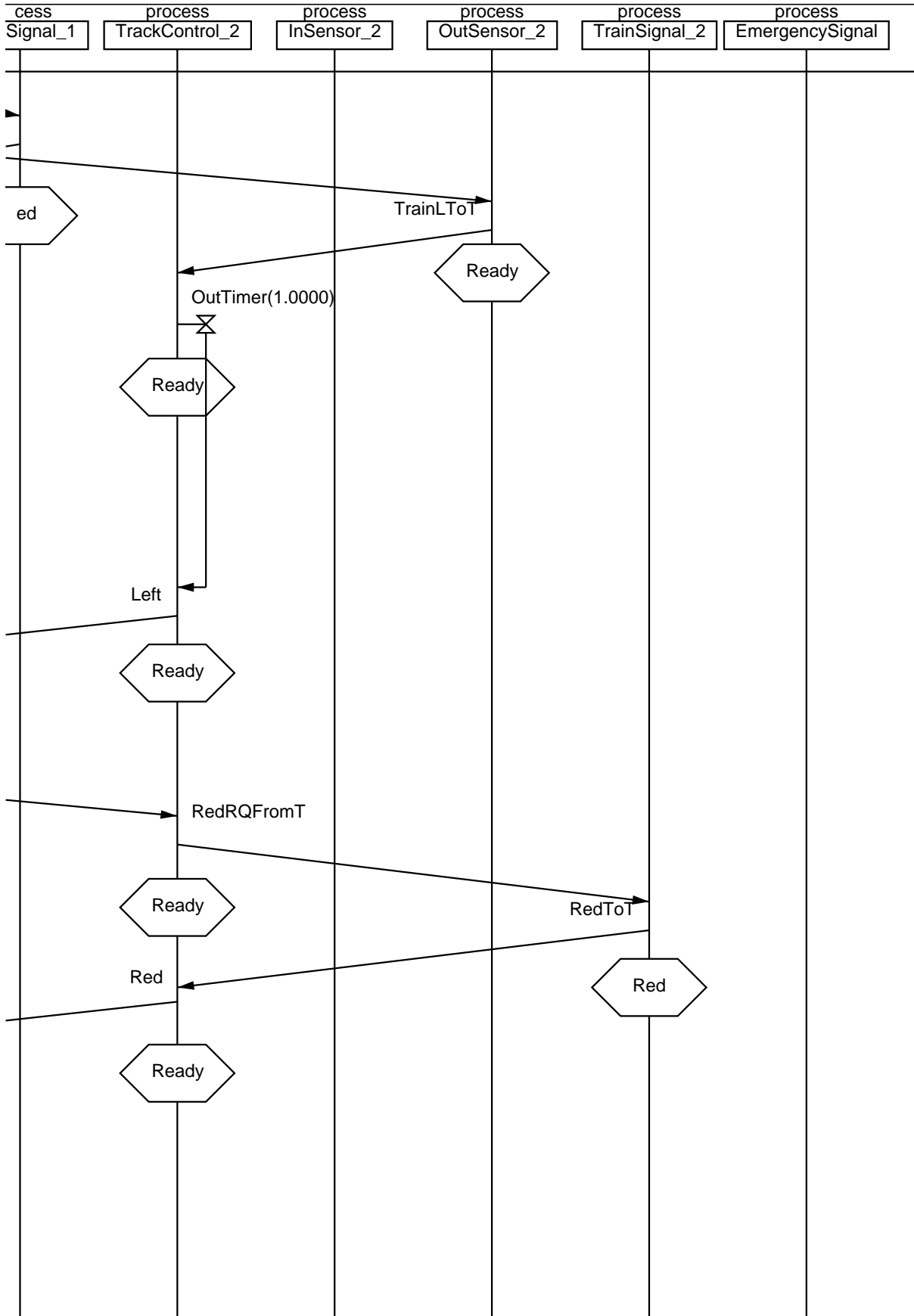
OutSensor_2

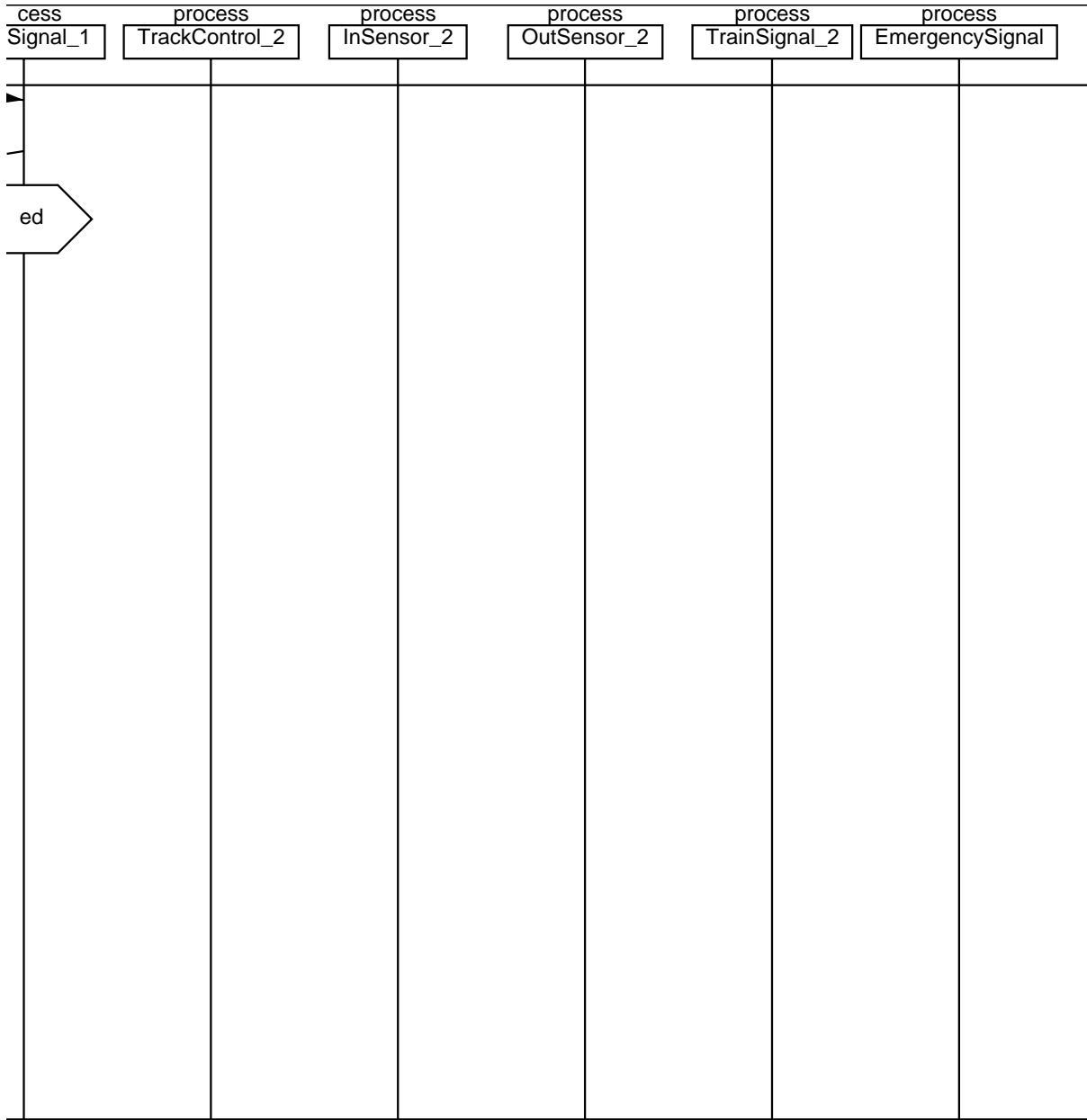
process
<<Block tr:2>>
TrainSignal

TrainSignal_2

process
EmergencySignal

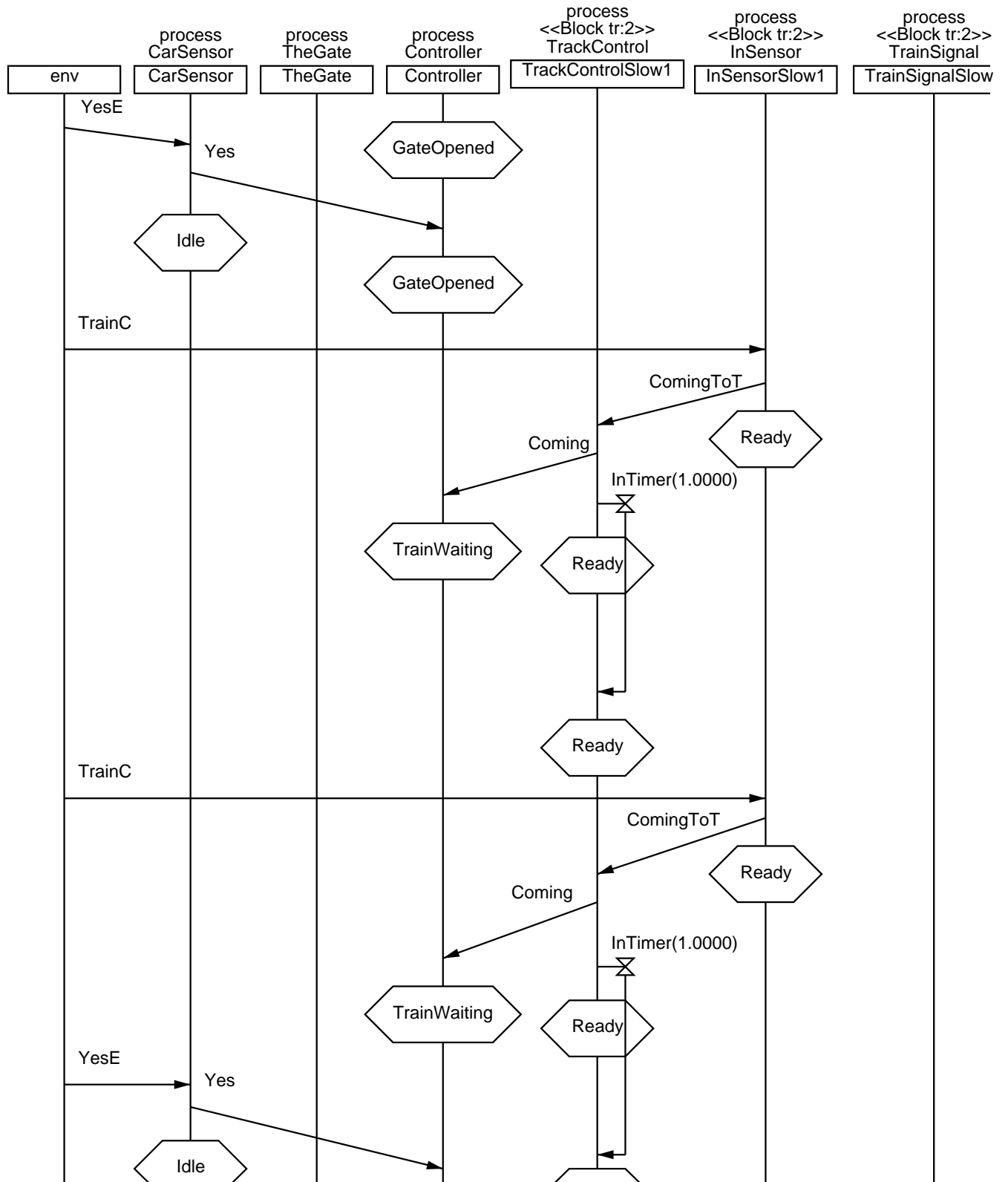
EmergencySignal

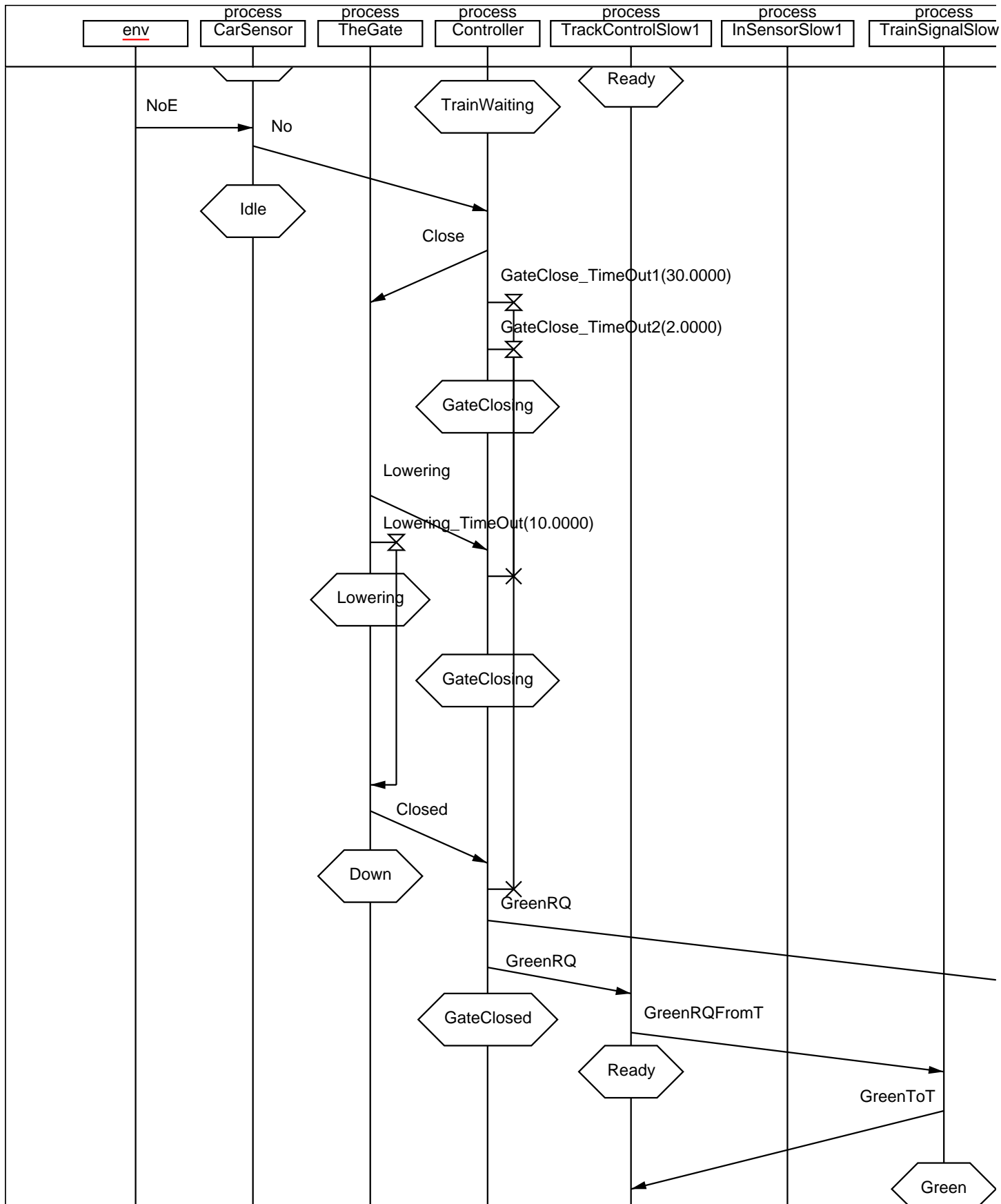


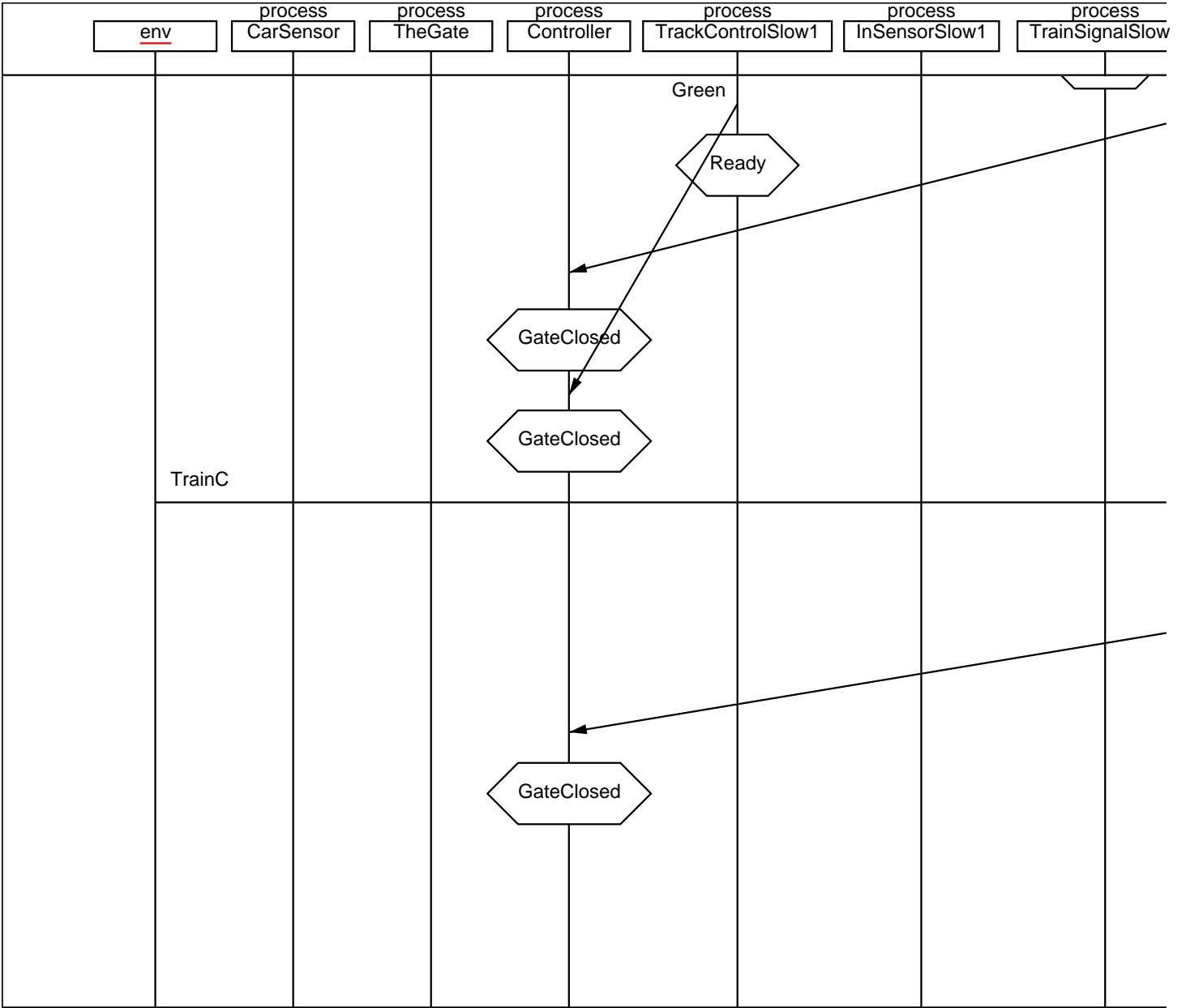


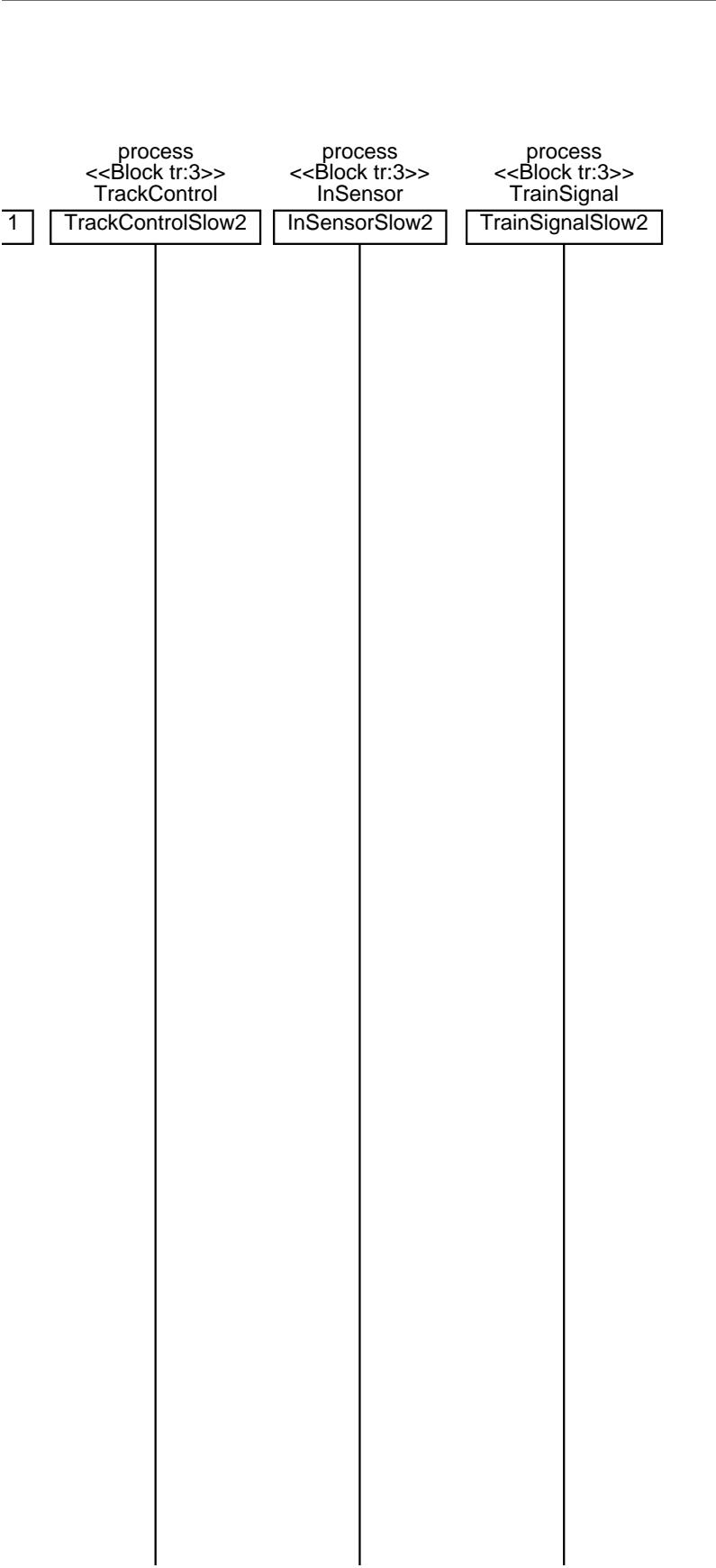
MSC Demo_TestCaseE

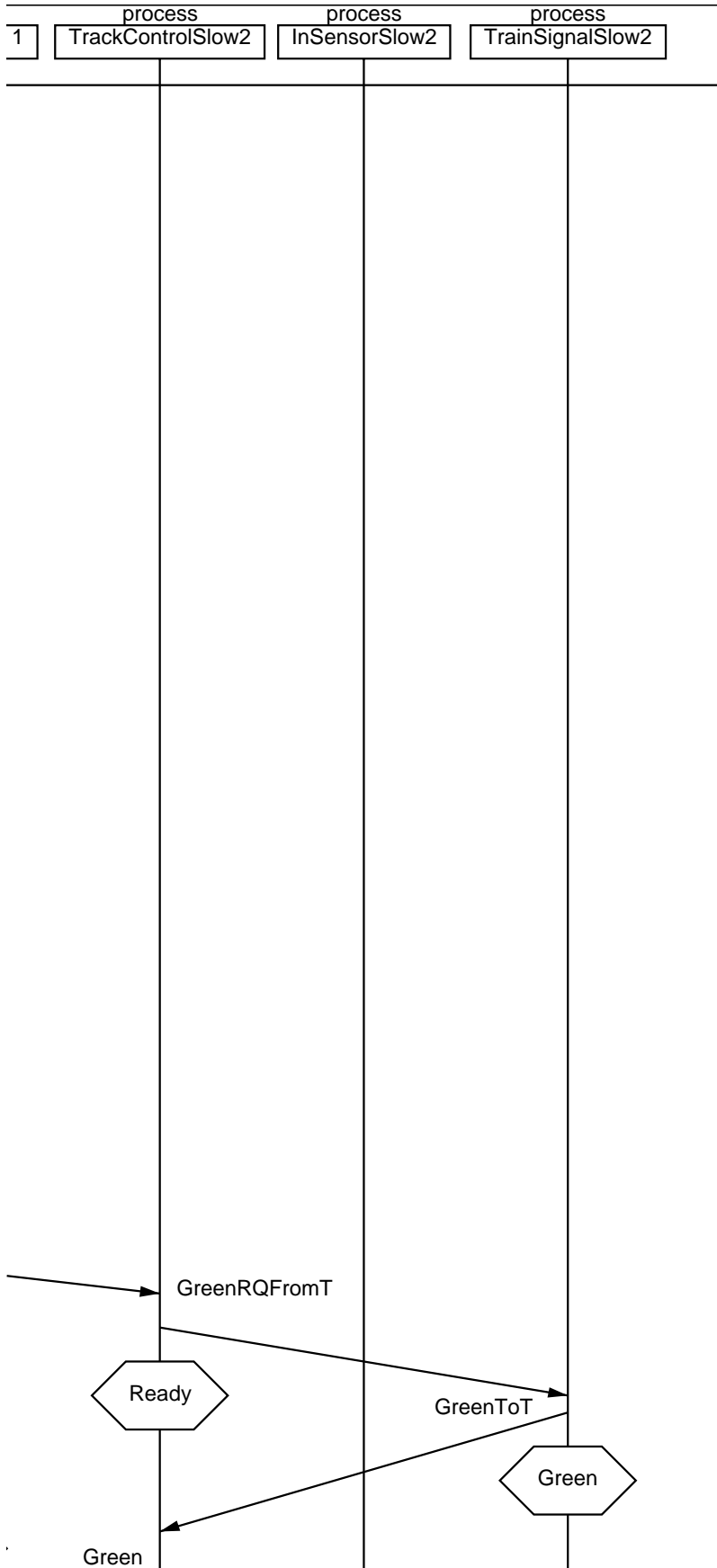
Simplified MSC from Simulation trace generated by SDL Simulator 4.3

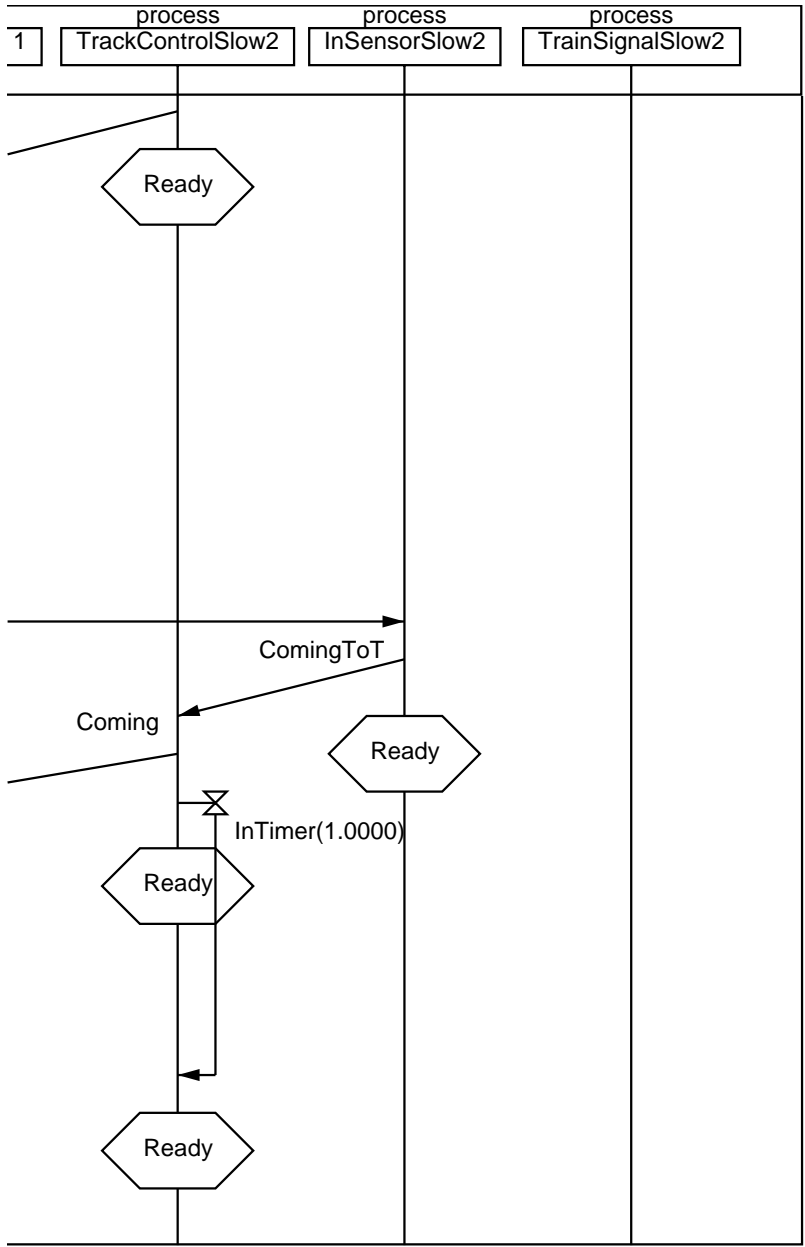








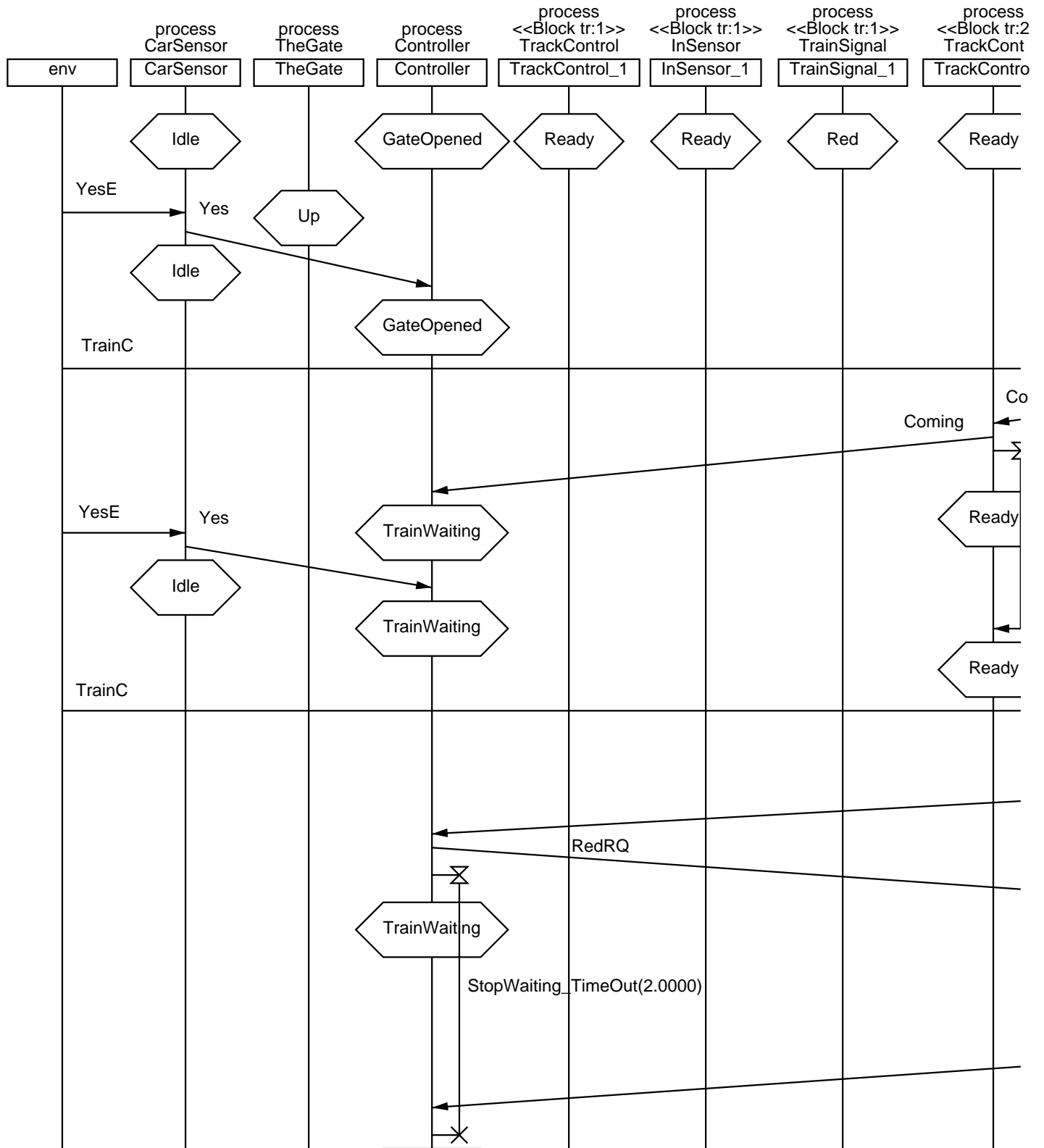


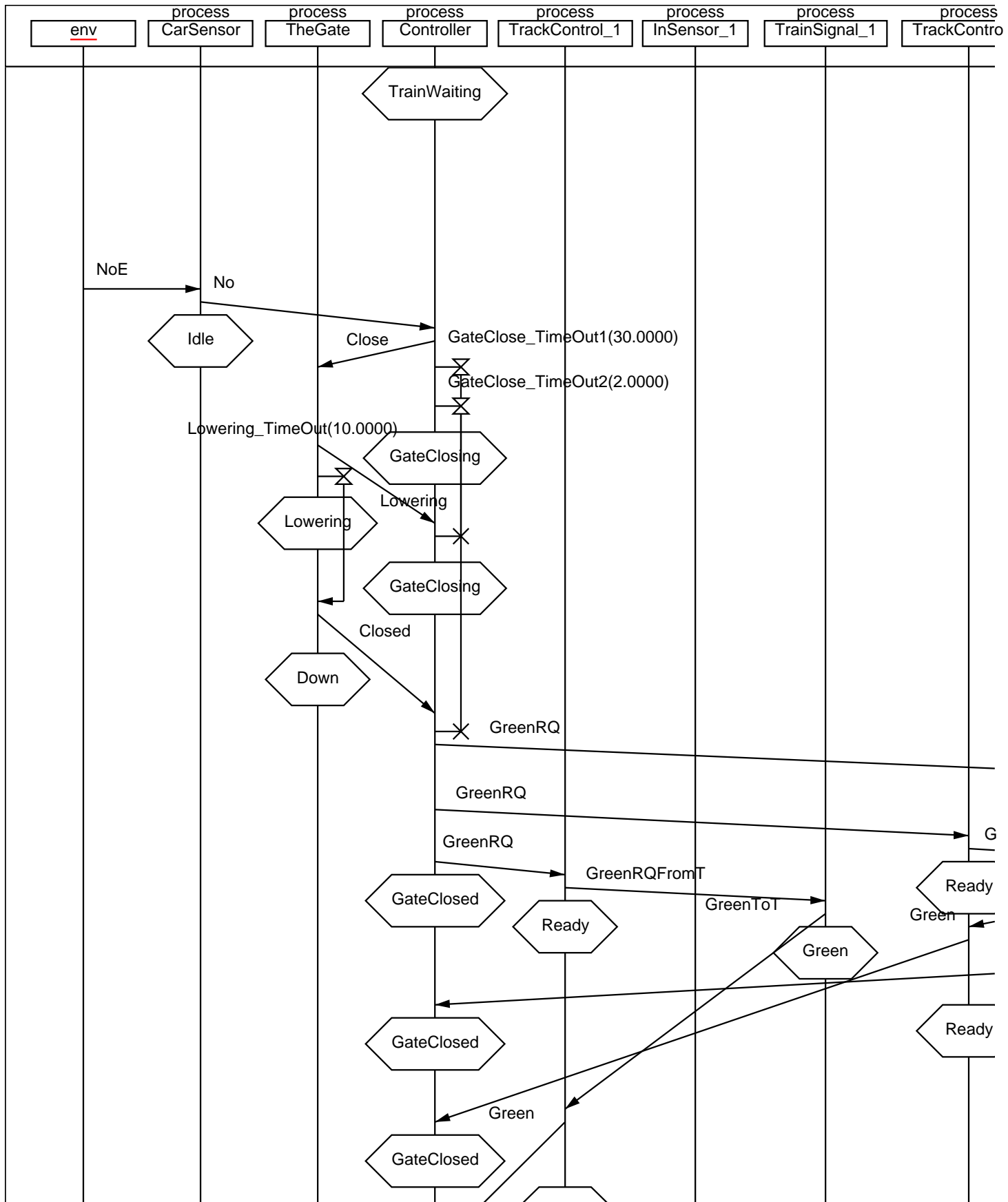


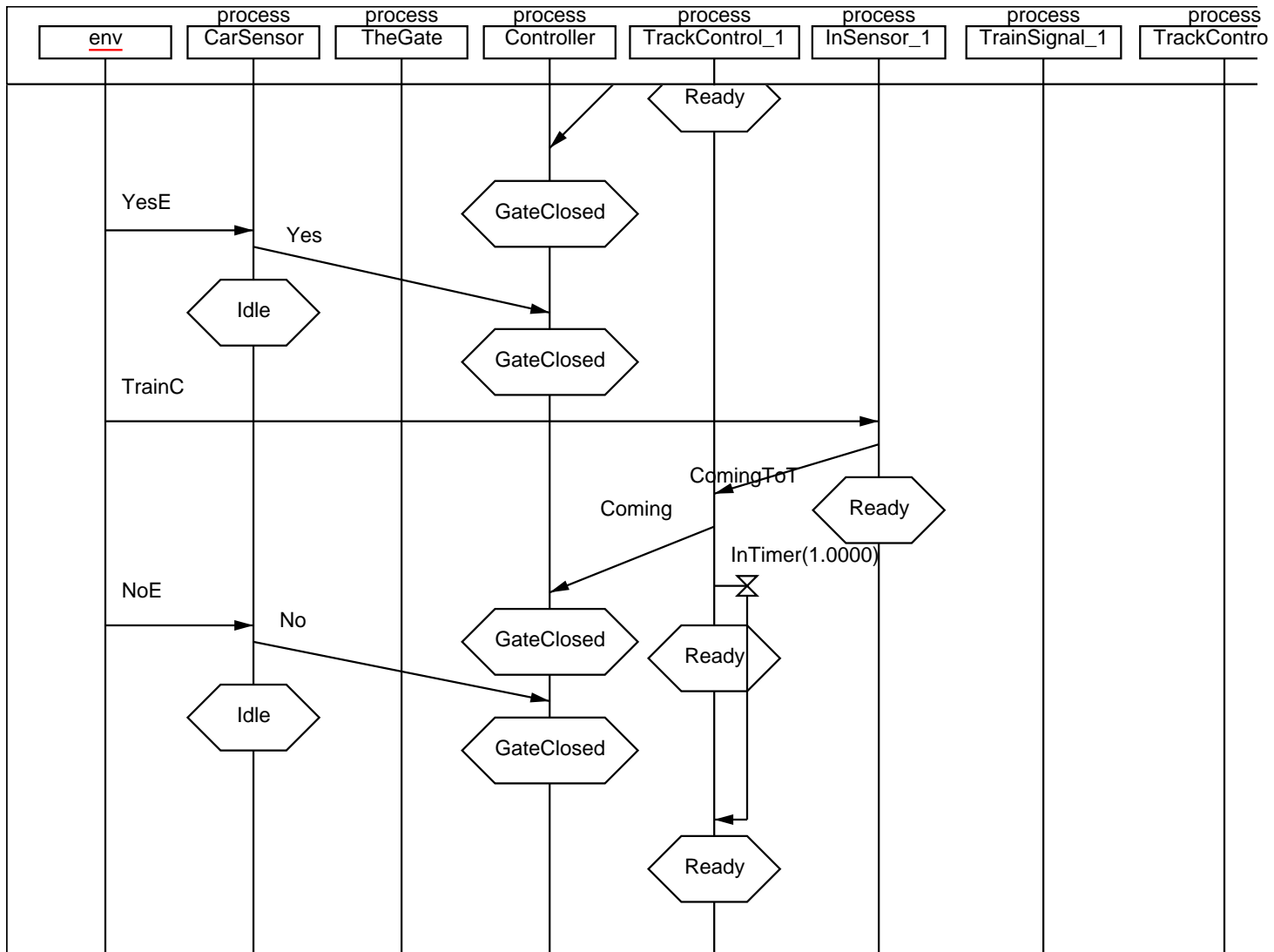
MSC Demo_TestCaseF_Strategy3

Simplified MSC from Simulation trace generated by SDL Simulator 4.3

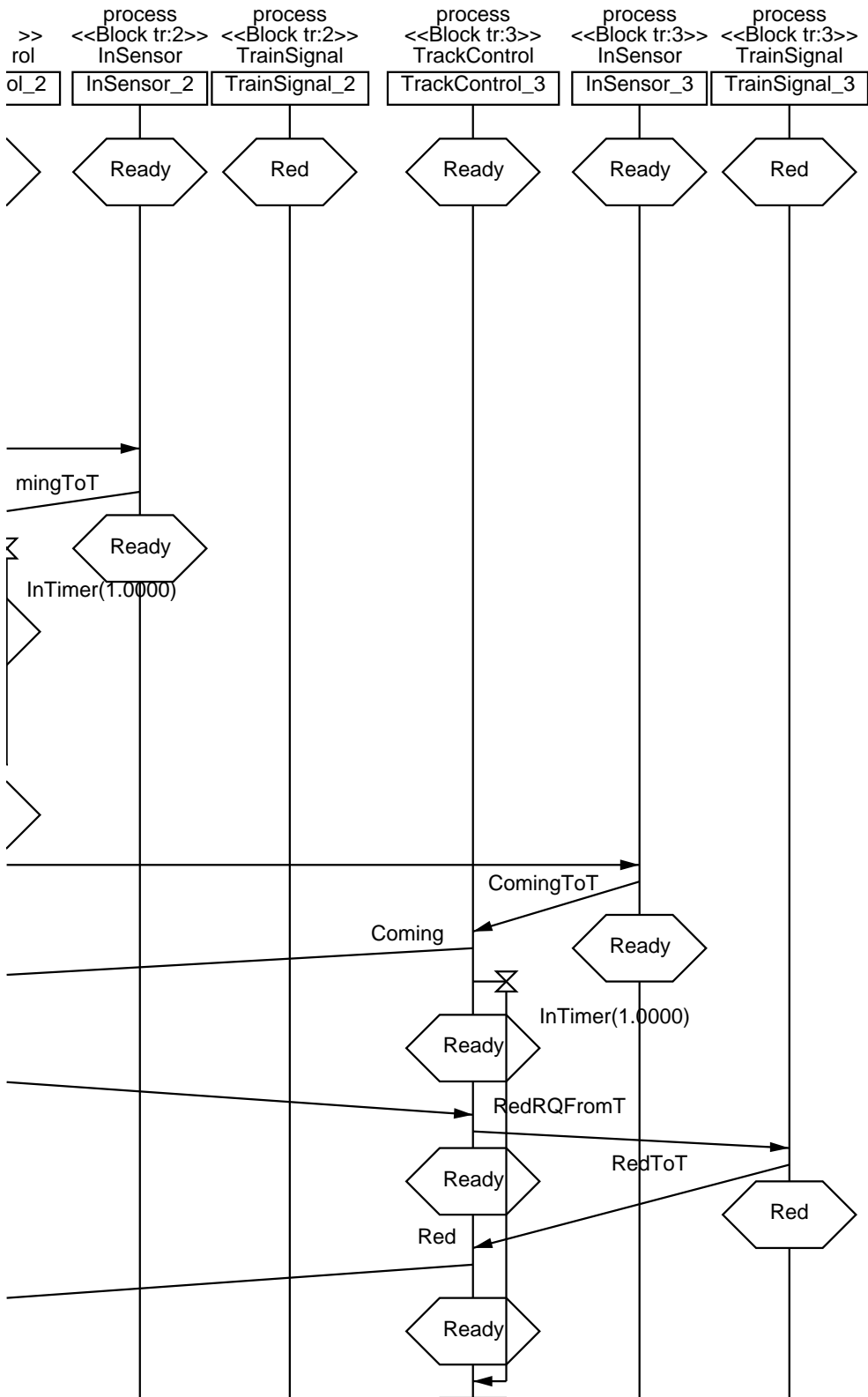
Track Layout:
There are three tracks:
Track1 is a fast track. Trac

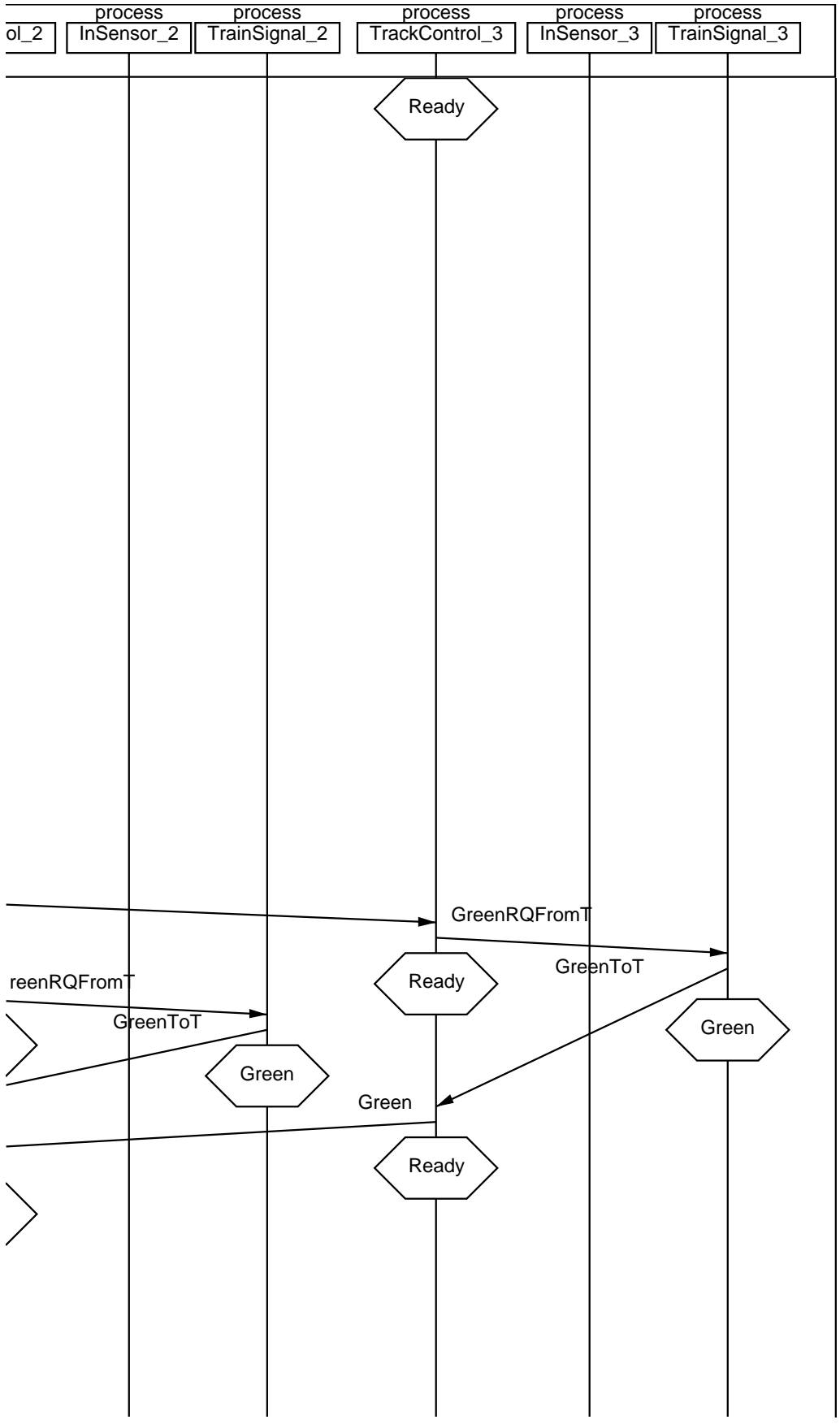






k 2 and Track 3 are slow tracks

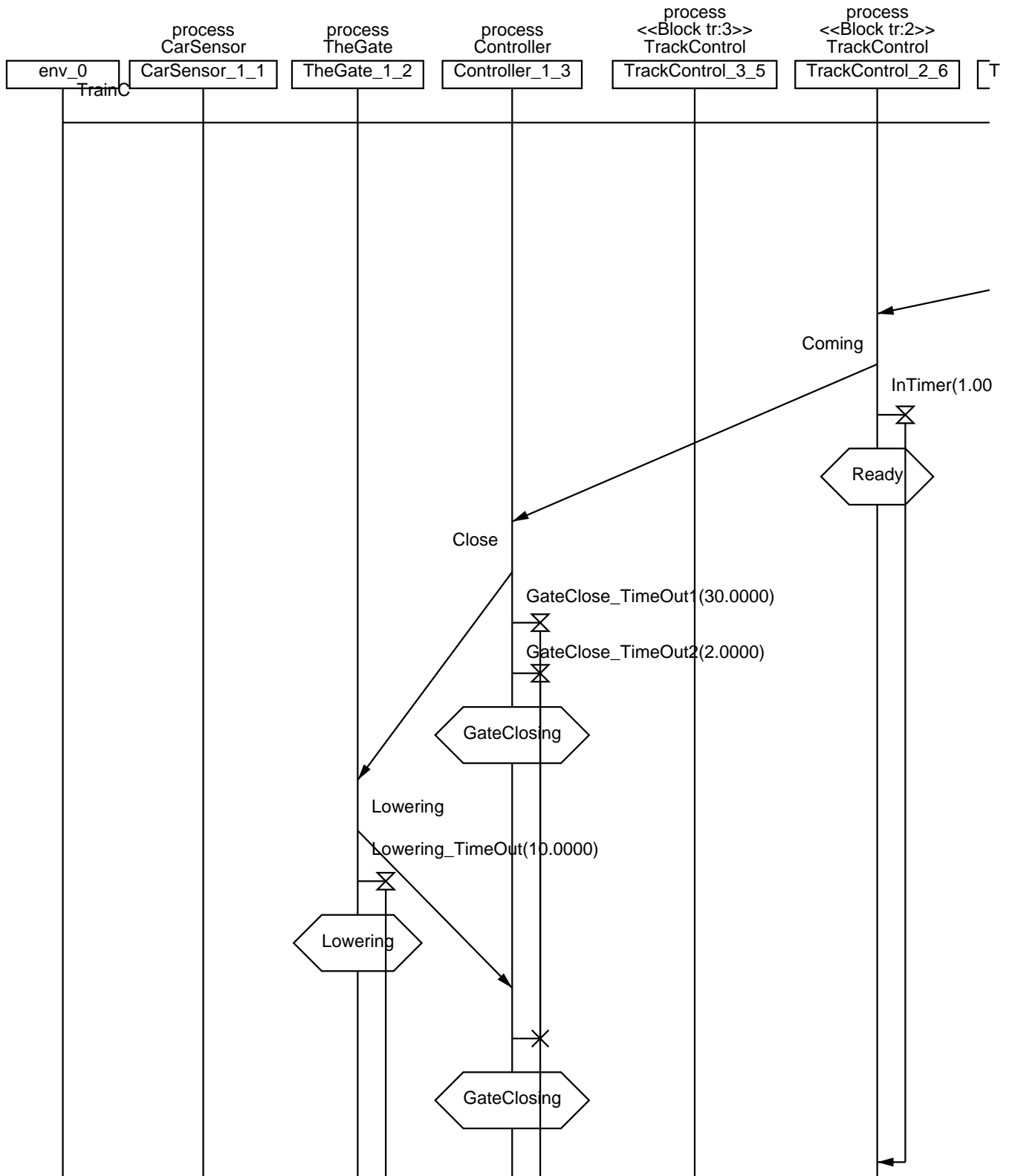


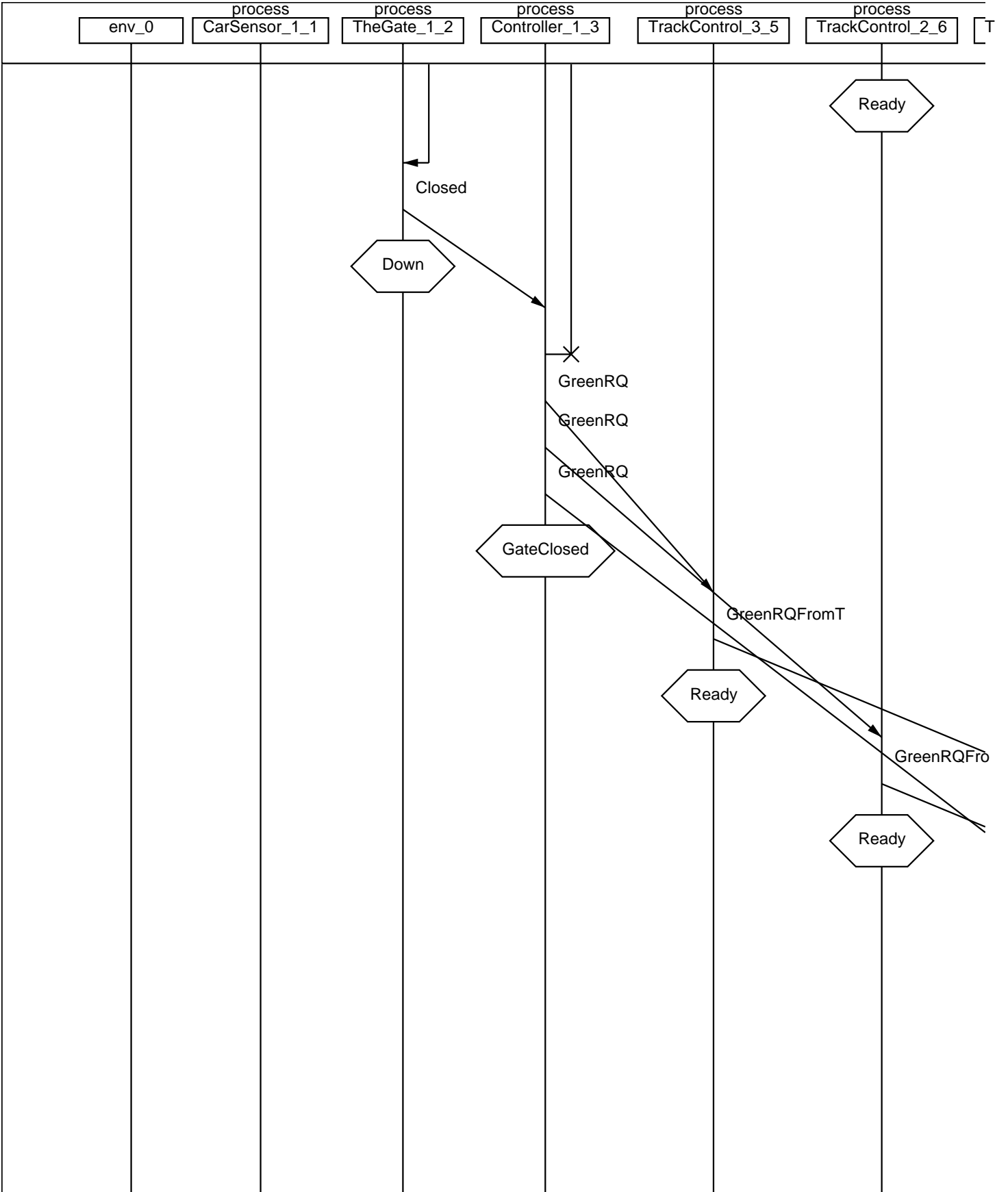


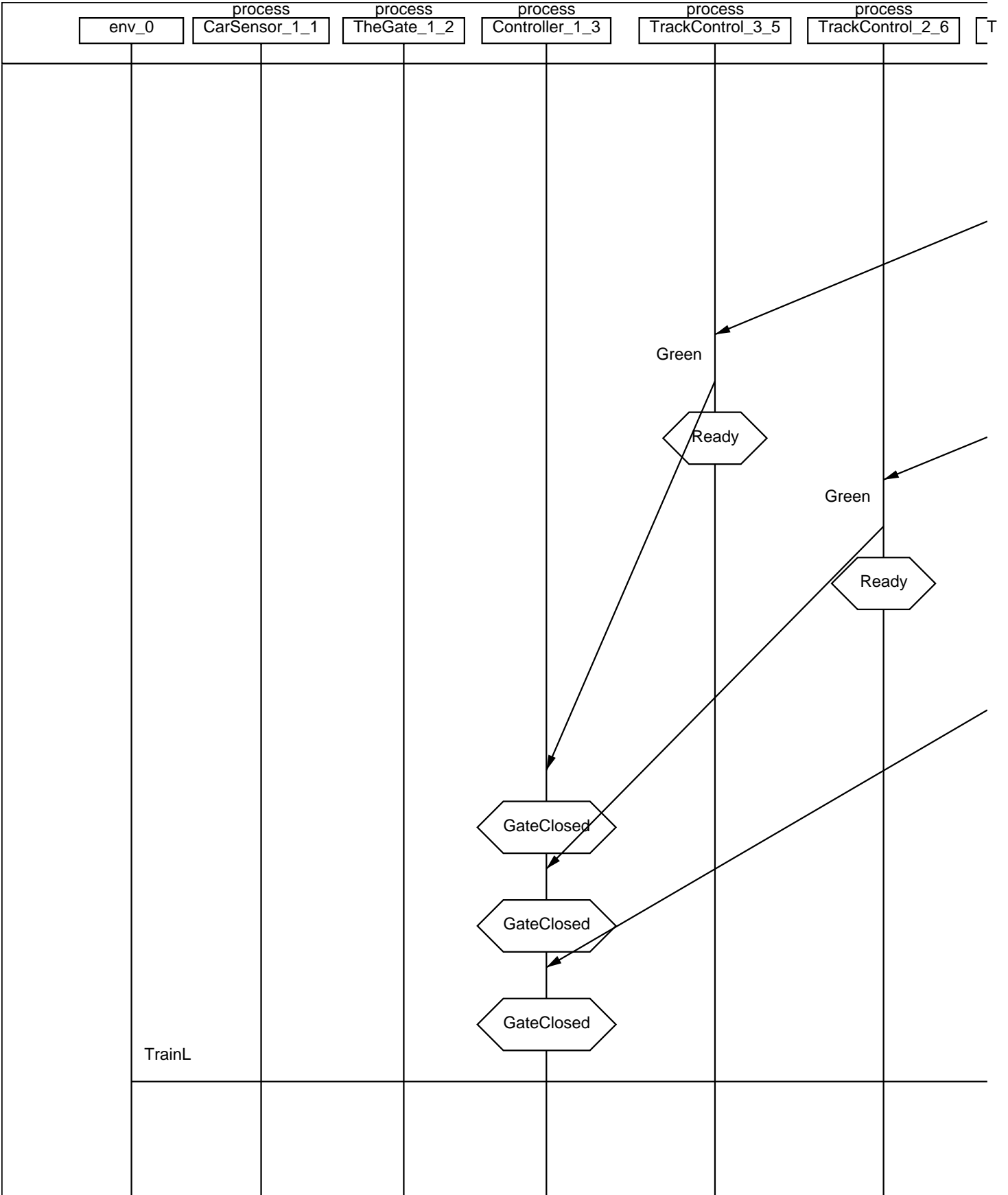
ol_2	process InSensor_2	process TrainSignal_2	process TrackControl_3	process InSensor_3	process TrainSignal_3

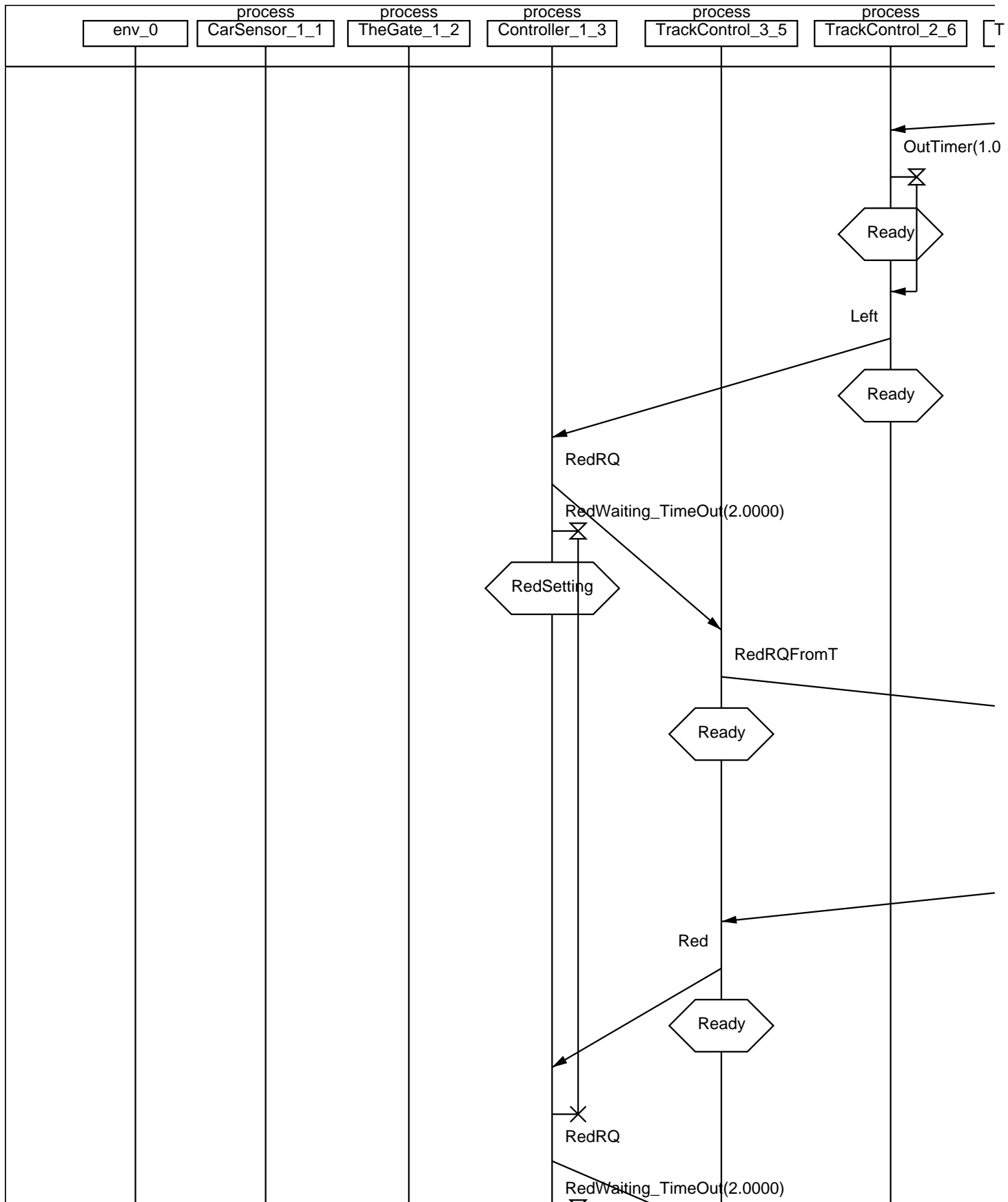
MSC CompleteMSC_TestCaseA

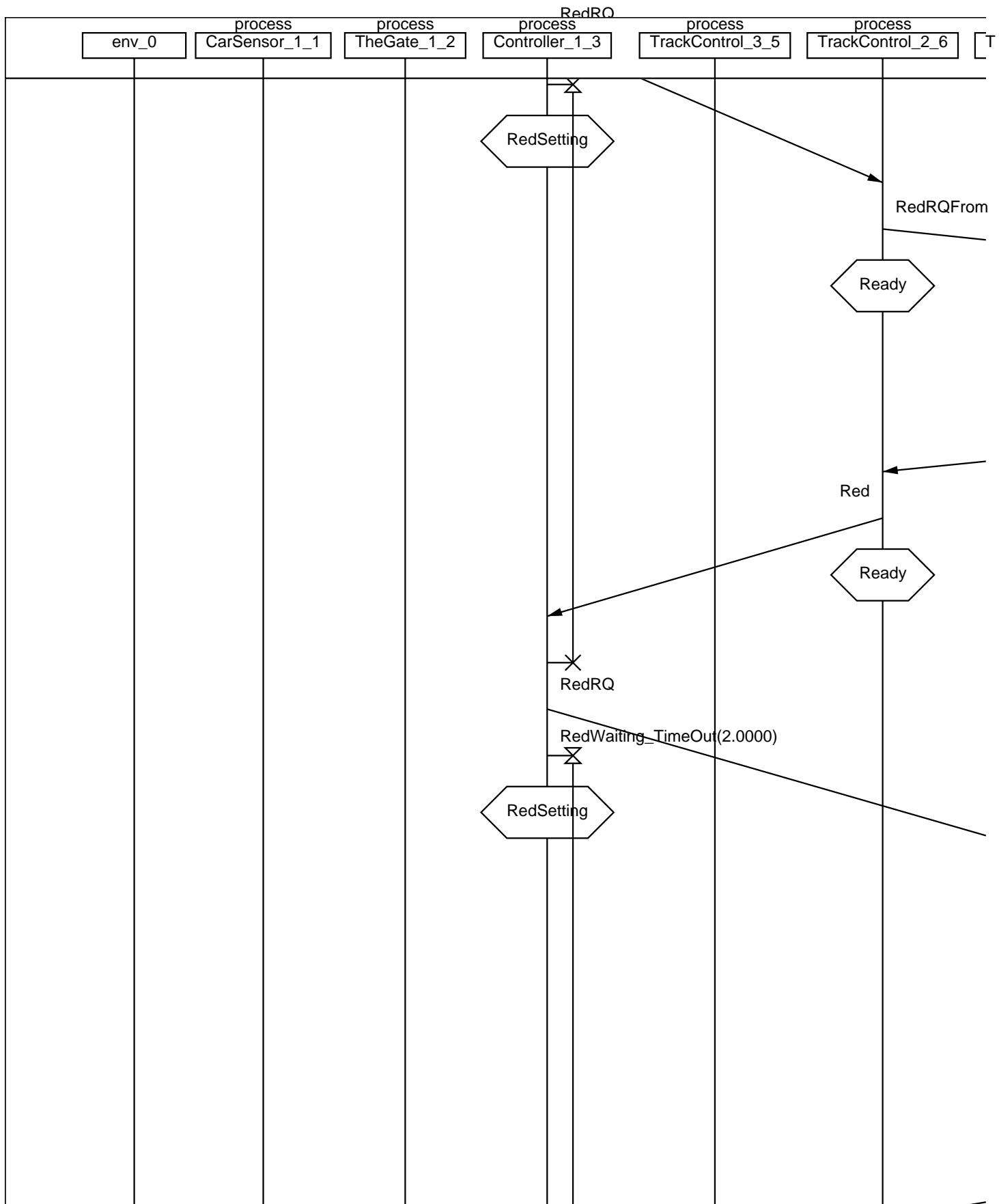
Simulation trace
generated by SDL Simulator 4.3

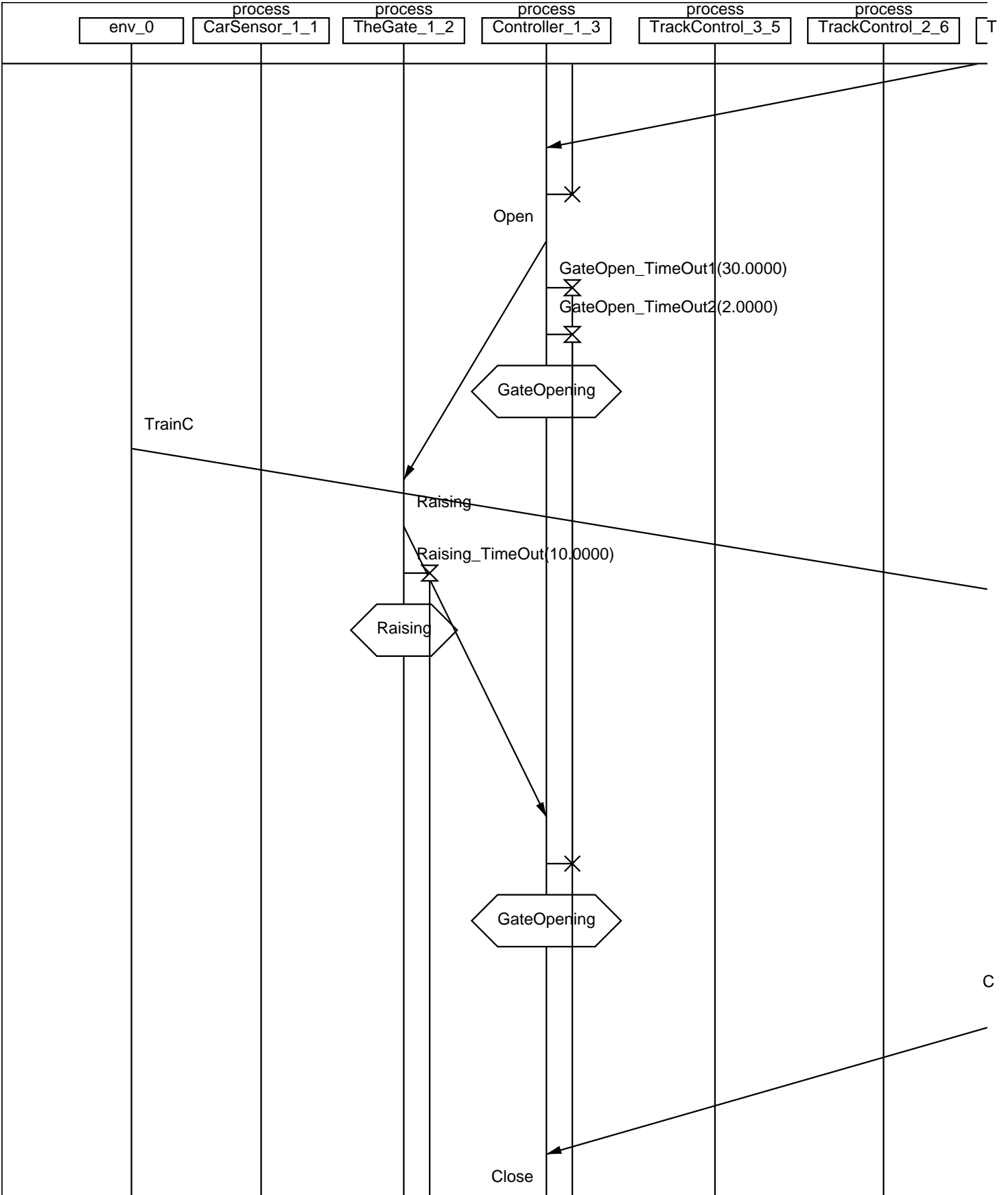


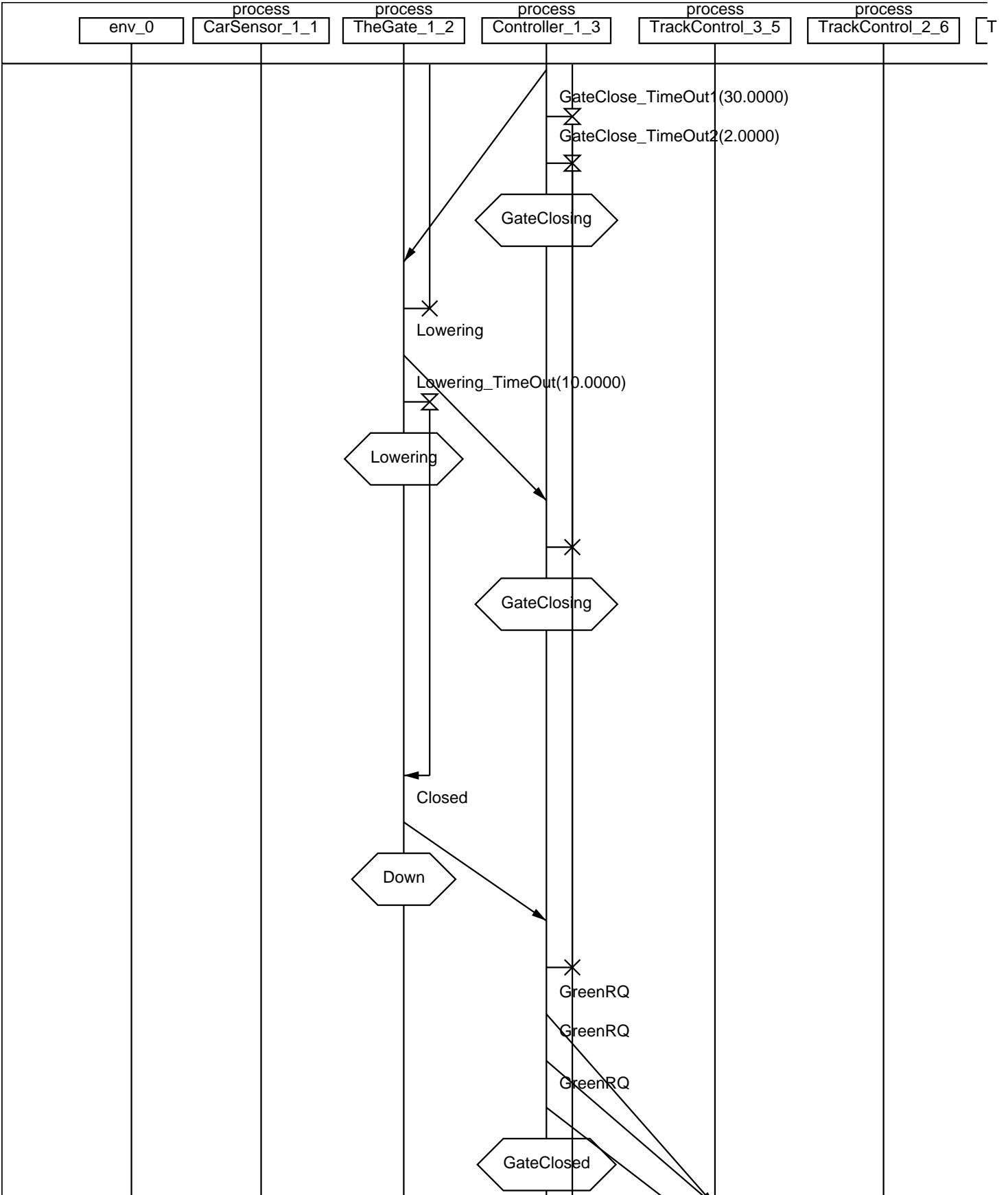


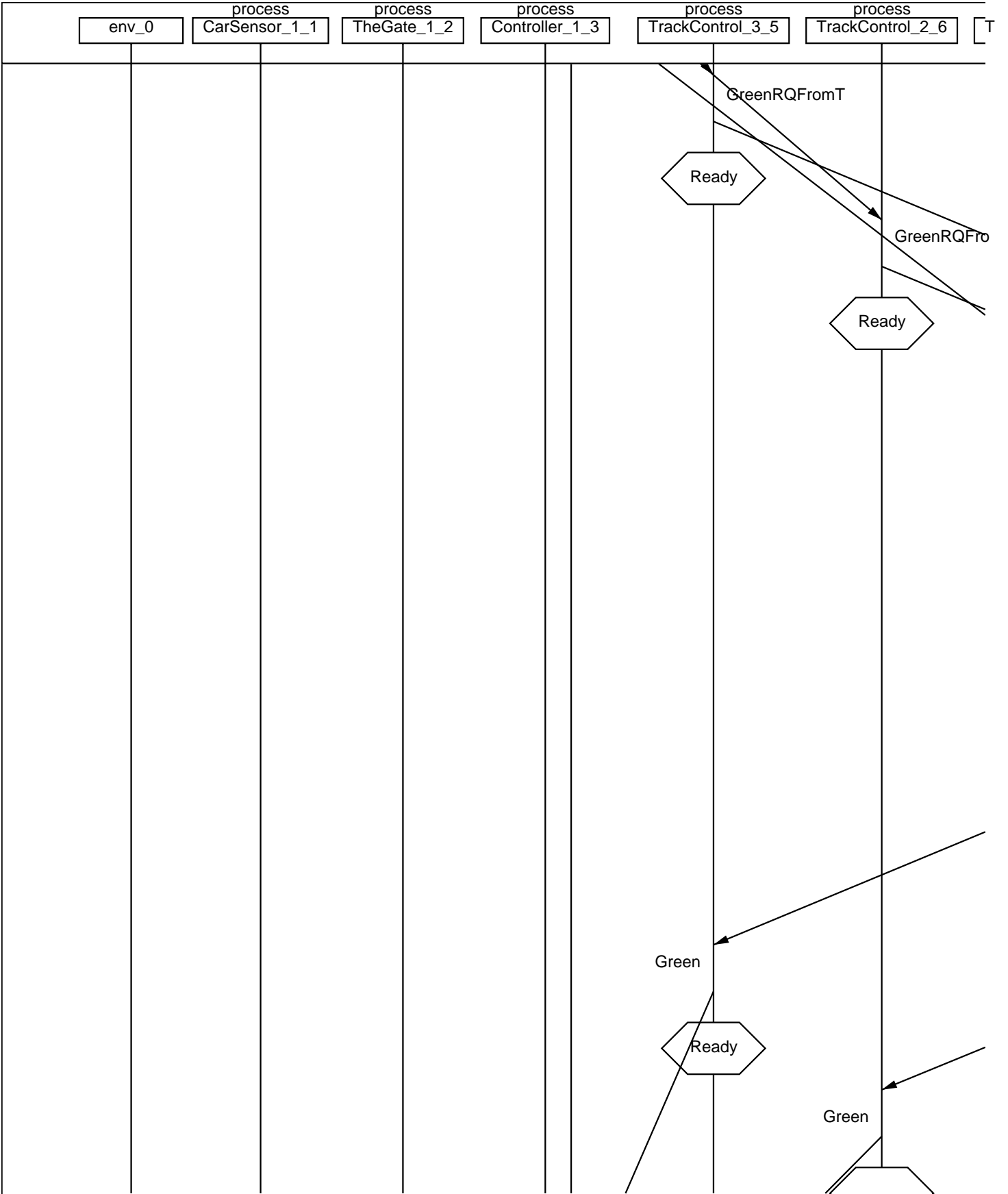


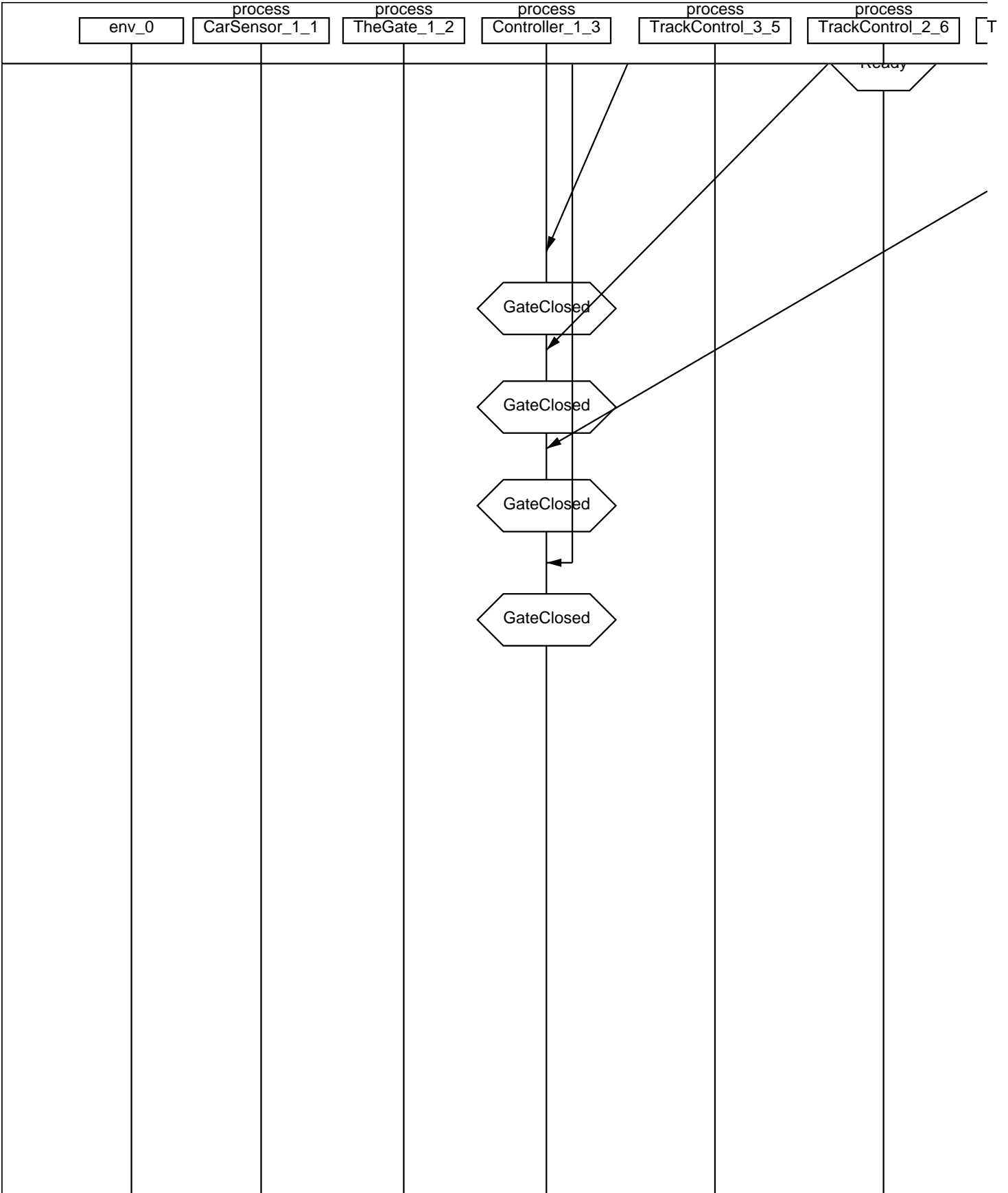


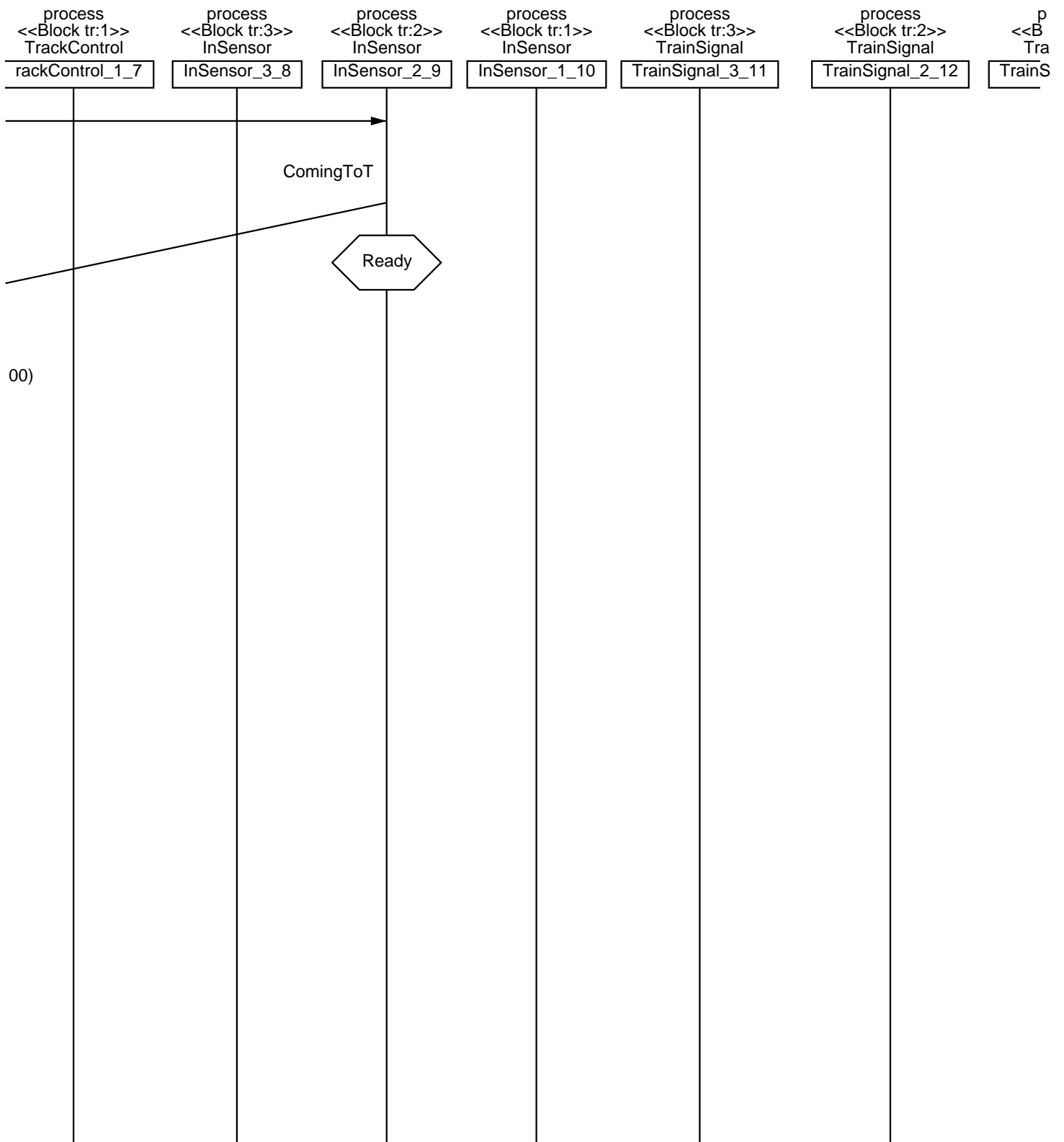


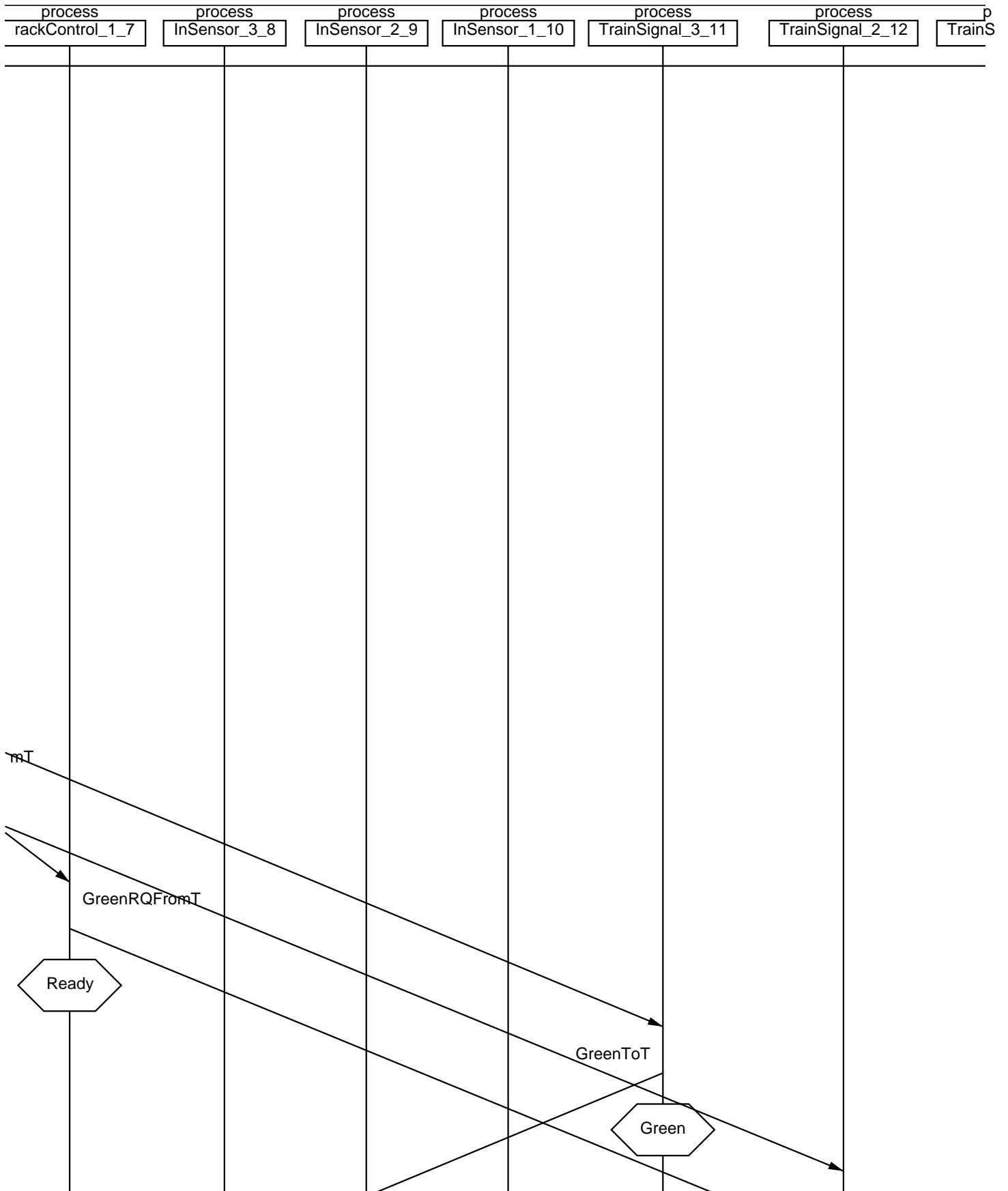


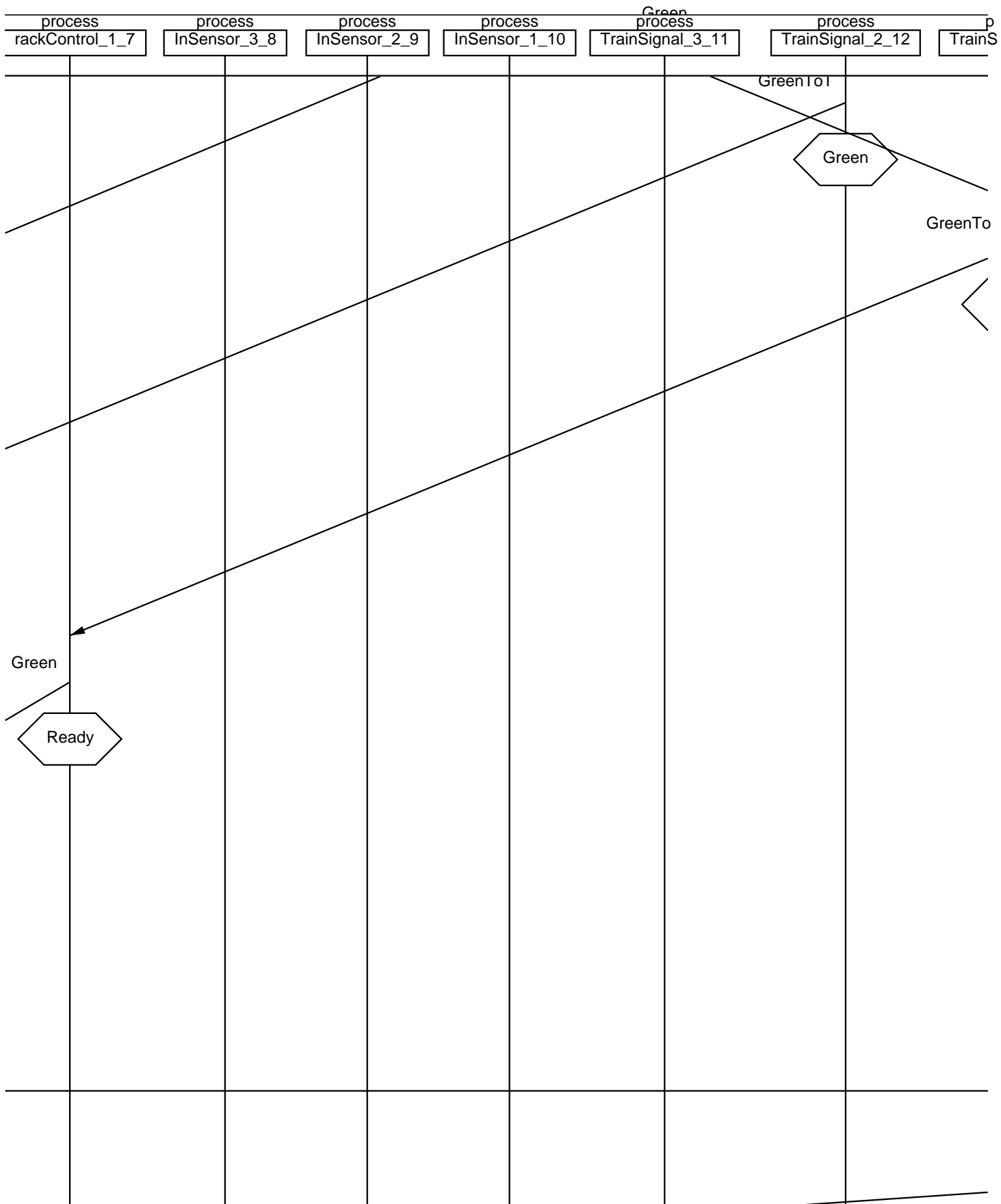


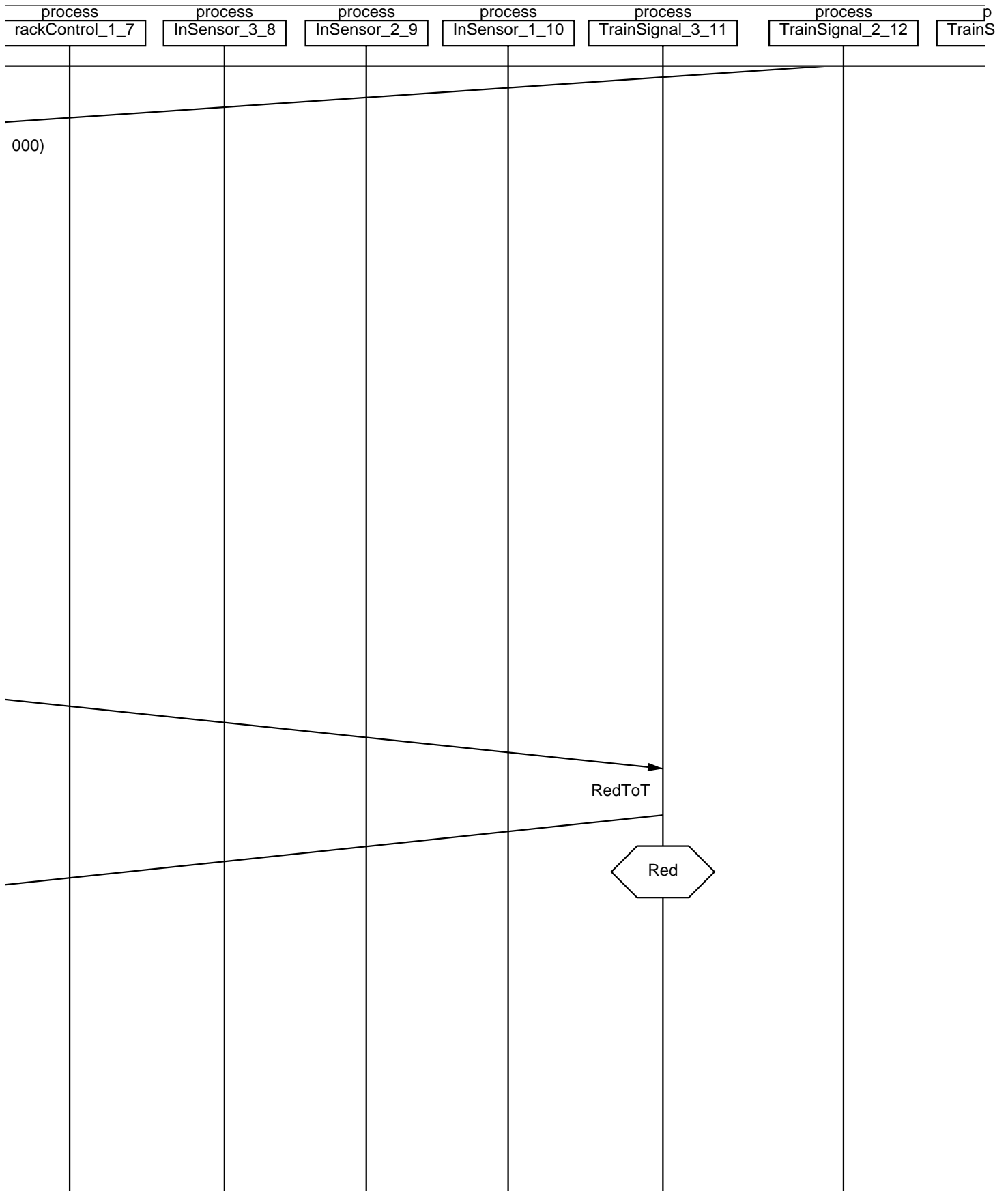


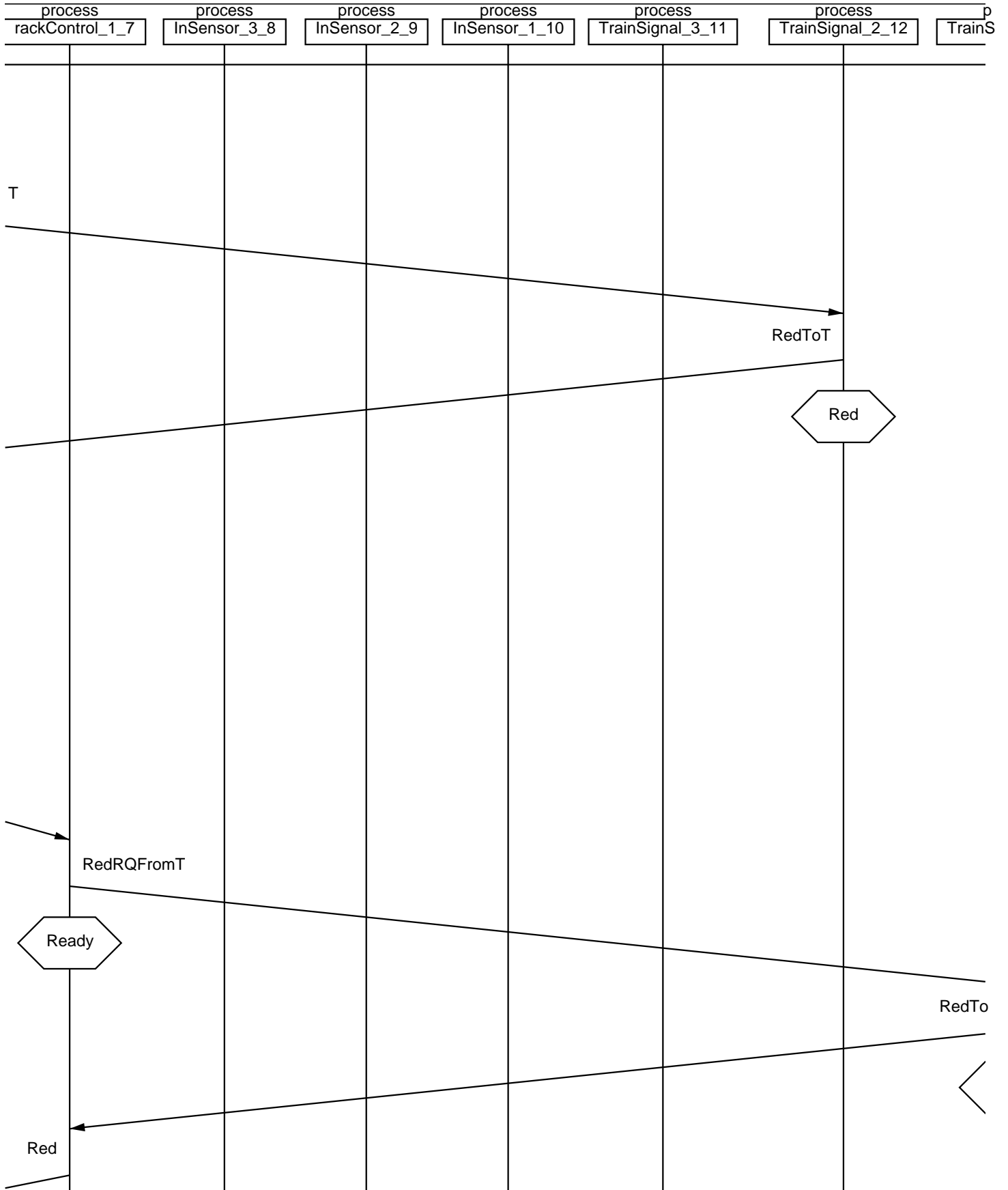


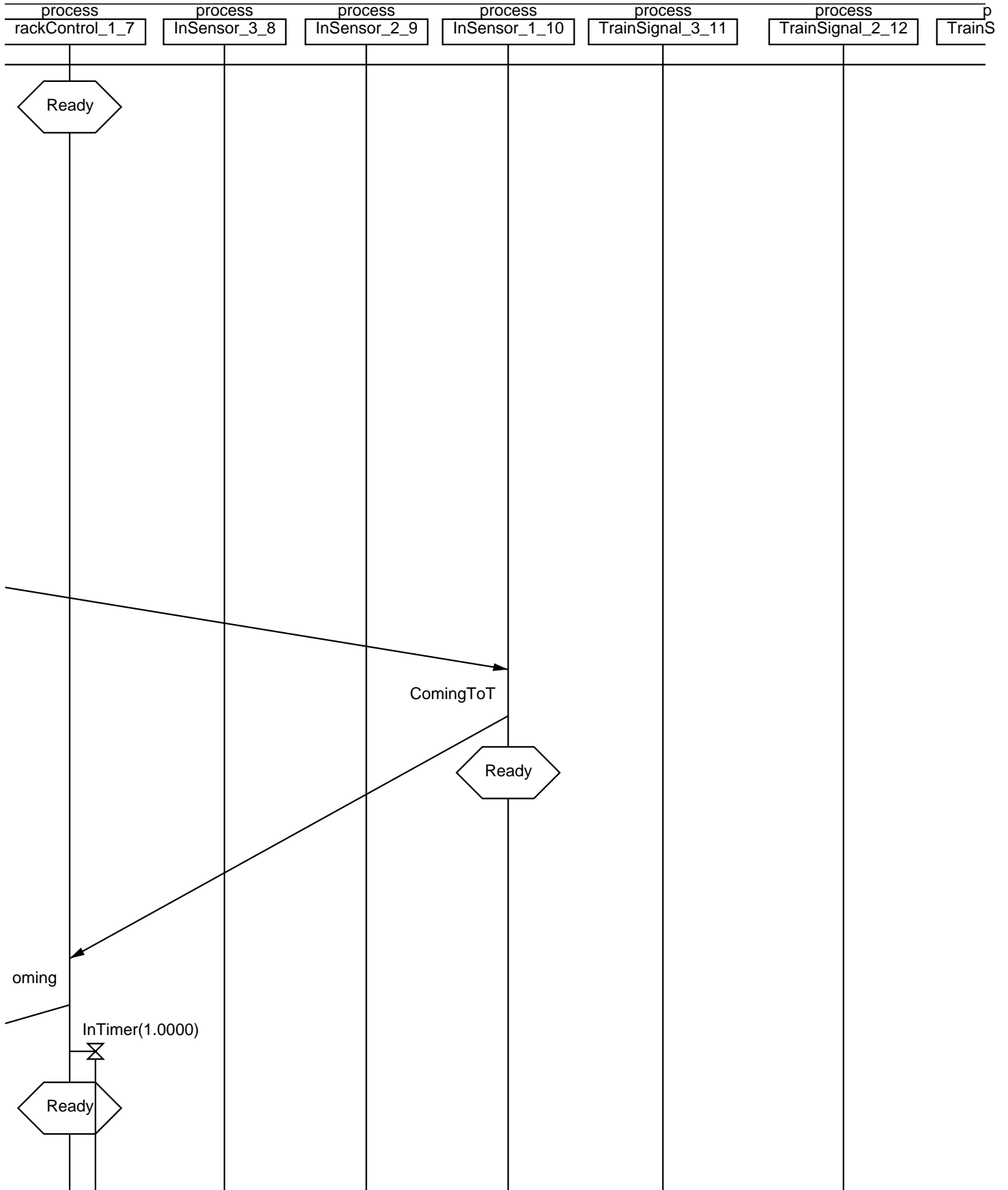


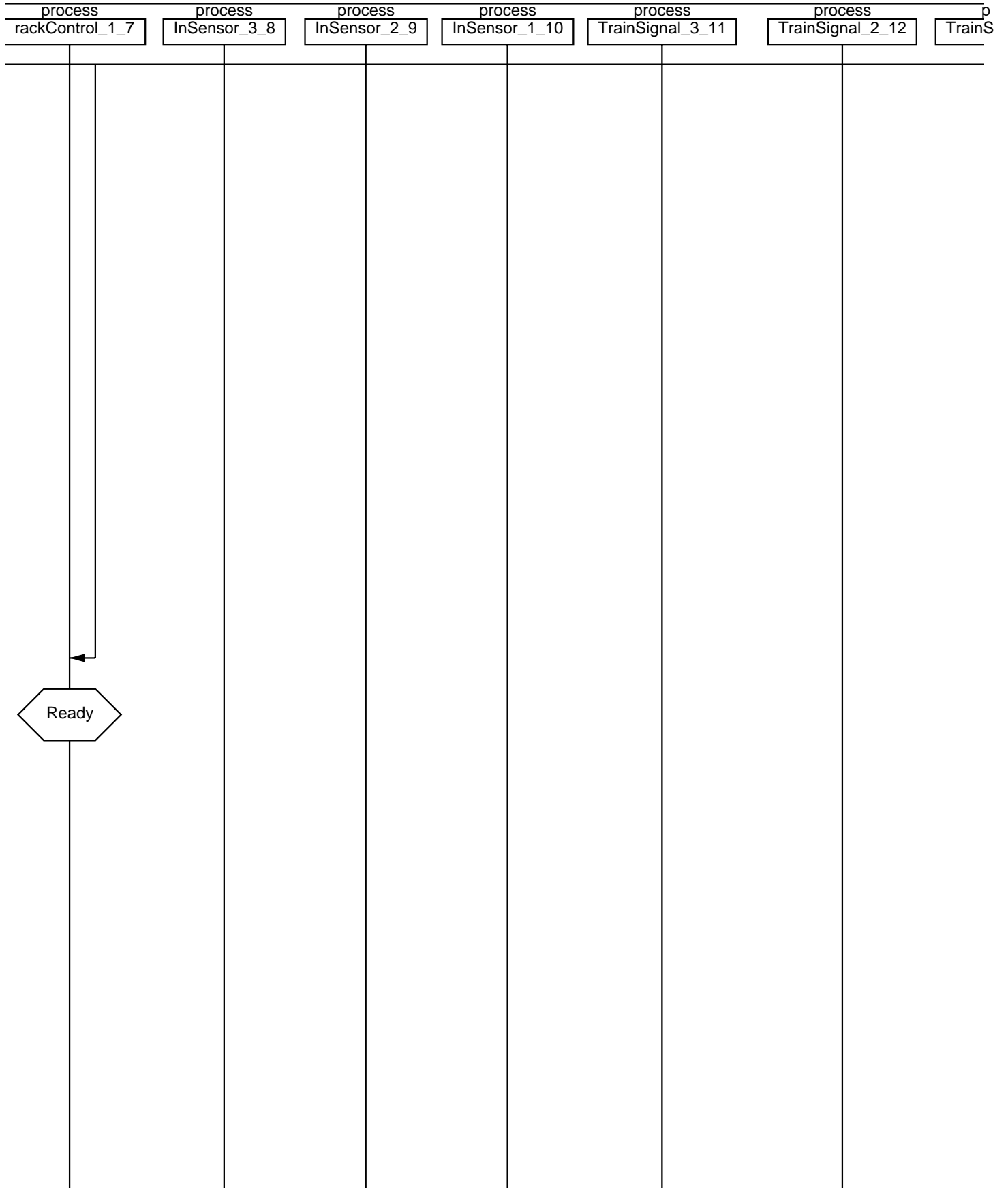


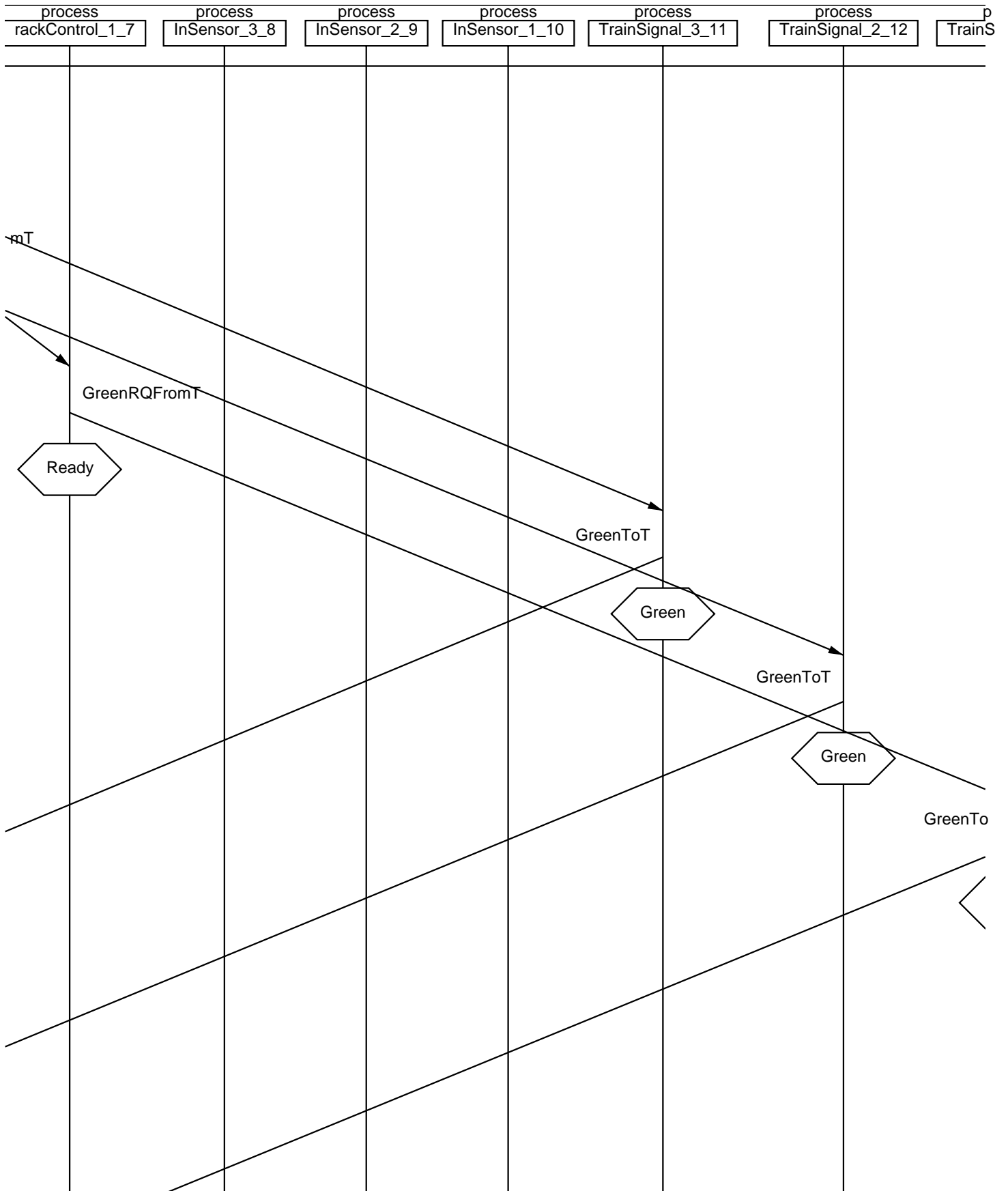


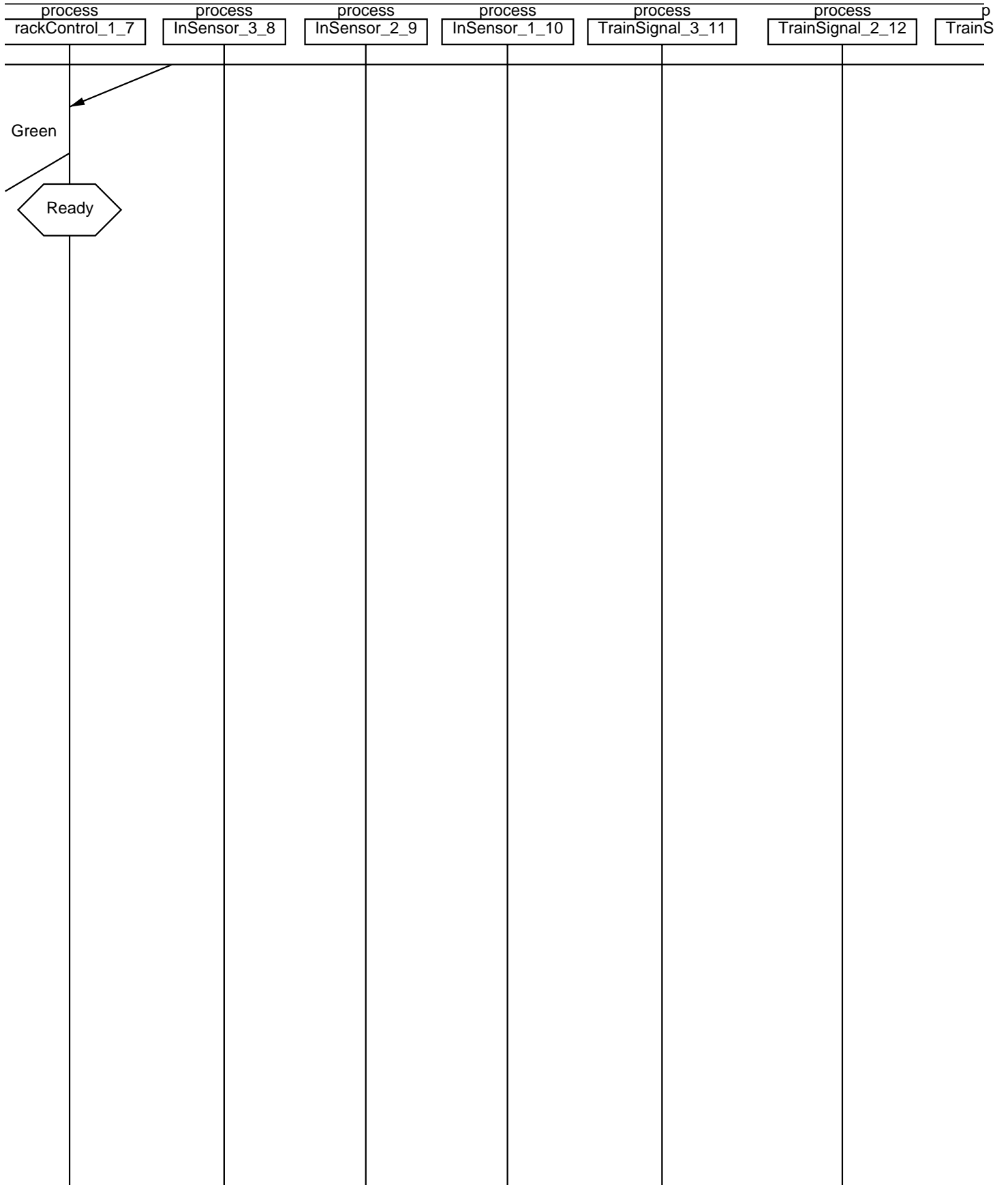












rocess
lock tr:1>>
inSignal

ignal_1_13

process
<<Block tr:3>>
OutSensor

OutSensor_3_14

process
<<Block tr:2>>
OutSensor

OutSensor_2_15

process
<<Block tr:1>>
OutSensor

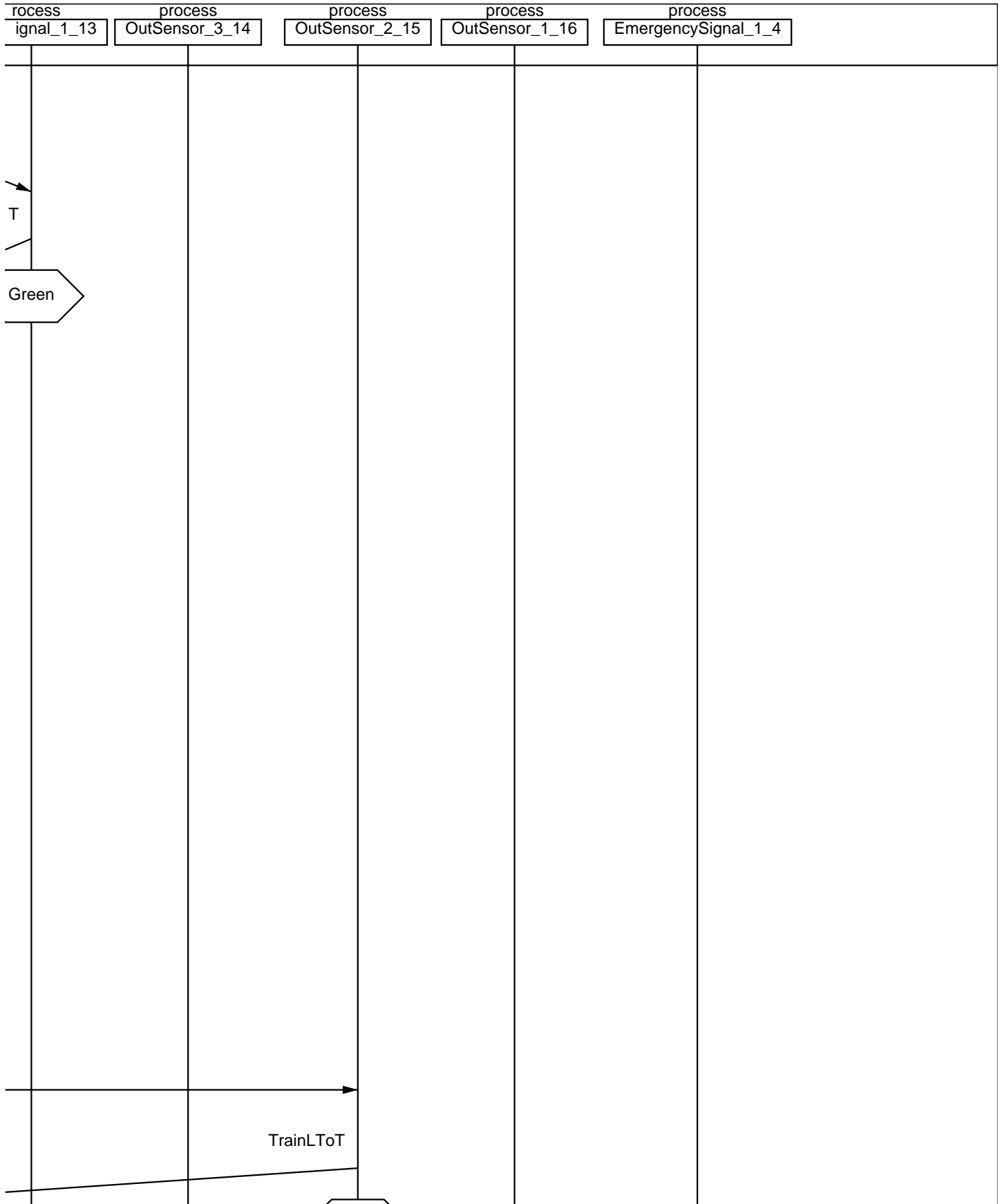
OutSensor_1_16

process
EmergencySignal

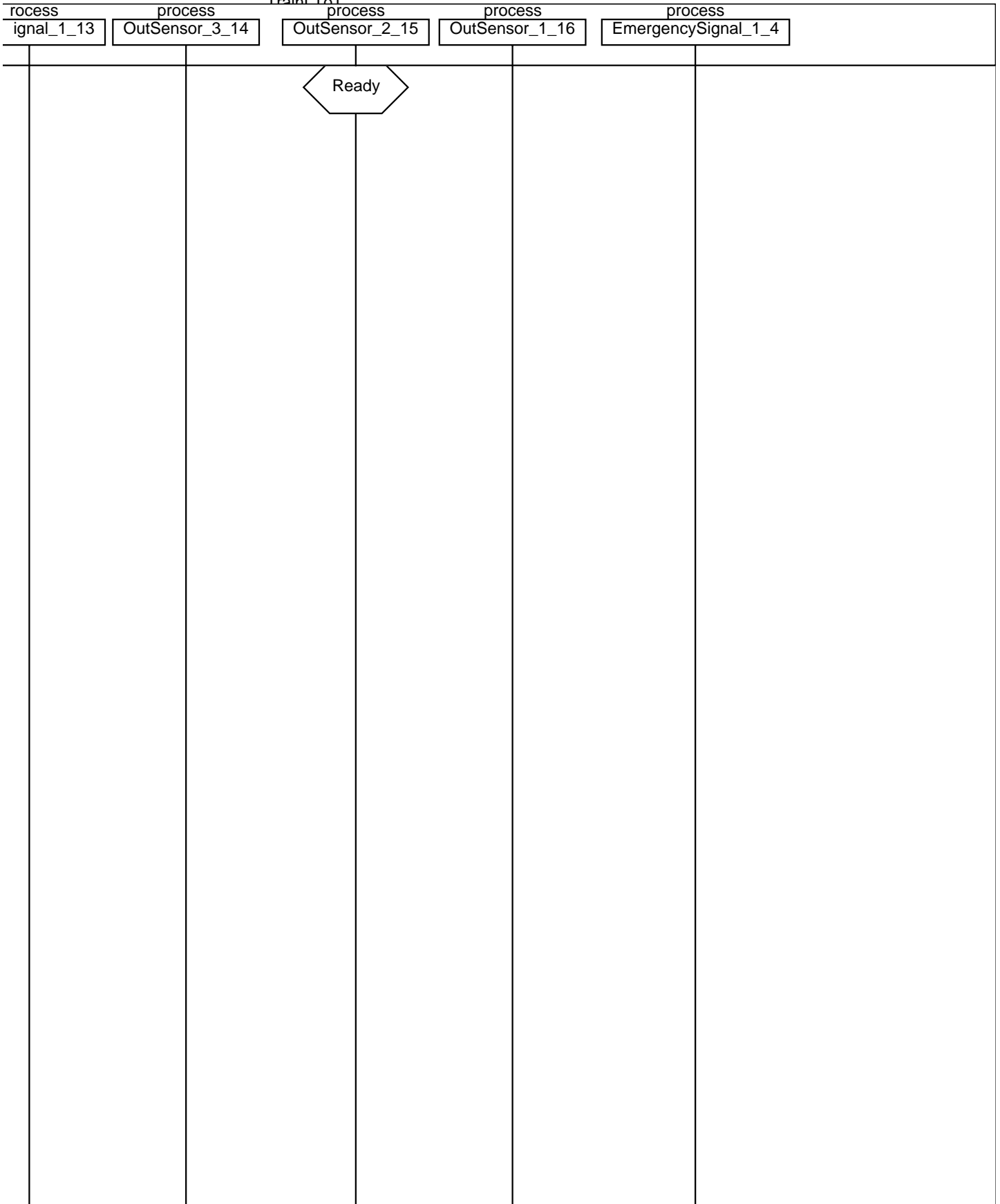
EmergencySignal_1_4

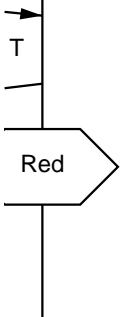
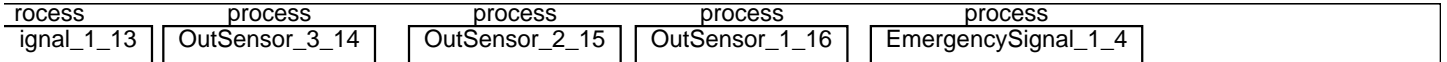
rocess ignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16	process EmergencySignal_1_4
----------------------	---------------------------	---------------------------	---------------------------	--------------------------------

--	--	--	--	--	--



Train ToT



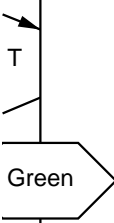
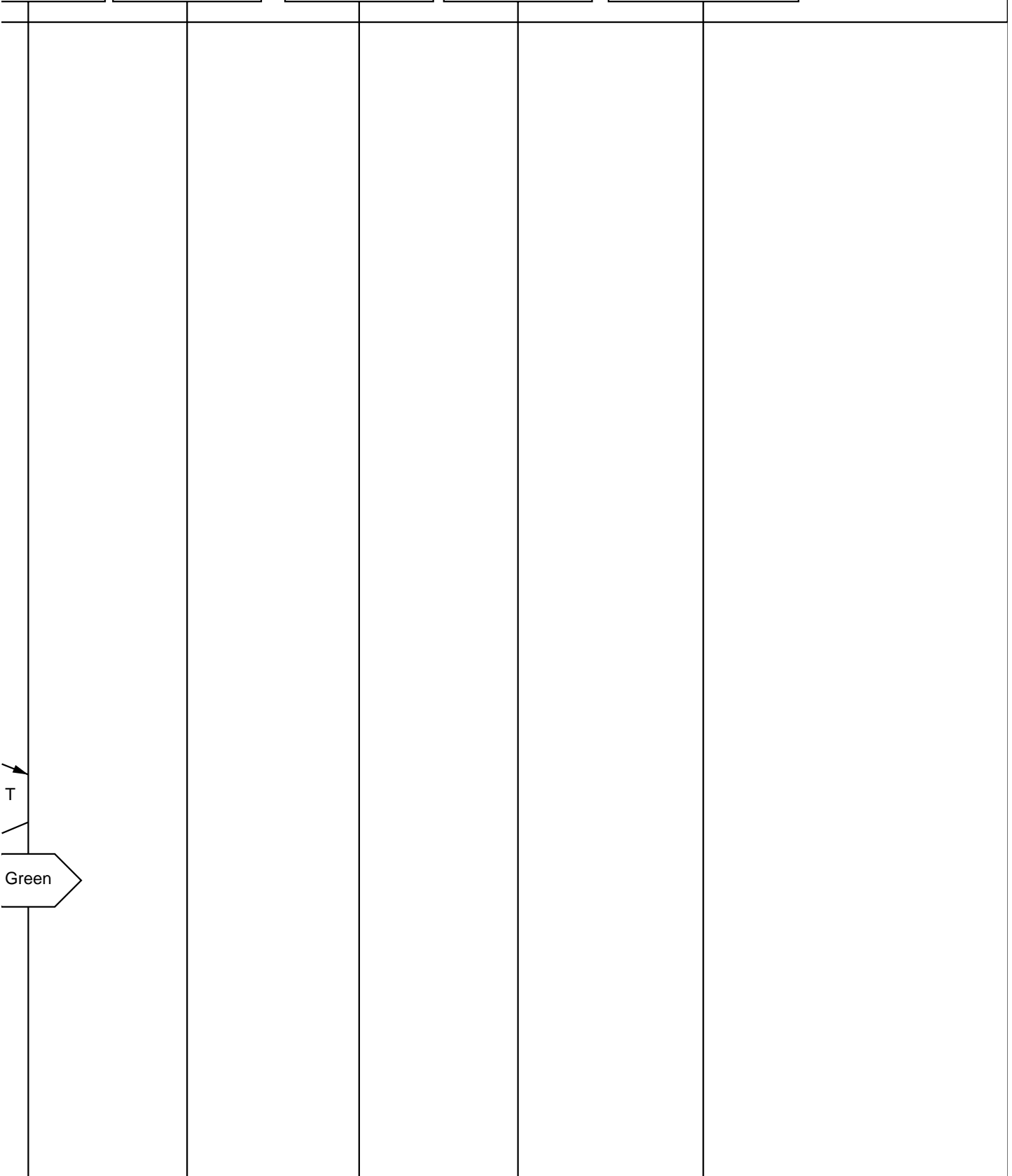
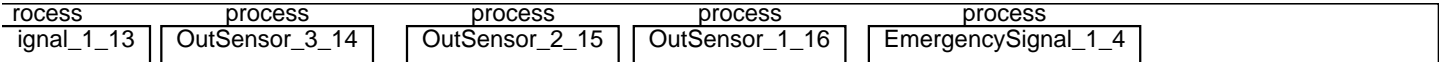


rocess ignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16	process EmergencySignal_1_4
----------------------	---------------------------	---------------------------	---------------------------	--------------------------------

--	--	--	--	--	--

rocess ignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16	process EmergencySignal_1_4
----------------------	---------------------------	---------------------------	---------------------------	--------------------------------

--	--	--	--	--	--

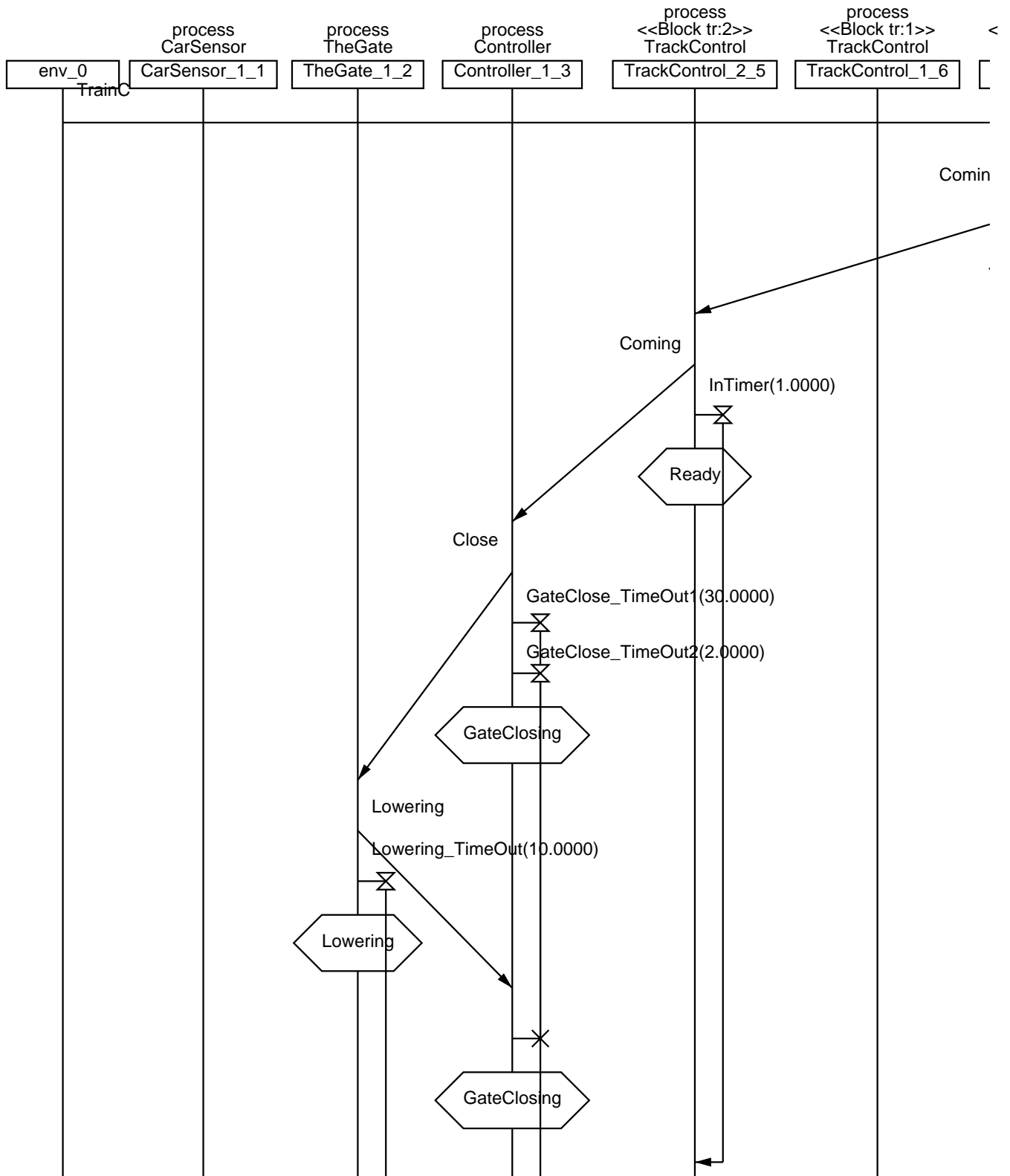


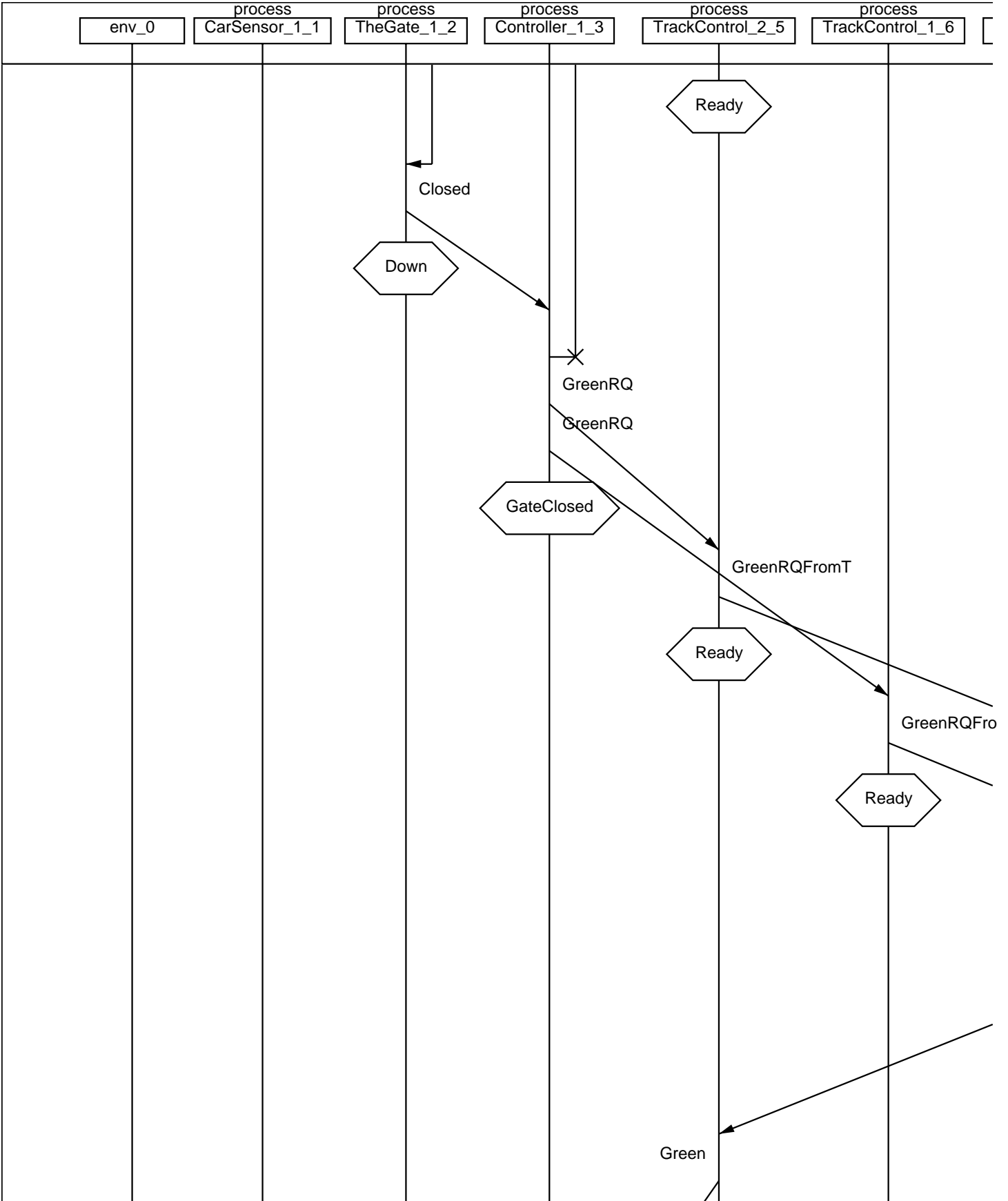
rocess ignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16	process EmergencySignal_1_4
----------------------	---------------------------	---------------------------	---------------------------	--------------------------------

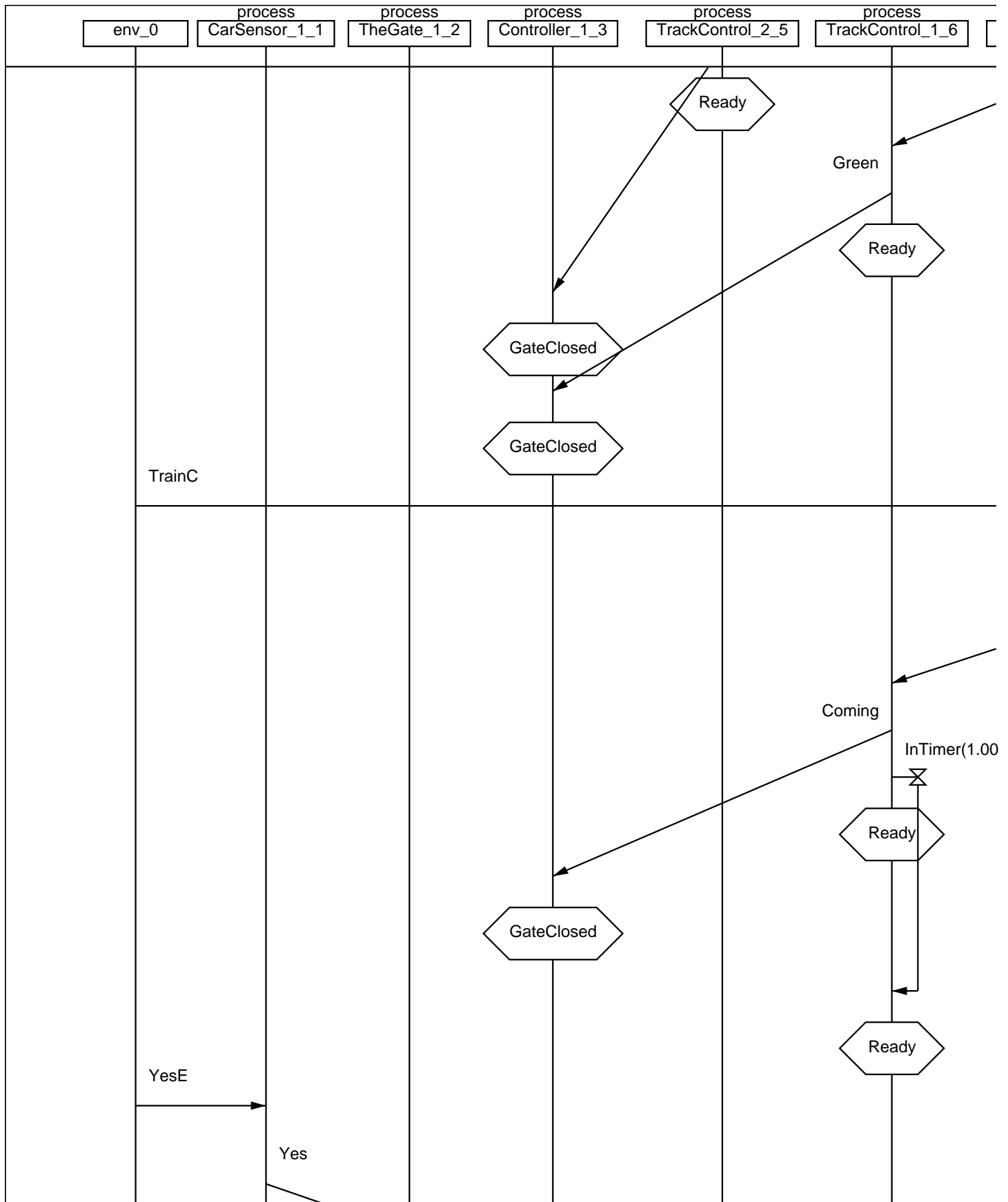
--	--	--	--	--

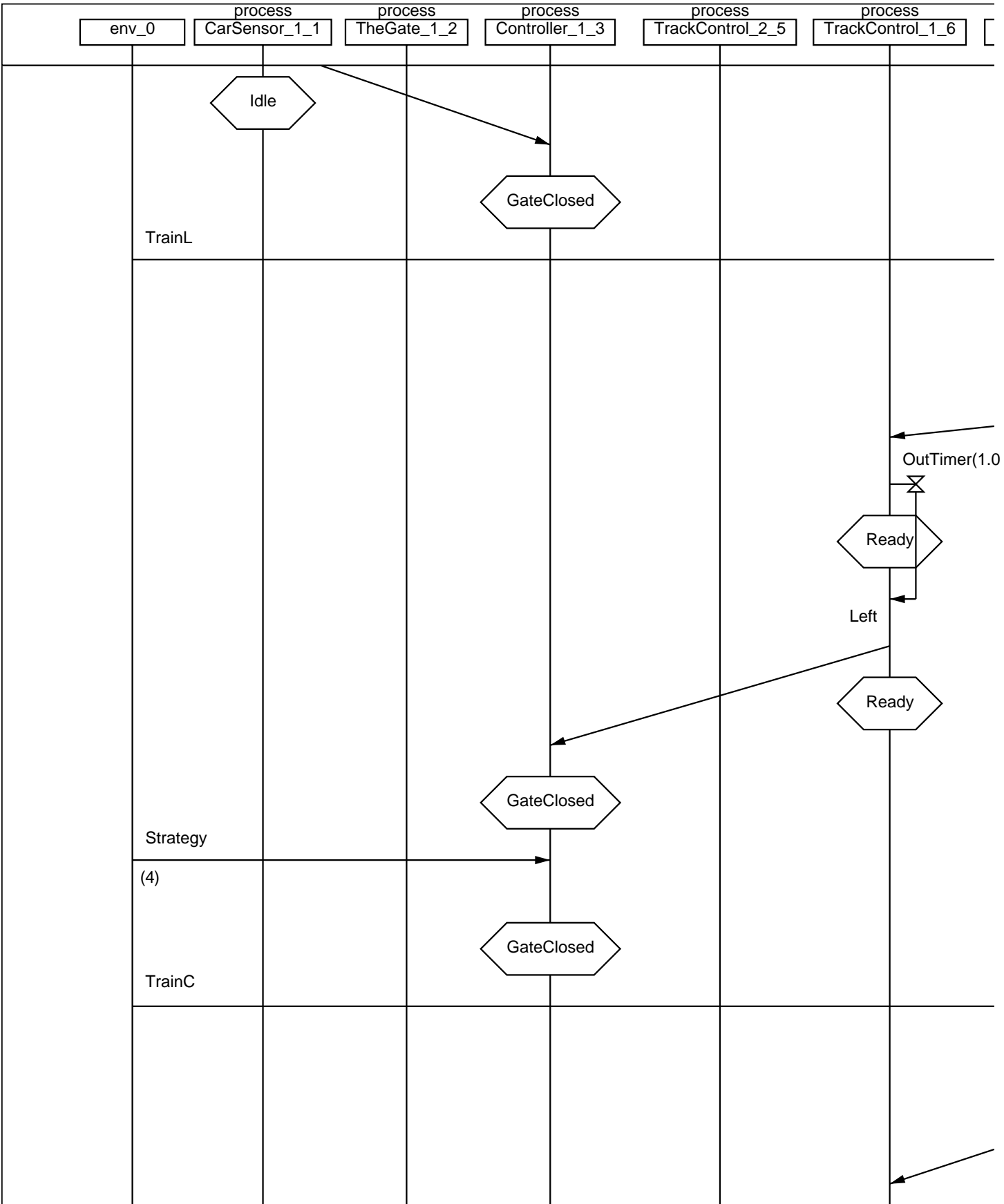
MSC CompleteMSC_TestCaseC

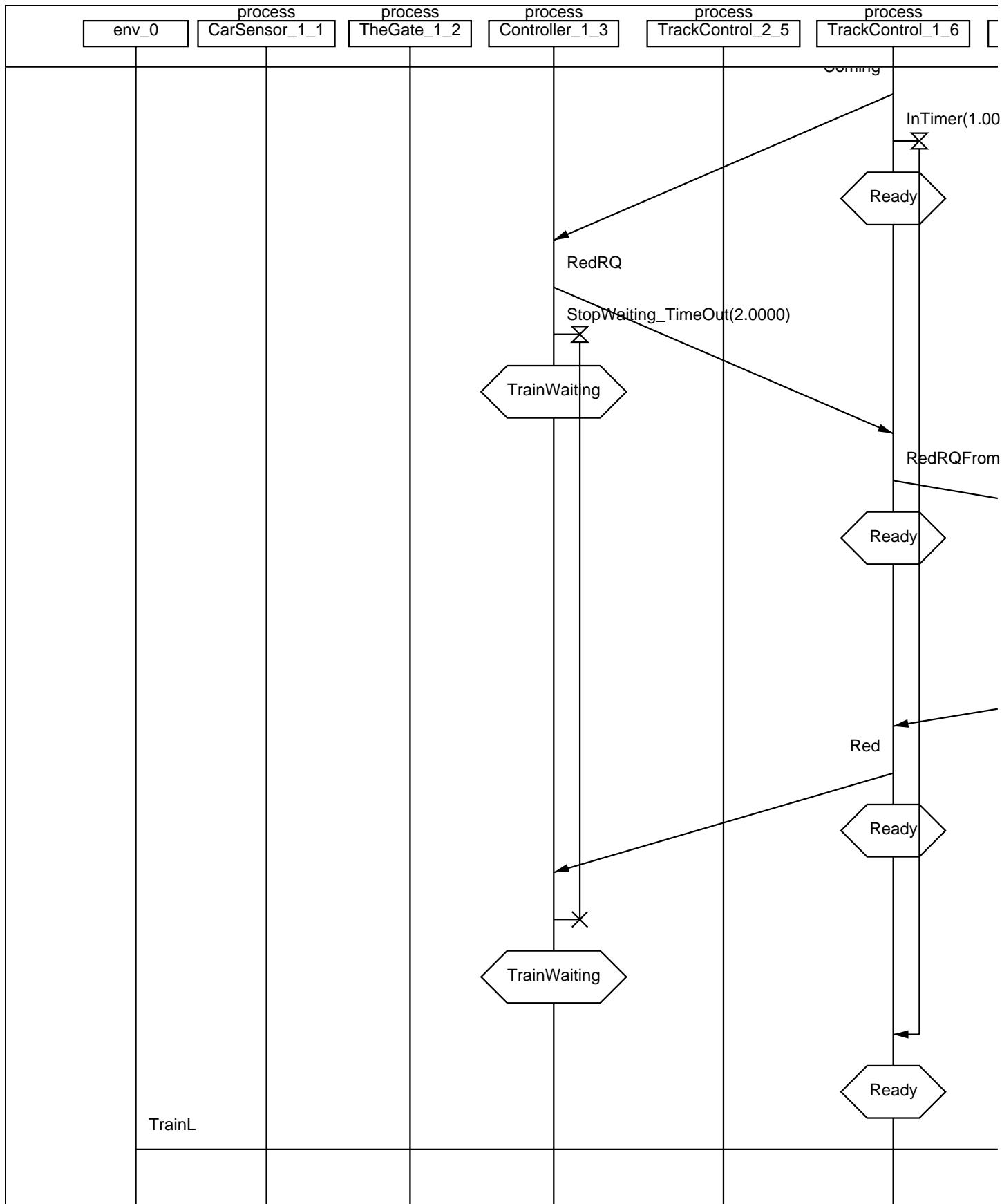
Simulation trace
generated by
SDL Simulator 4.3

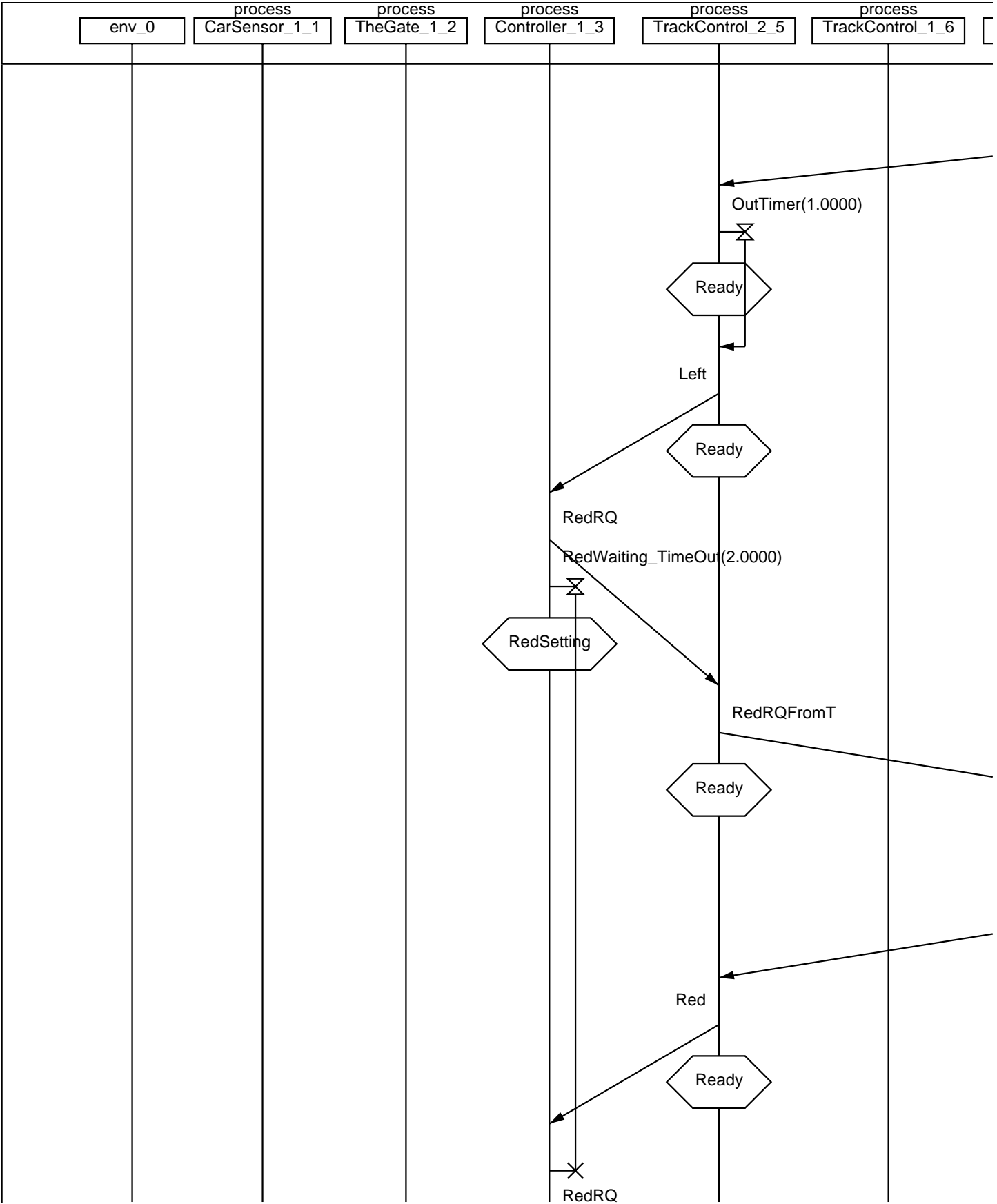


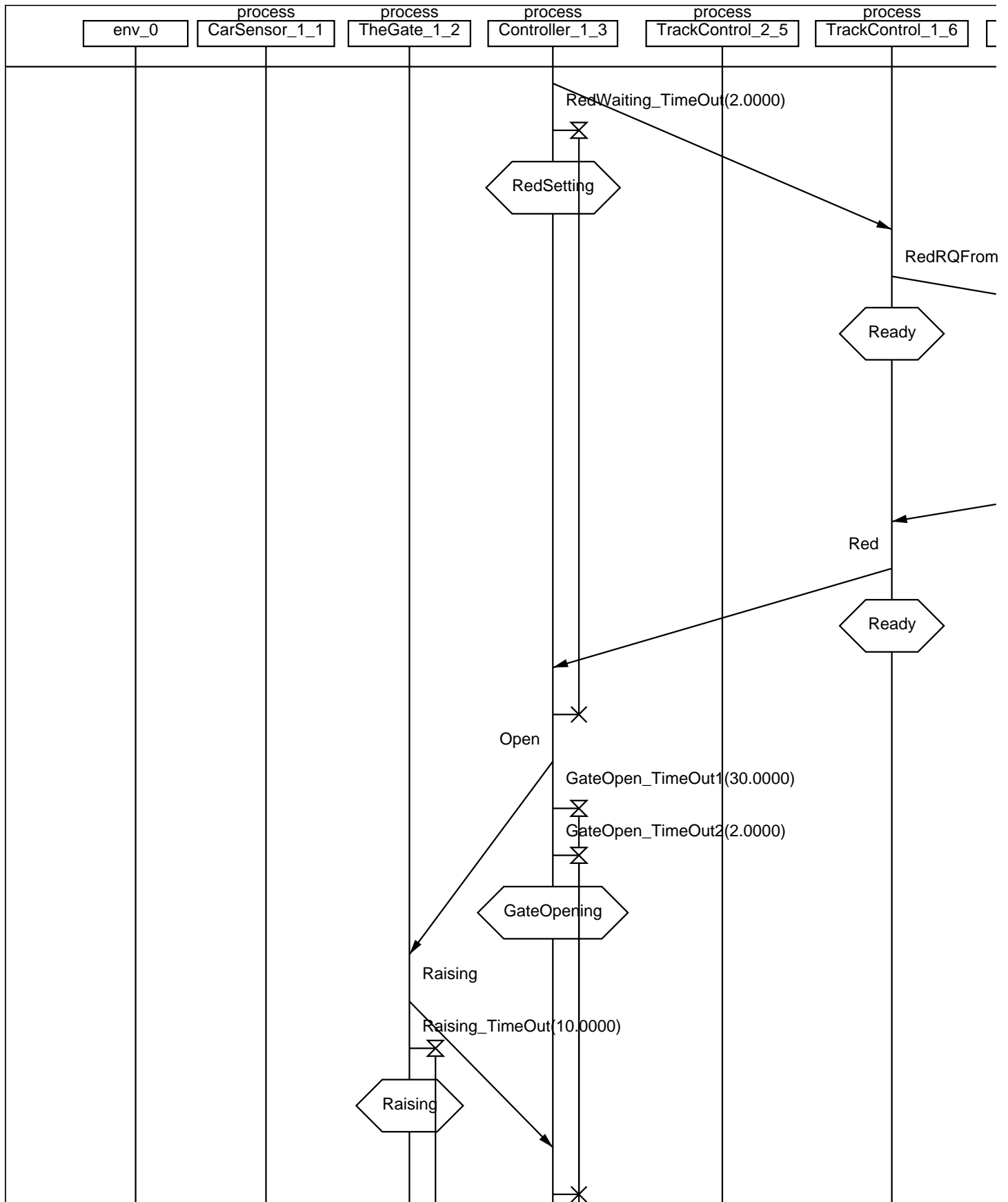


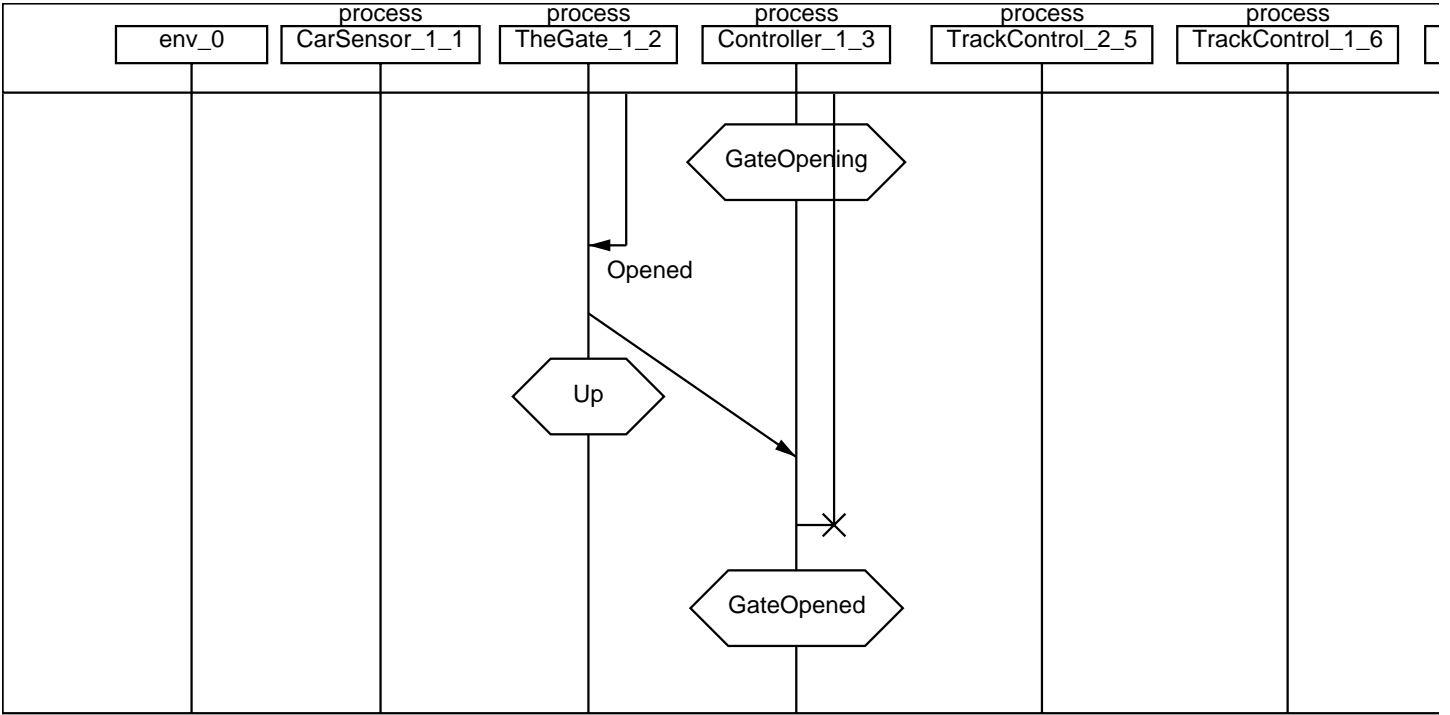


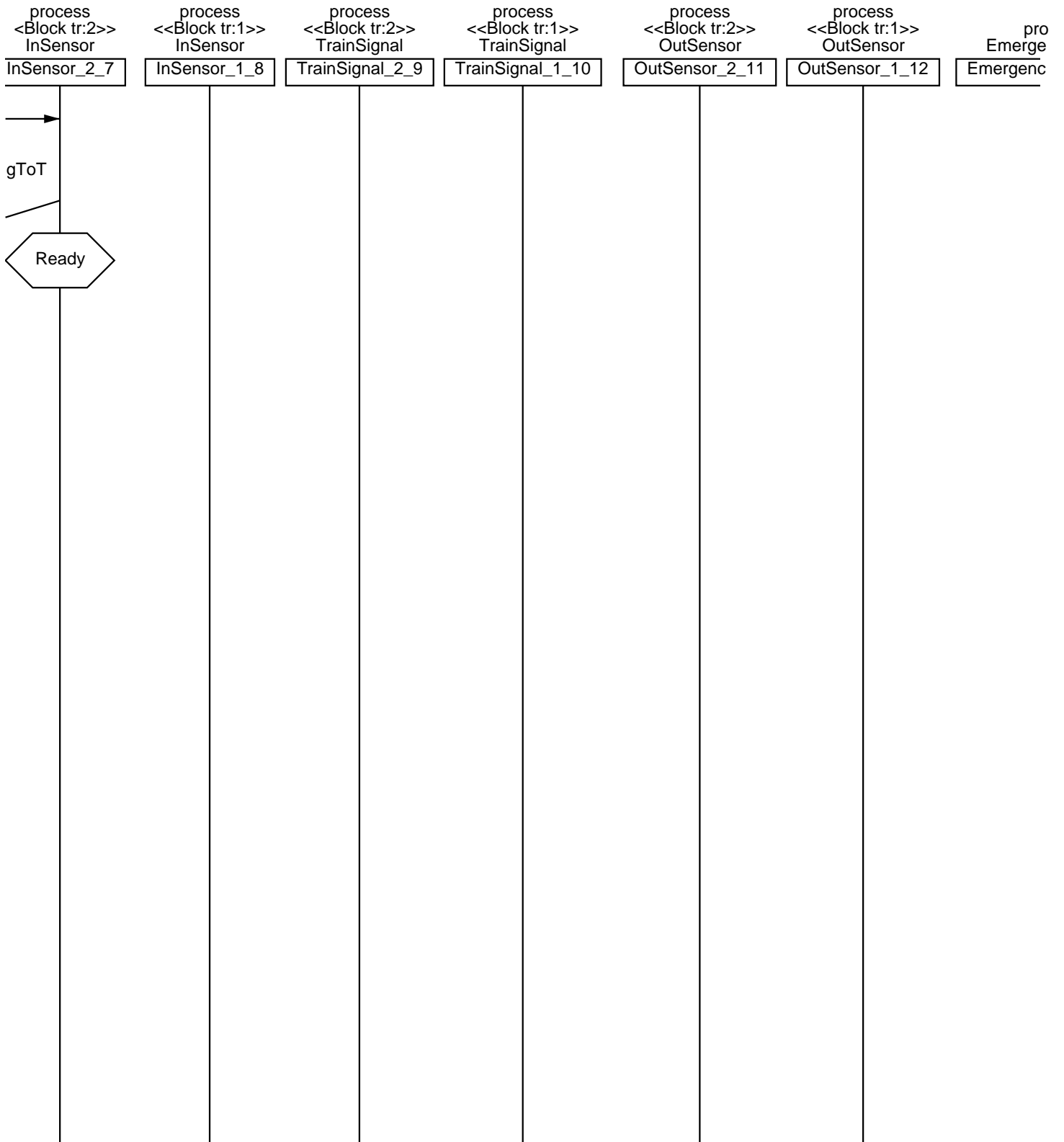




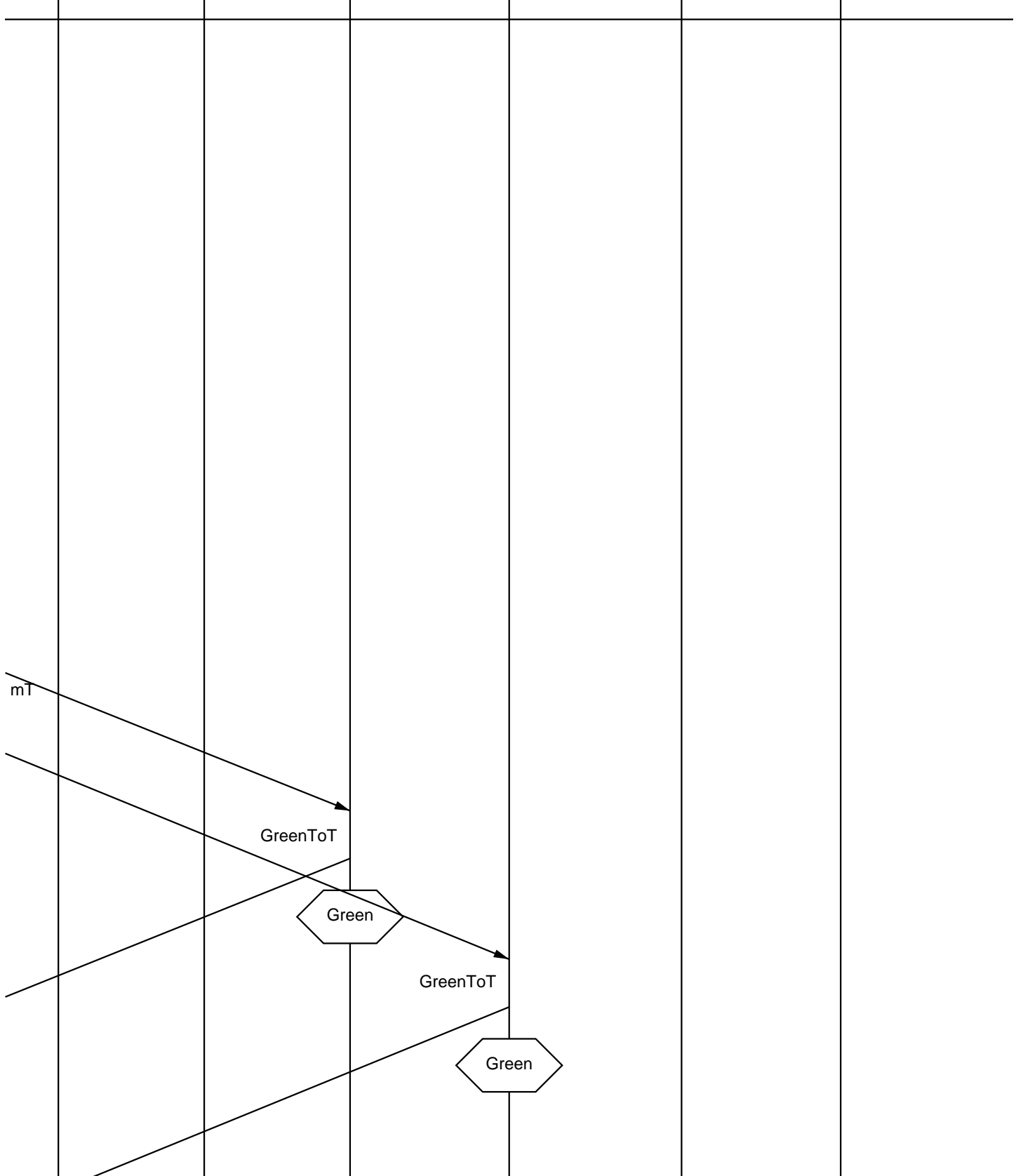


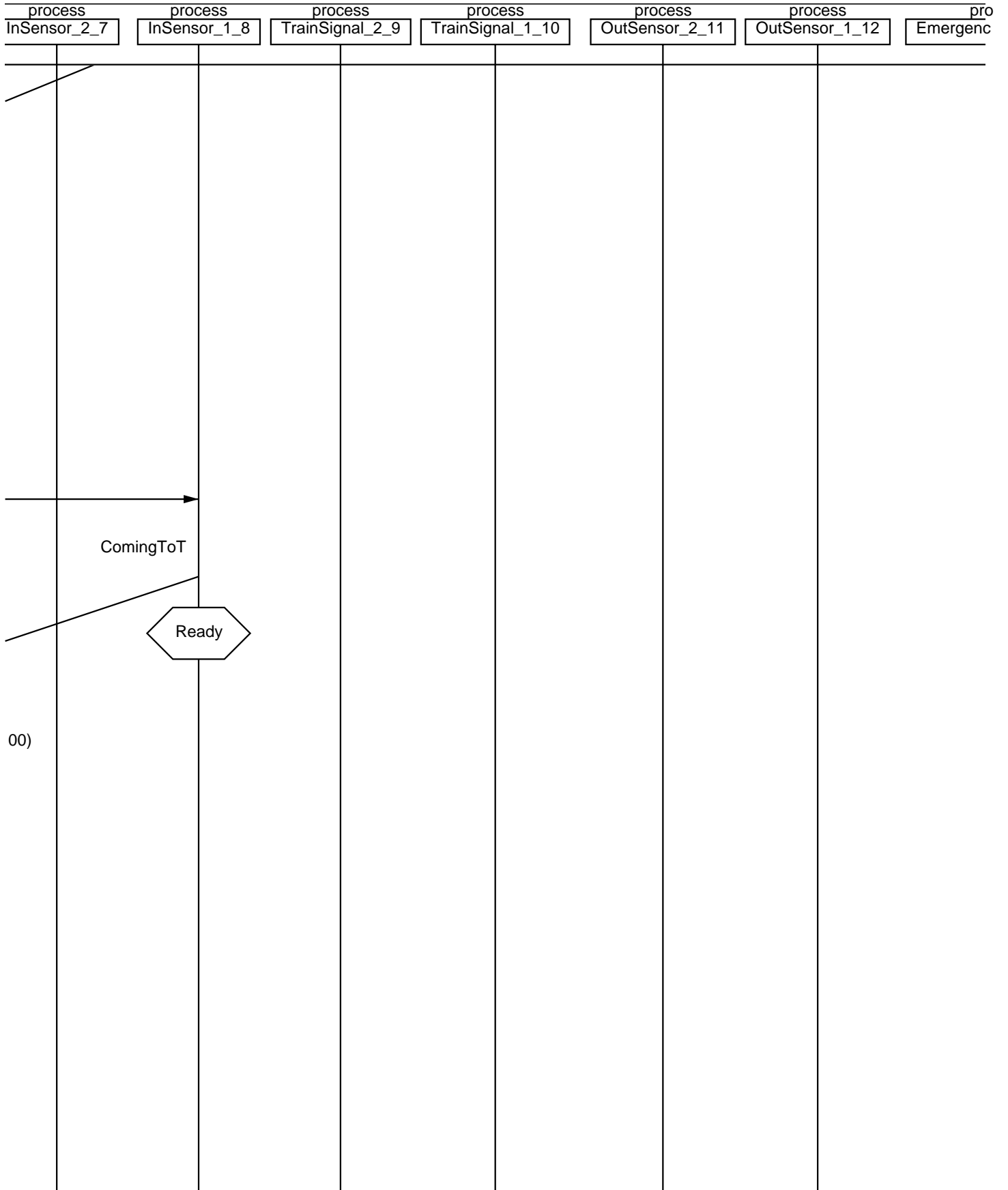


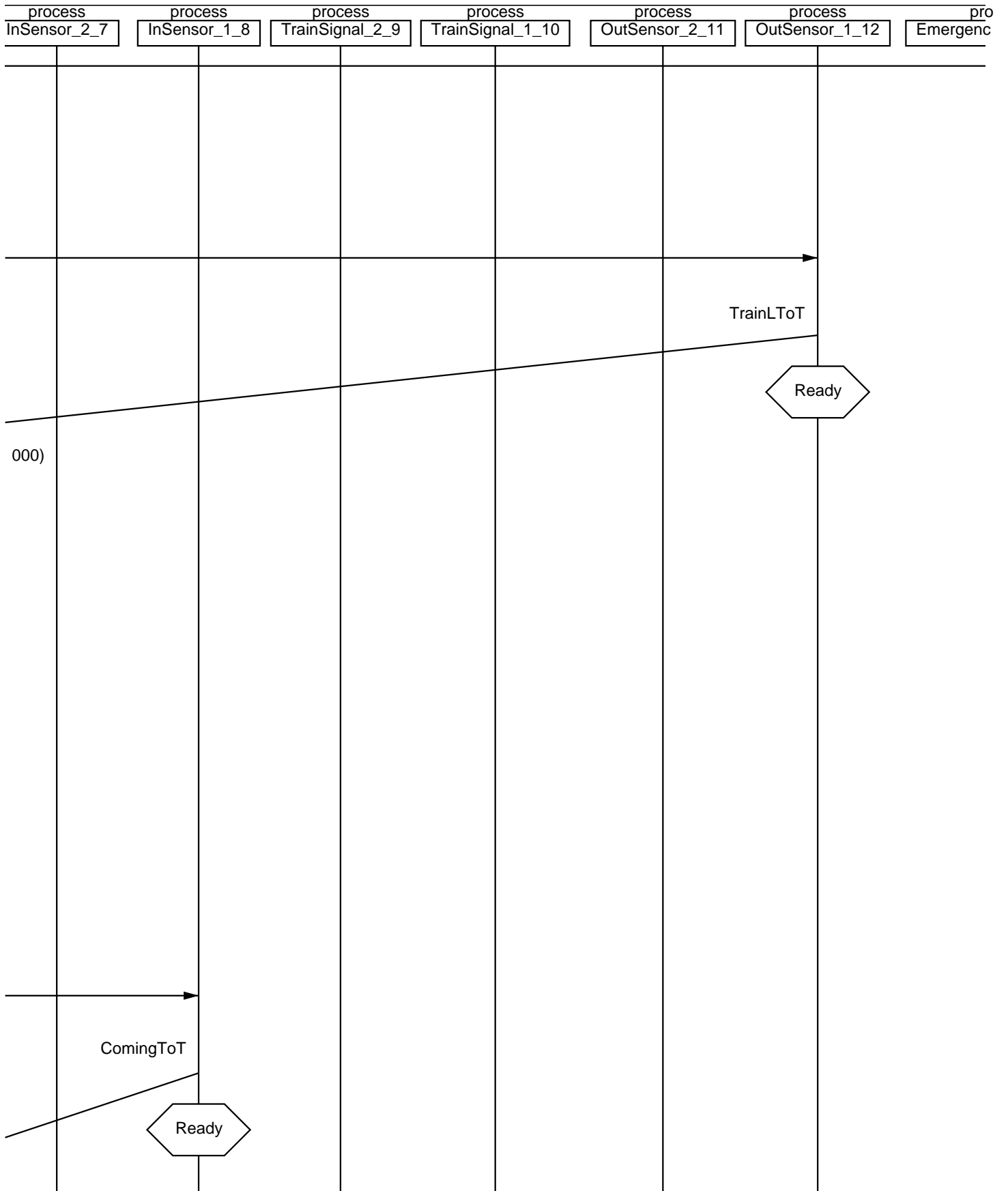


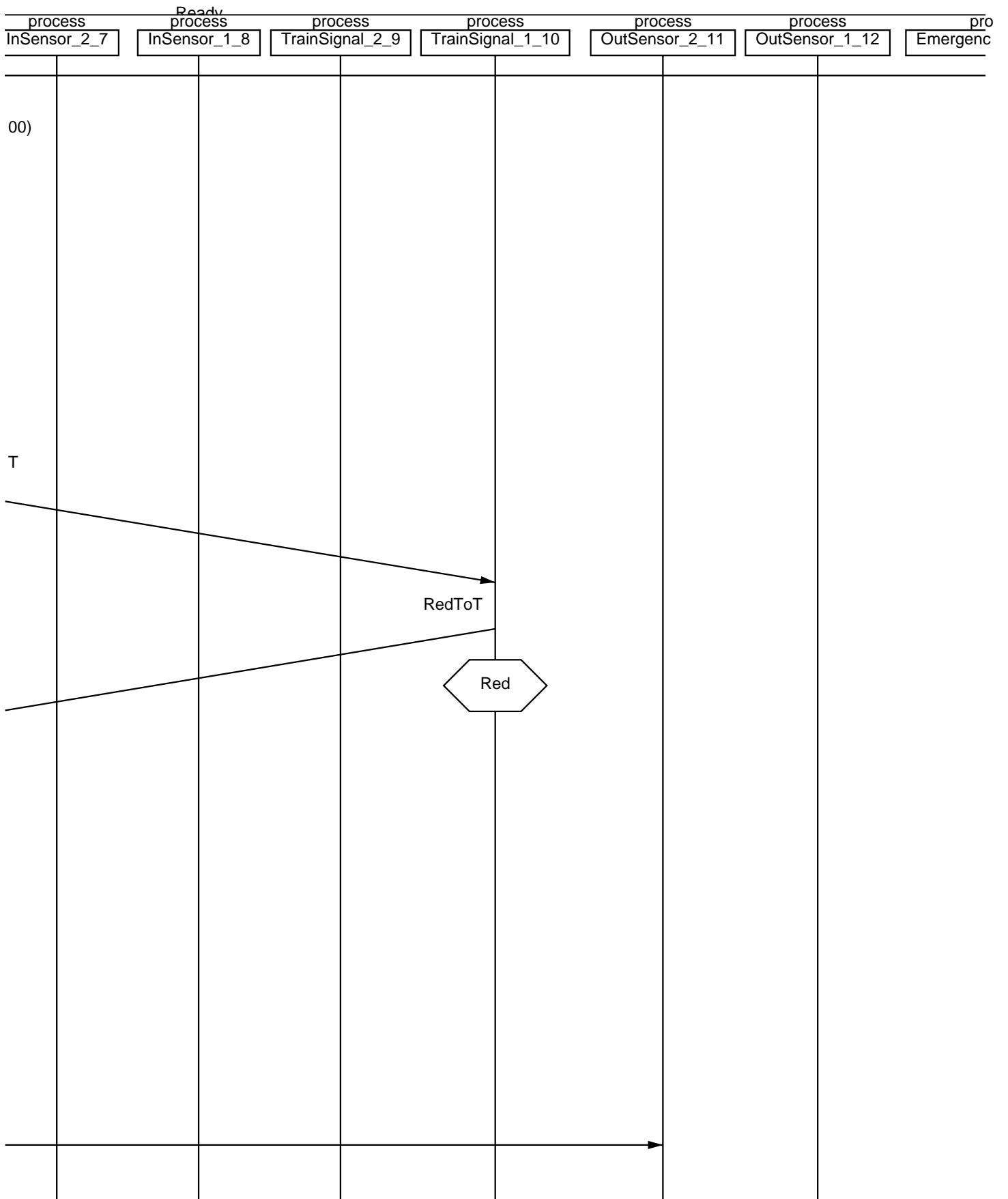


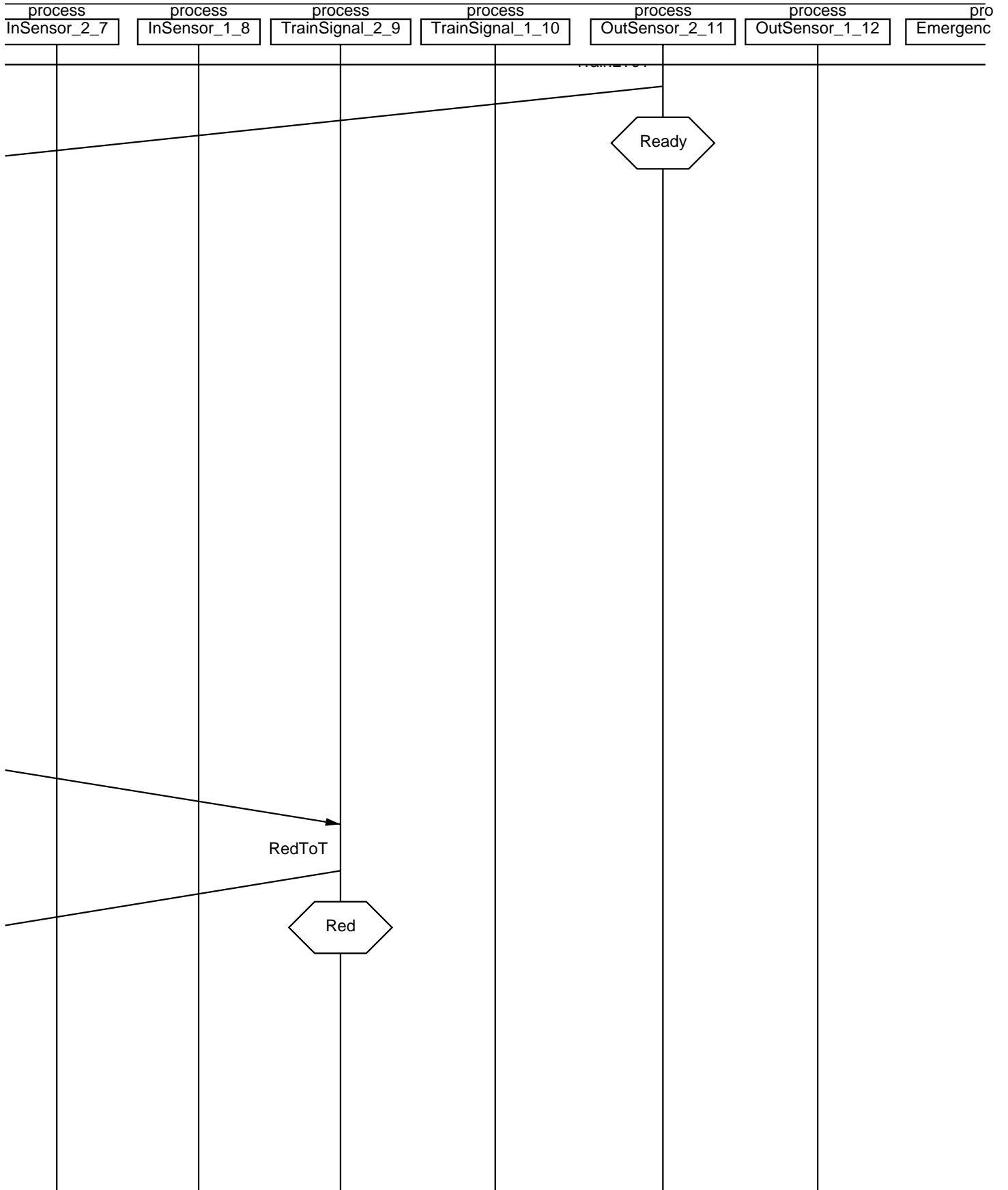
process process process process process process process
InSensor_2_7 InSensor_1_8 TrainSignal_2_9 TrainSignal_1_10 OutSensor_2_11 OutSensor_1_12 Emergenc

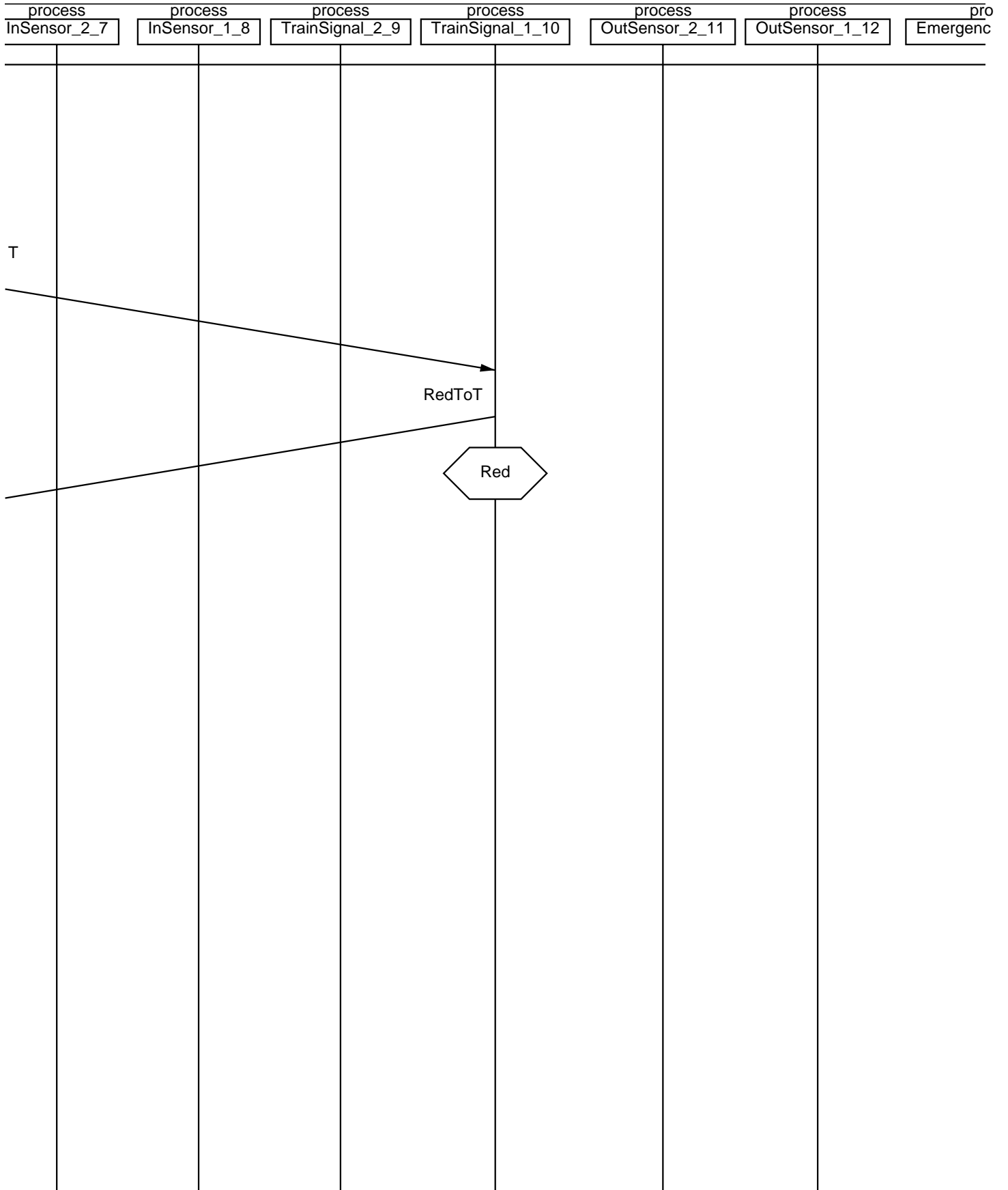












process InSensor_2_7	process InSensor_1_8	process TrainSignal_2_9	process TrainSignal_1_10	process OutSensor_2_11	process OutSensor_1_12	pro Emergenc

cess
ncySignal
ySignal_1_4

cess
ySignal_1_4

cess
ySignal_1_4

cess
ySignal_1_4

cess
ySignal_1_4

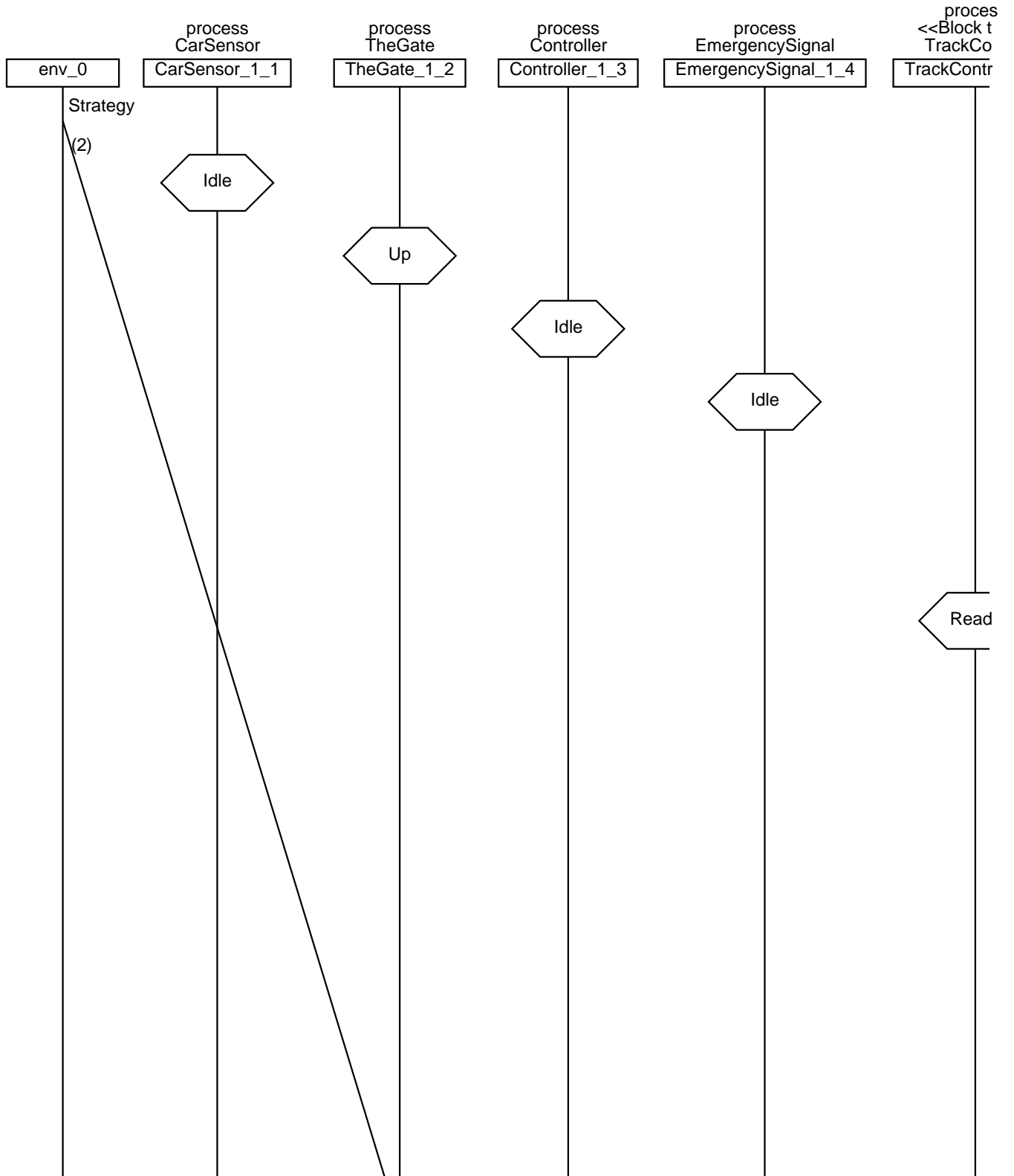
cess
ySignal_1_4

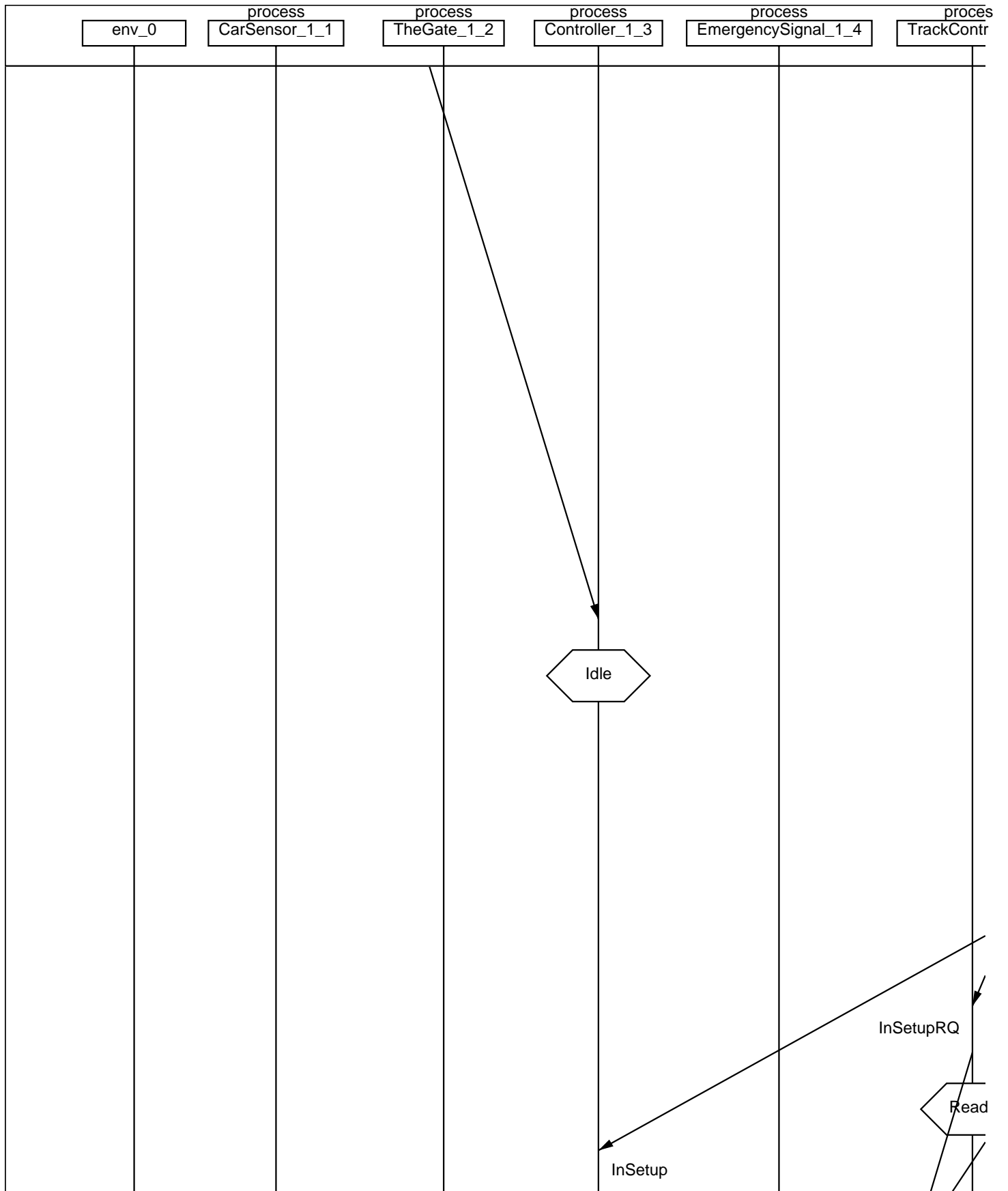
cess
ySignal_1_4

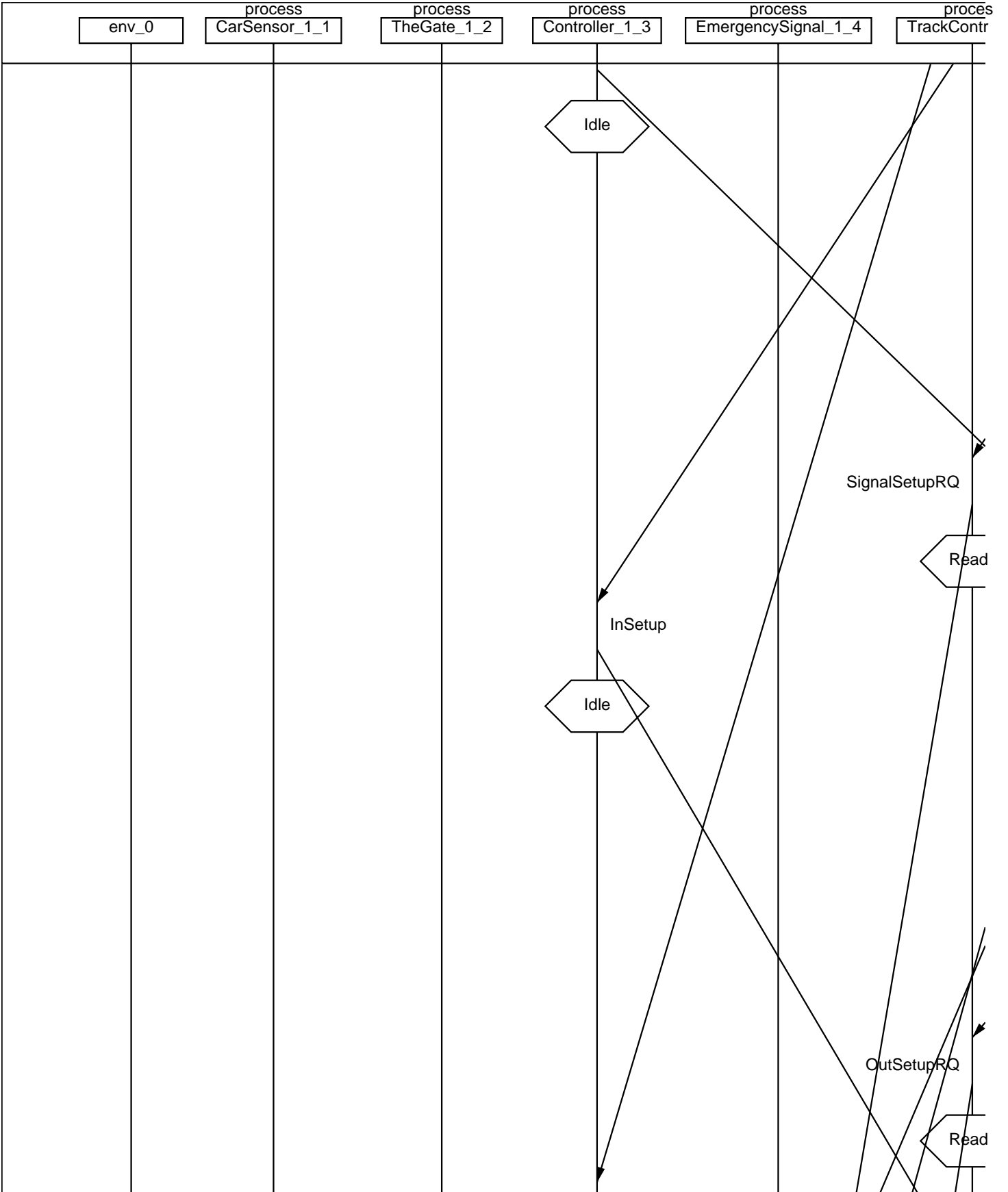
cess
ySignal_1_4

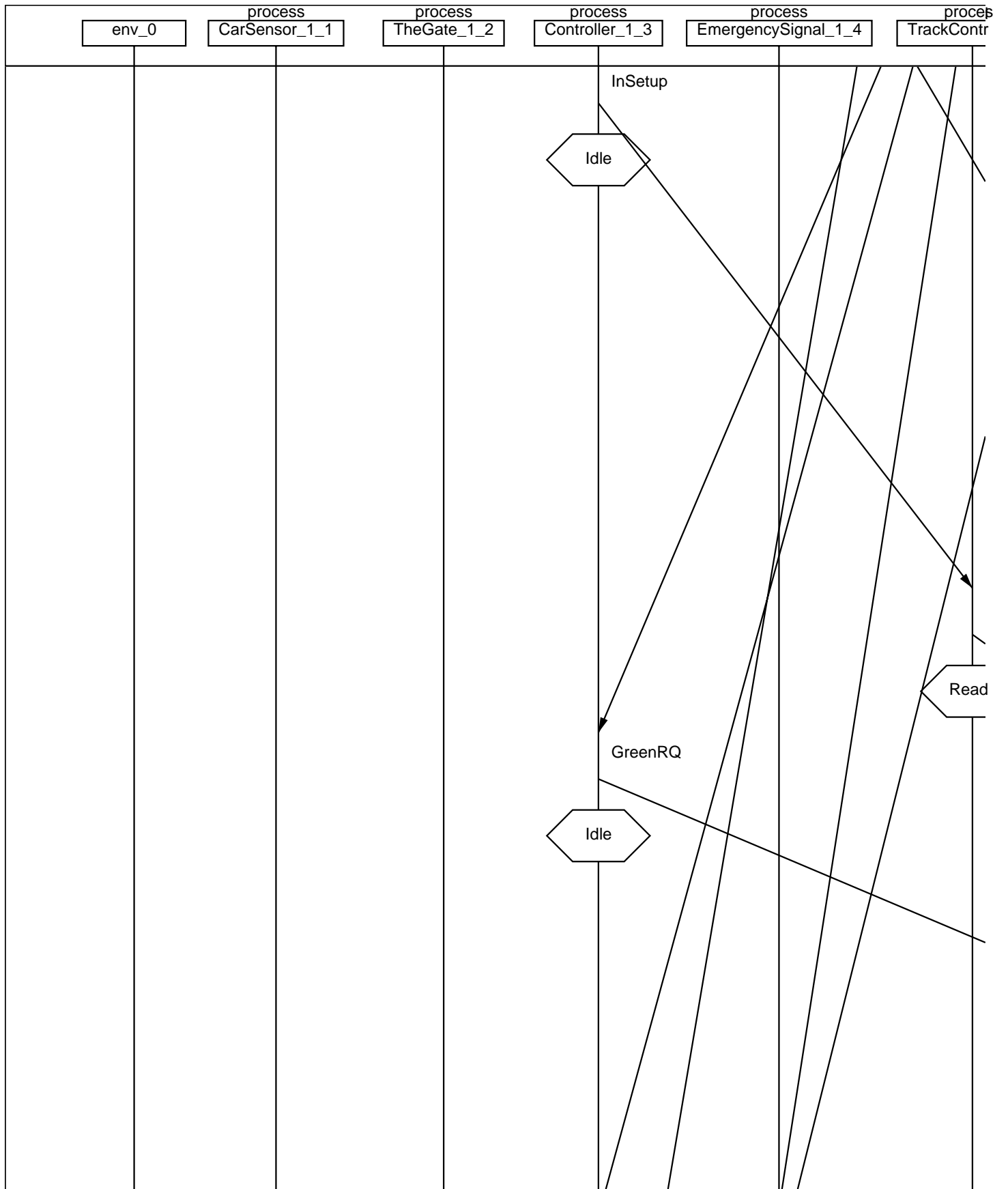
MSC CompleteMSC_TestCaseD_Strategy2

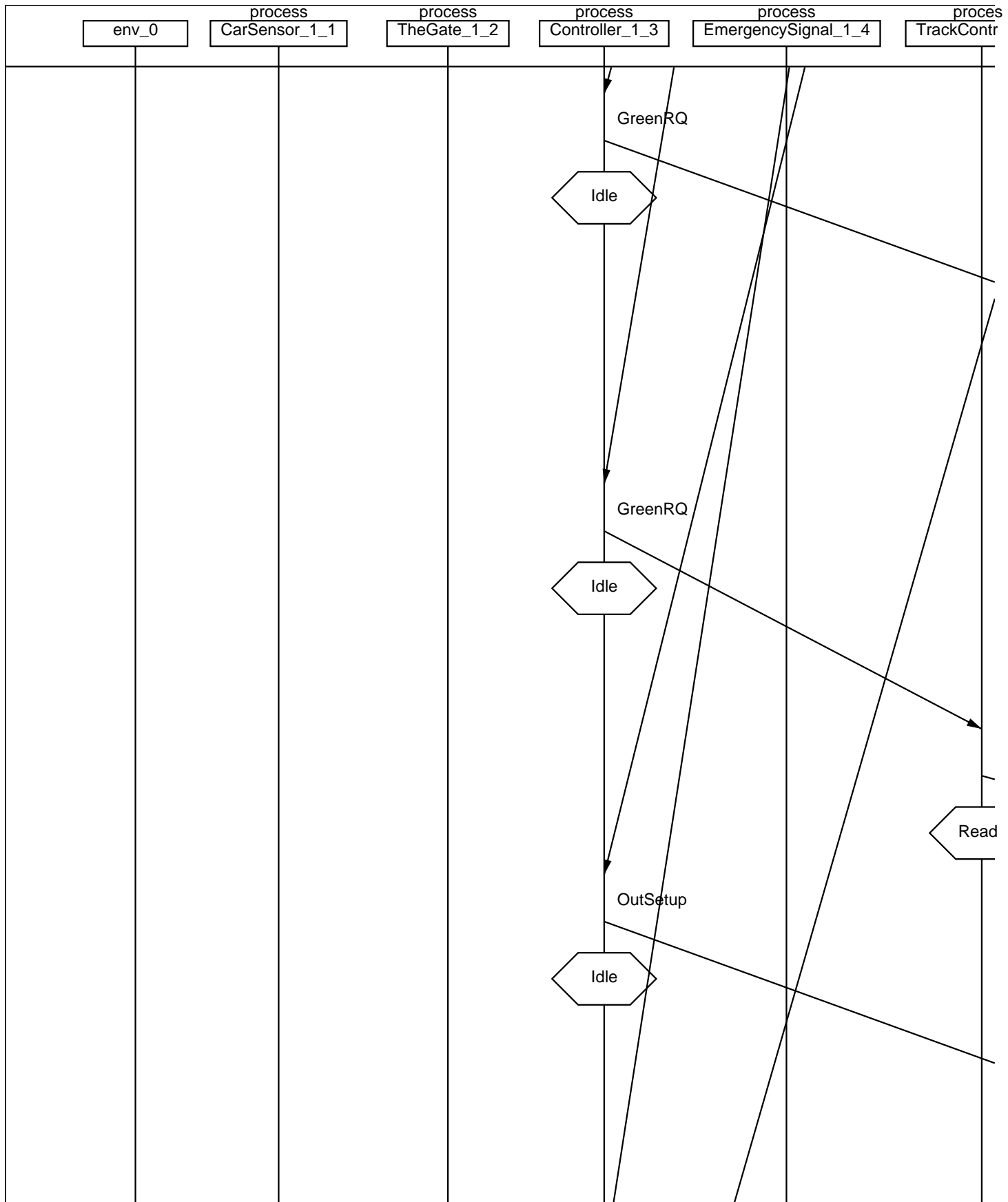
Simulation trace
generated by
SDL Simulator 4.3

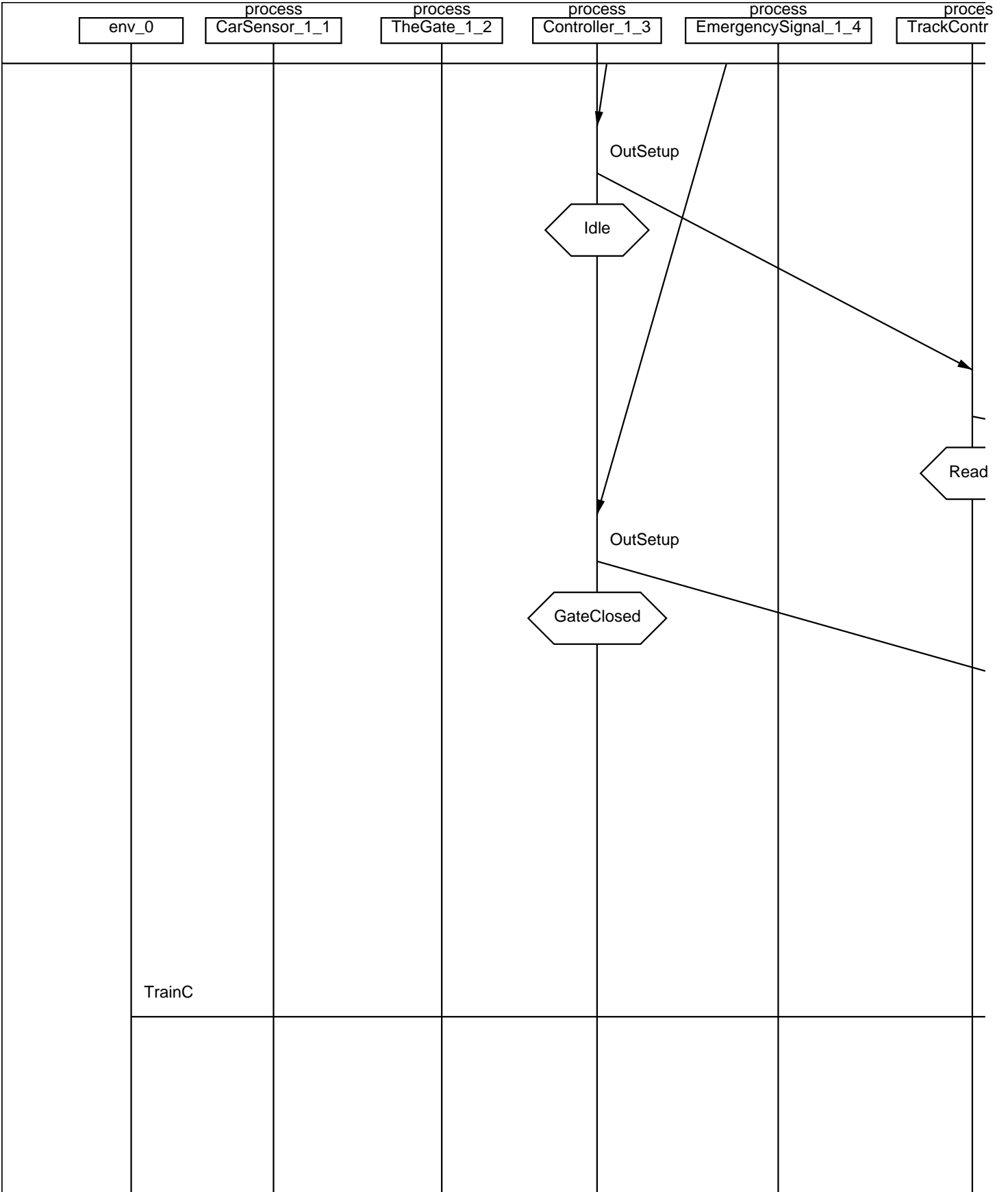


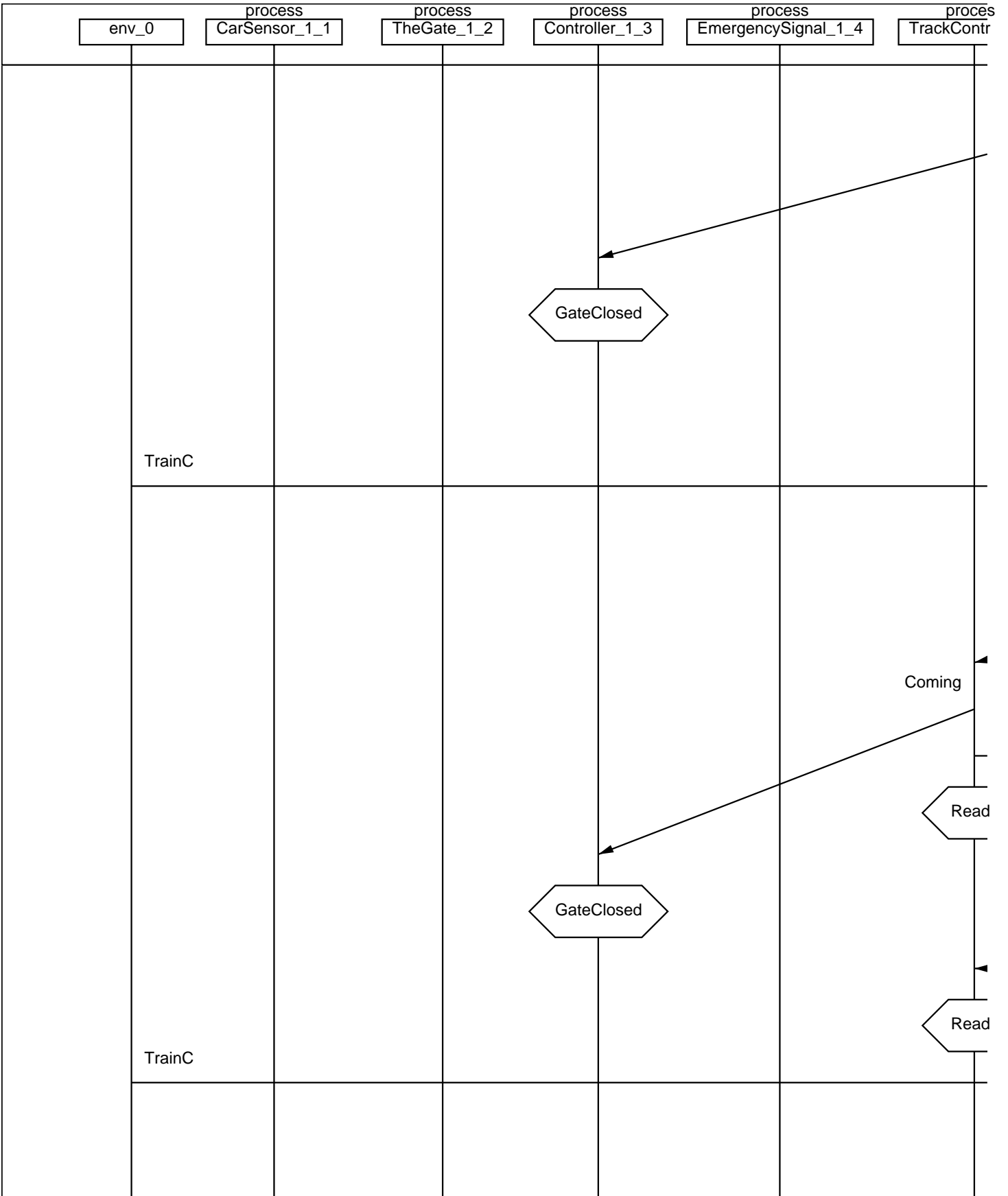


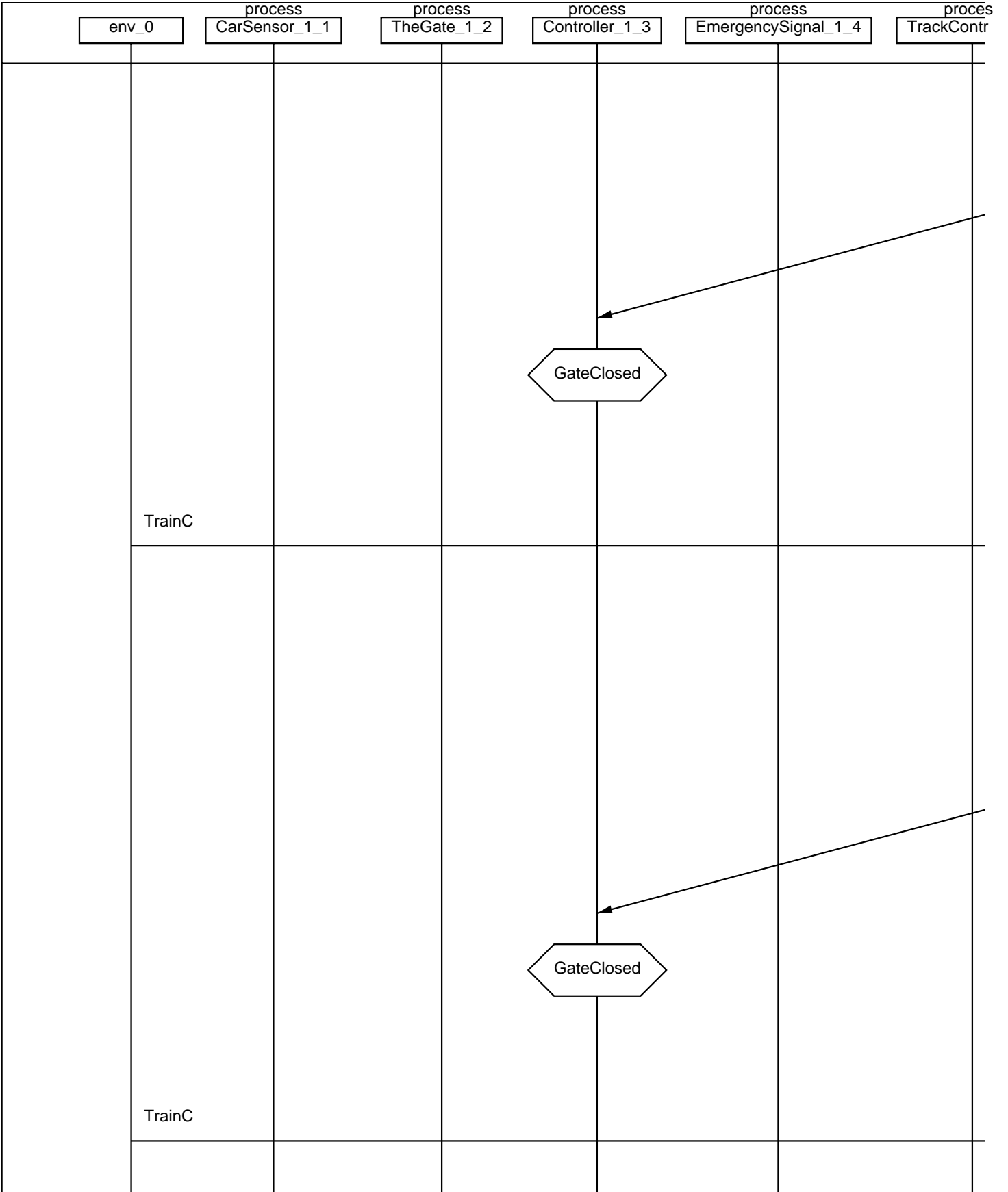


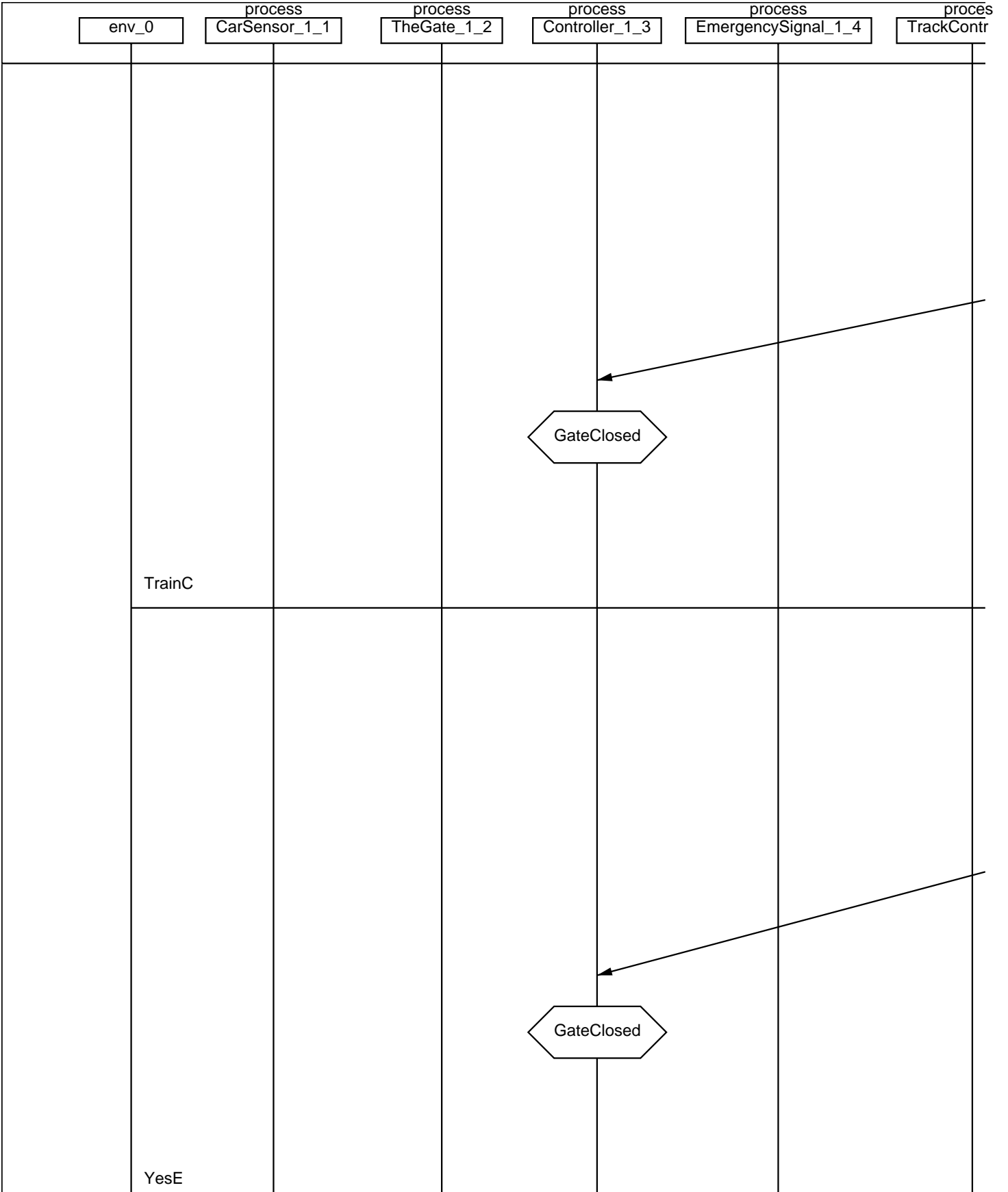


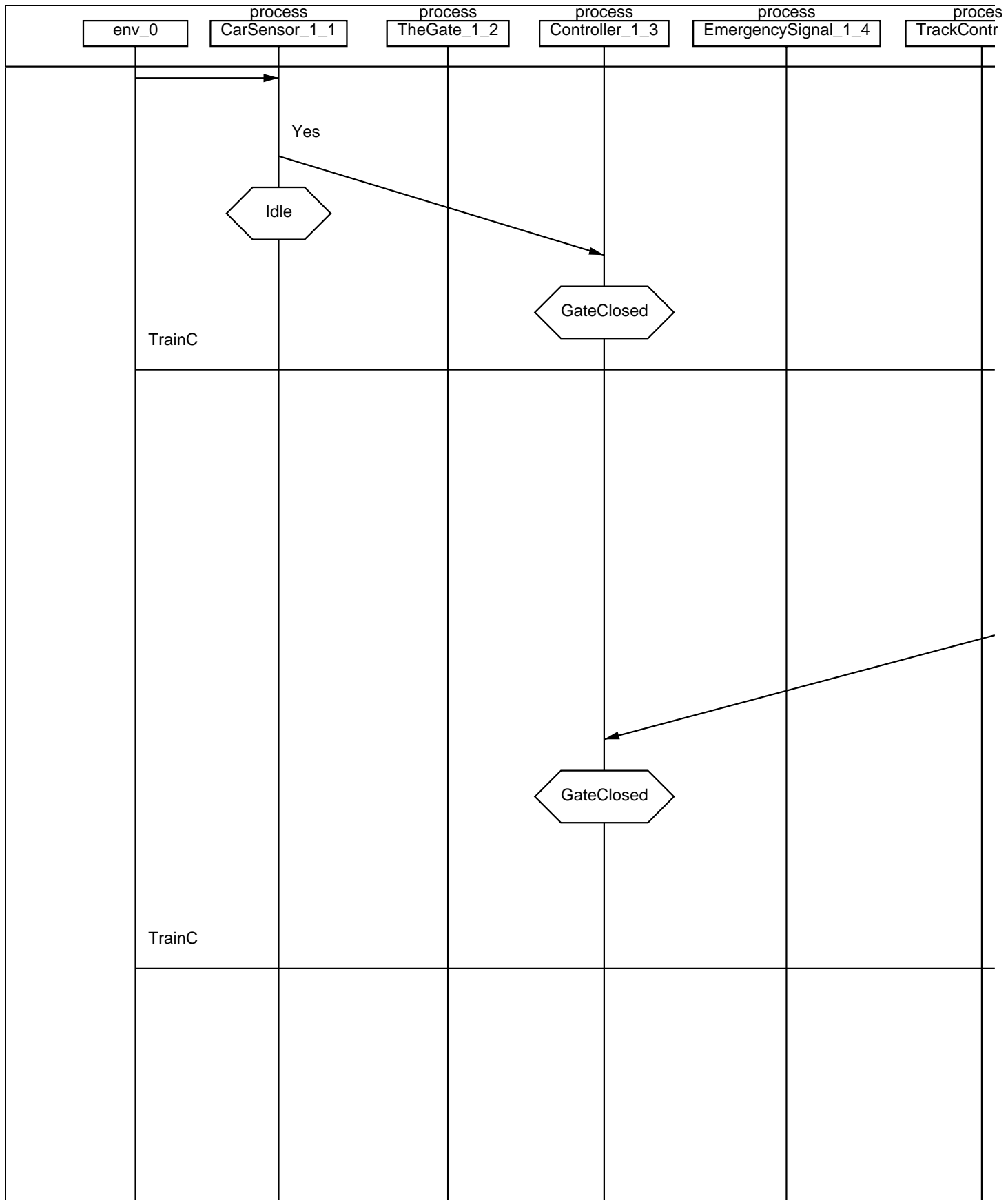


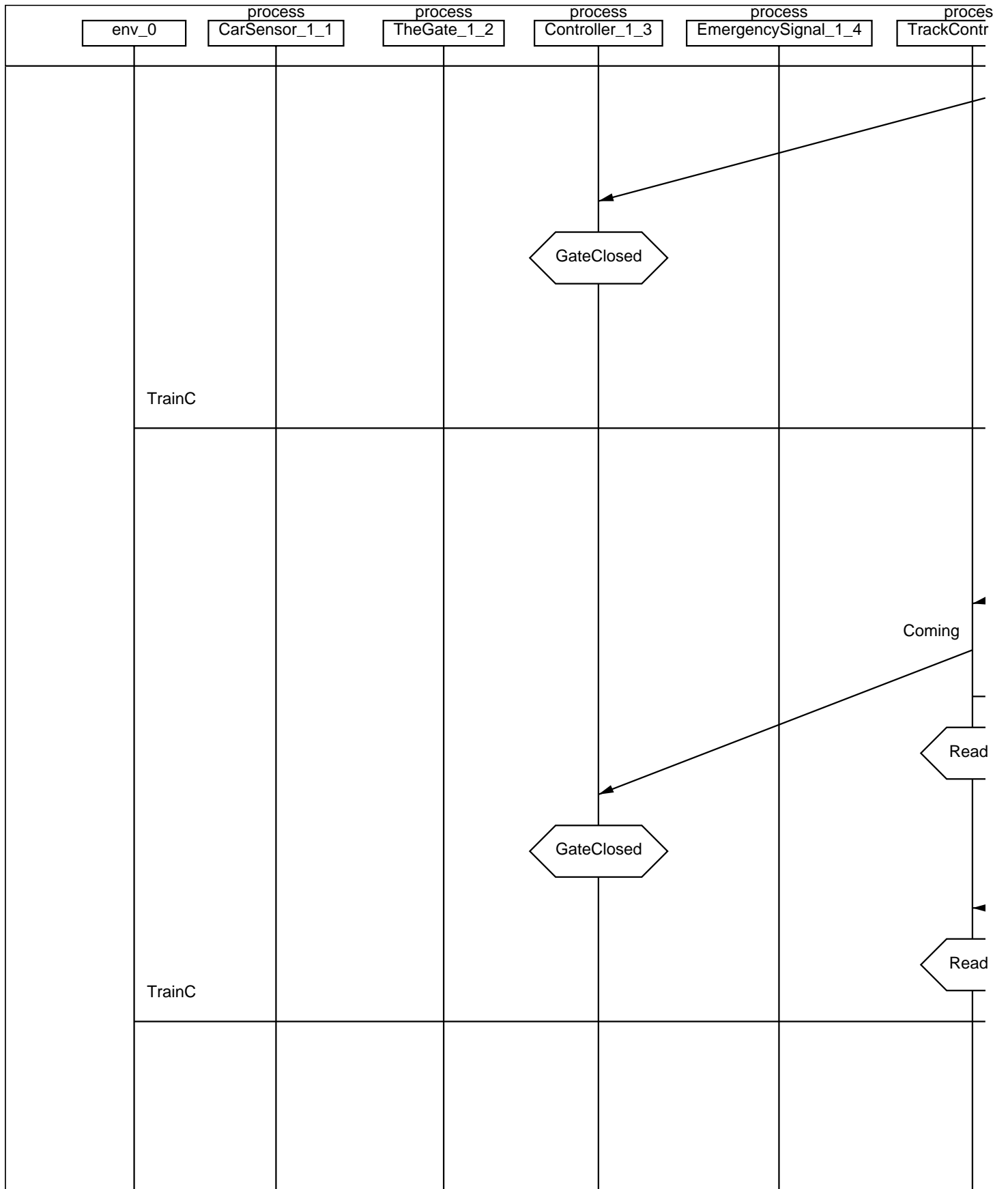


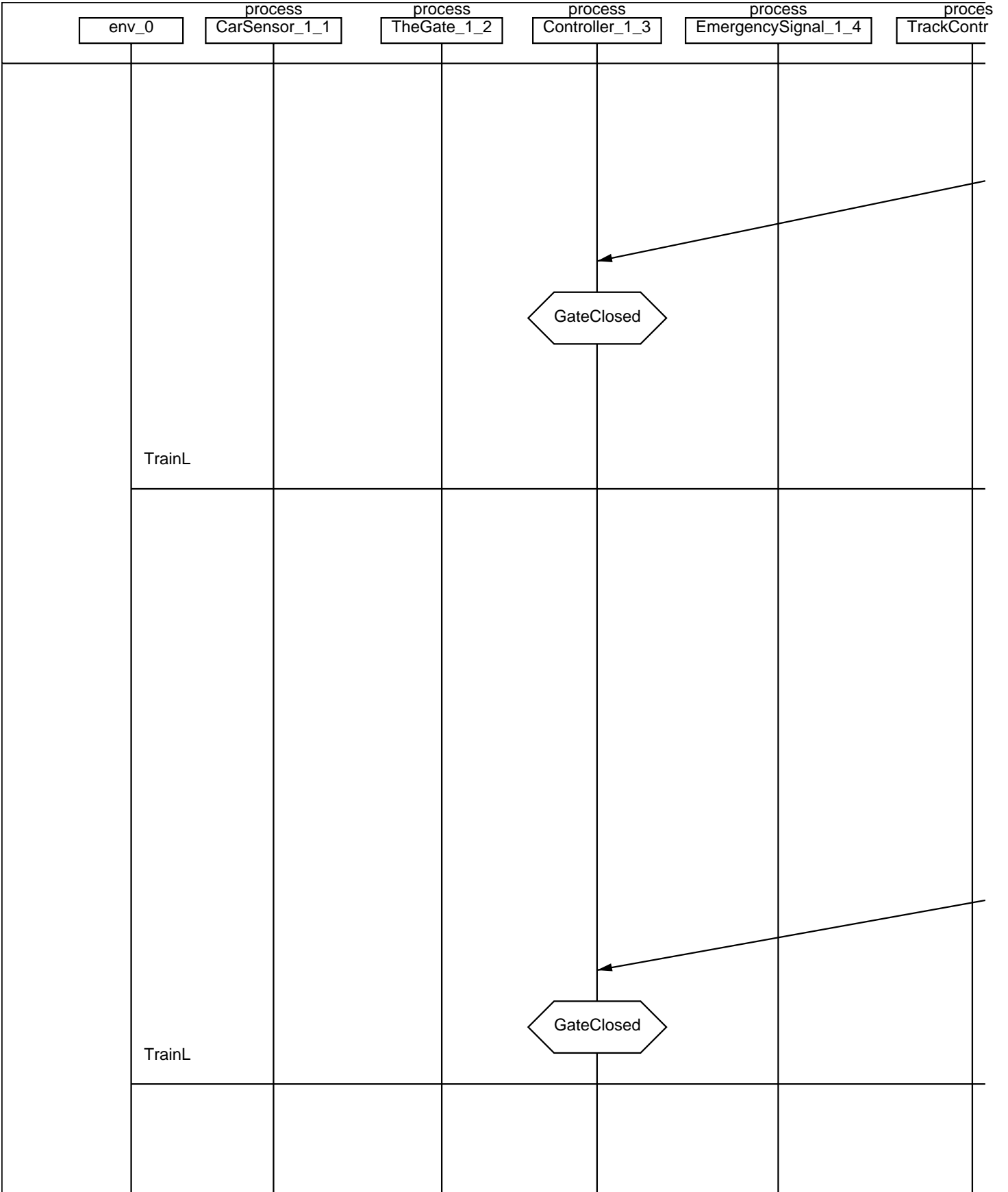


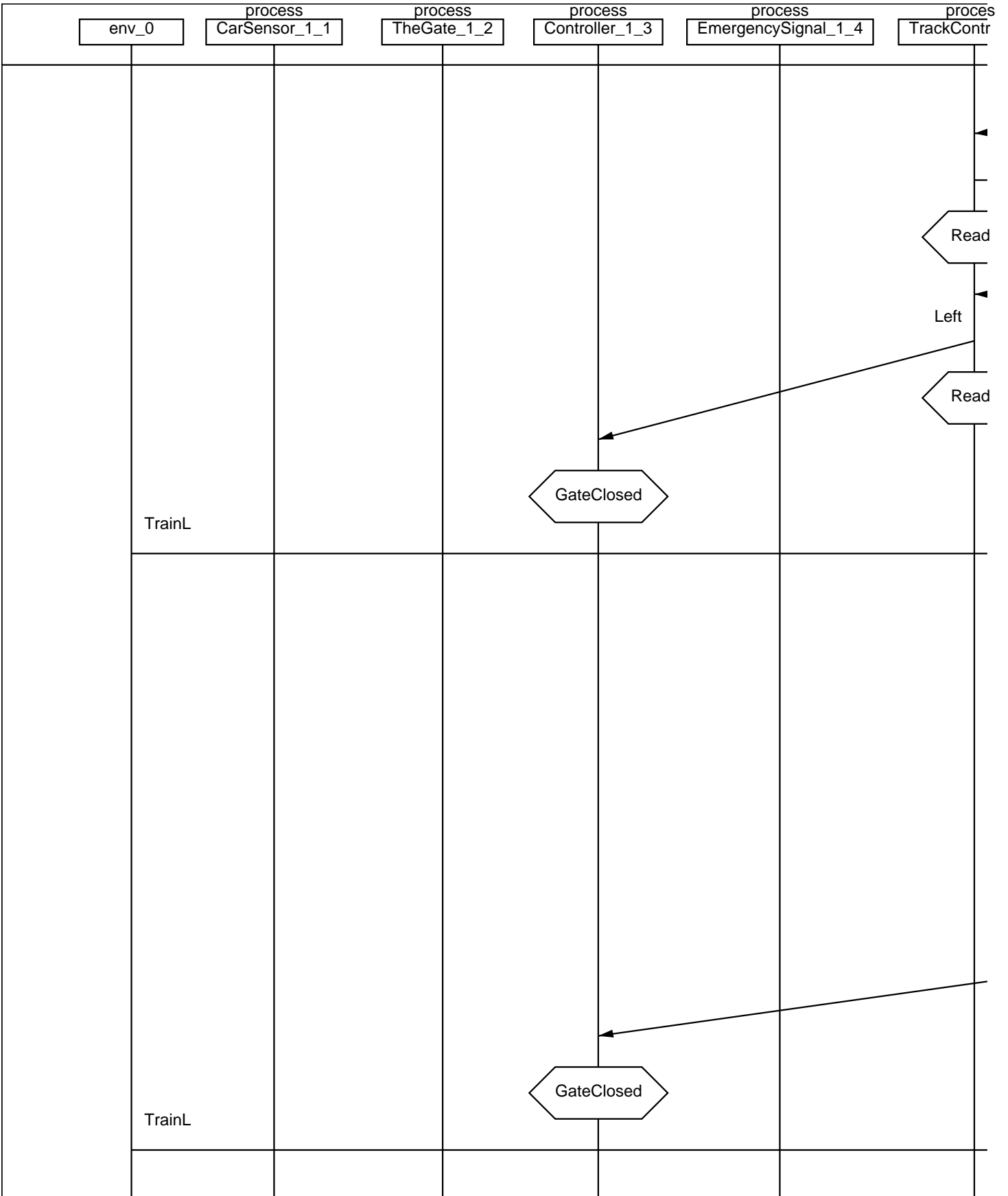


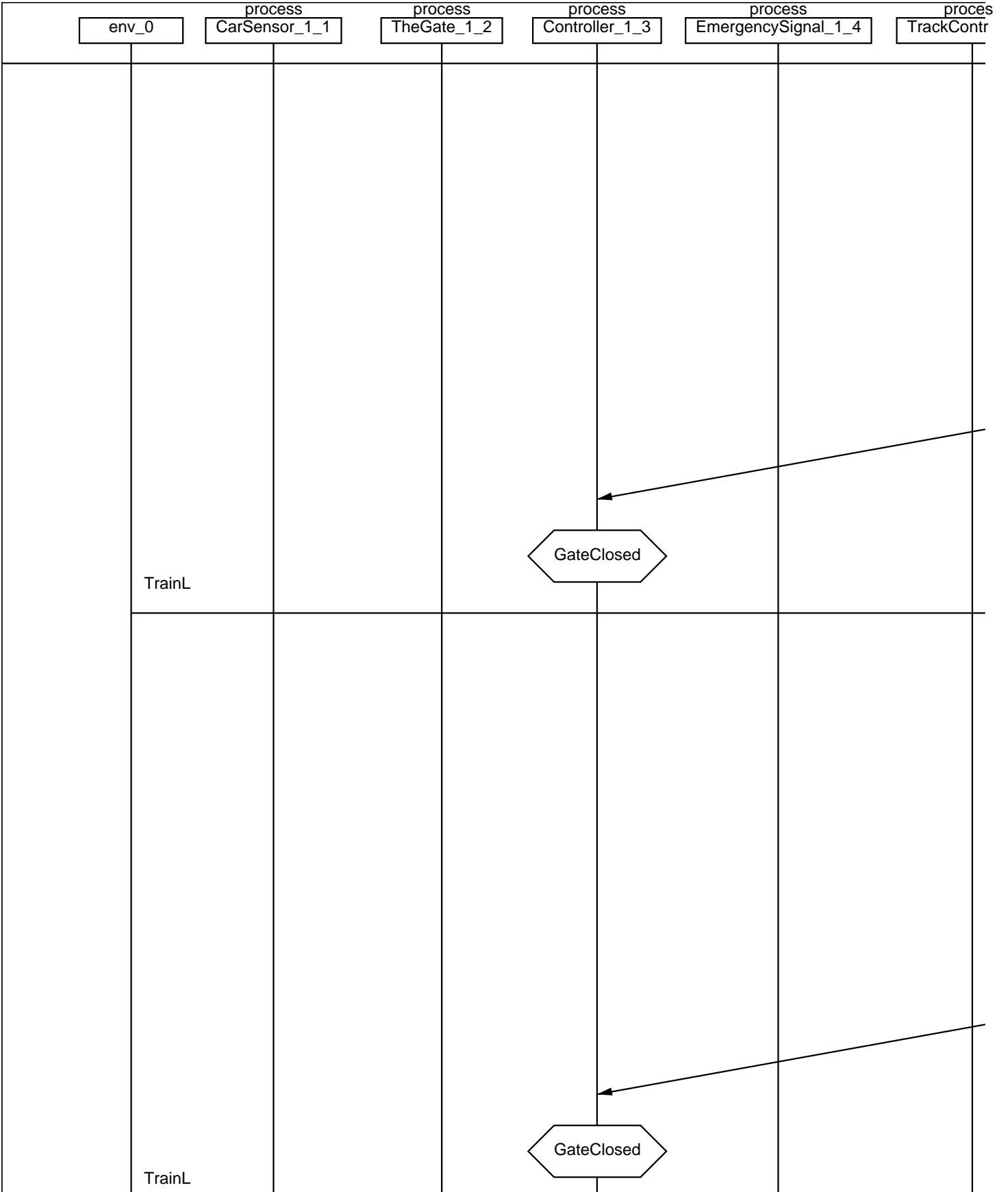


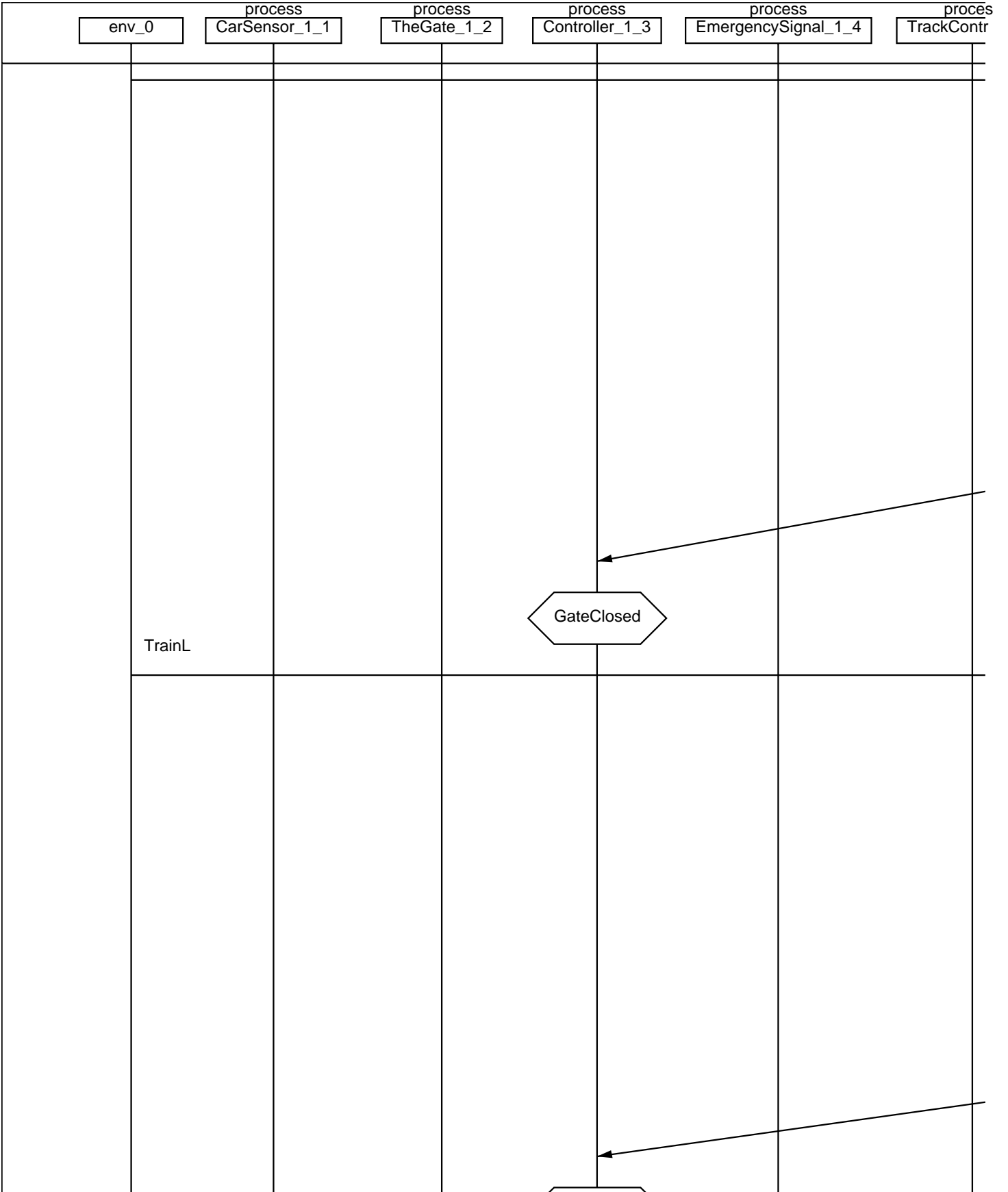


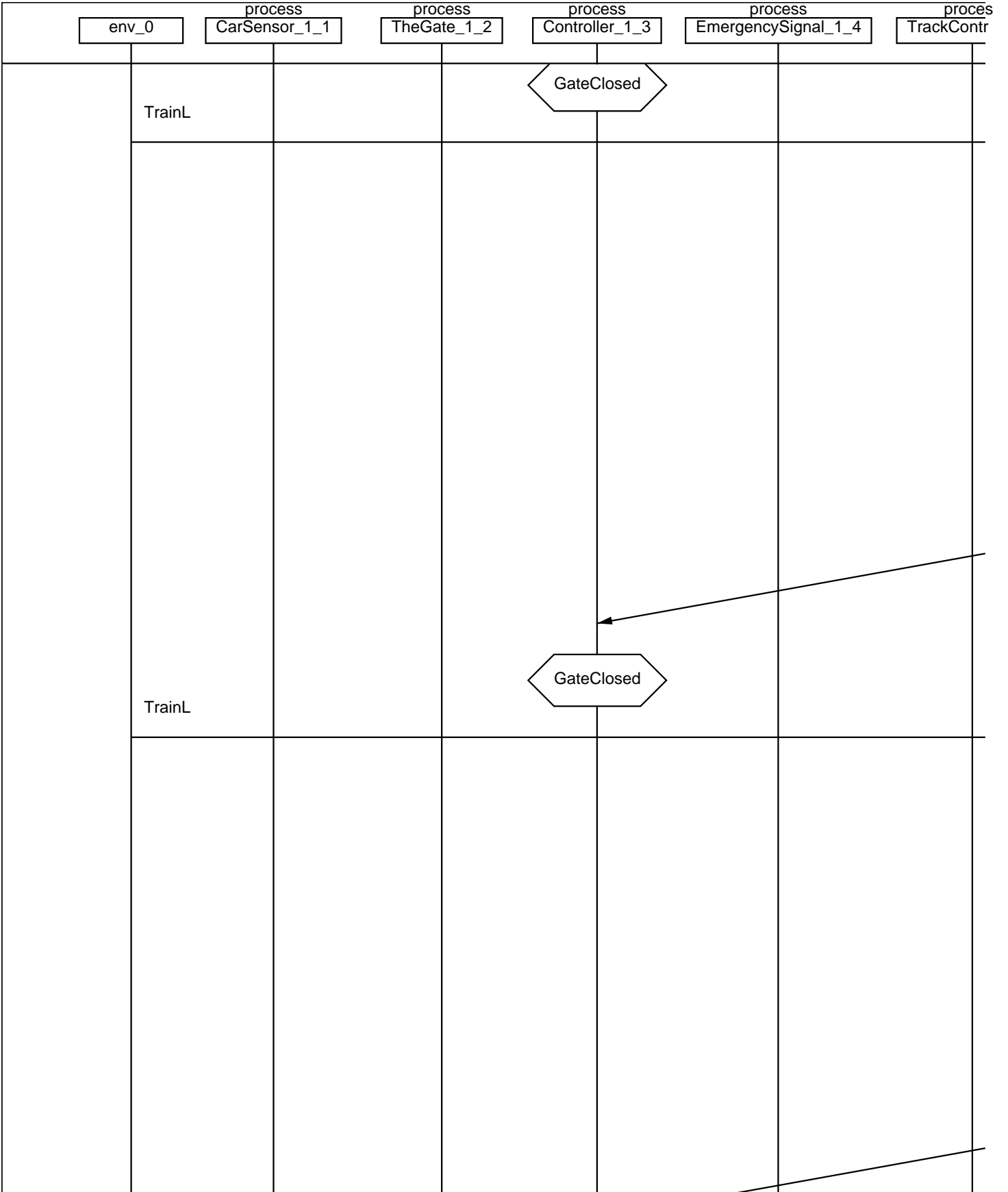


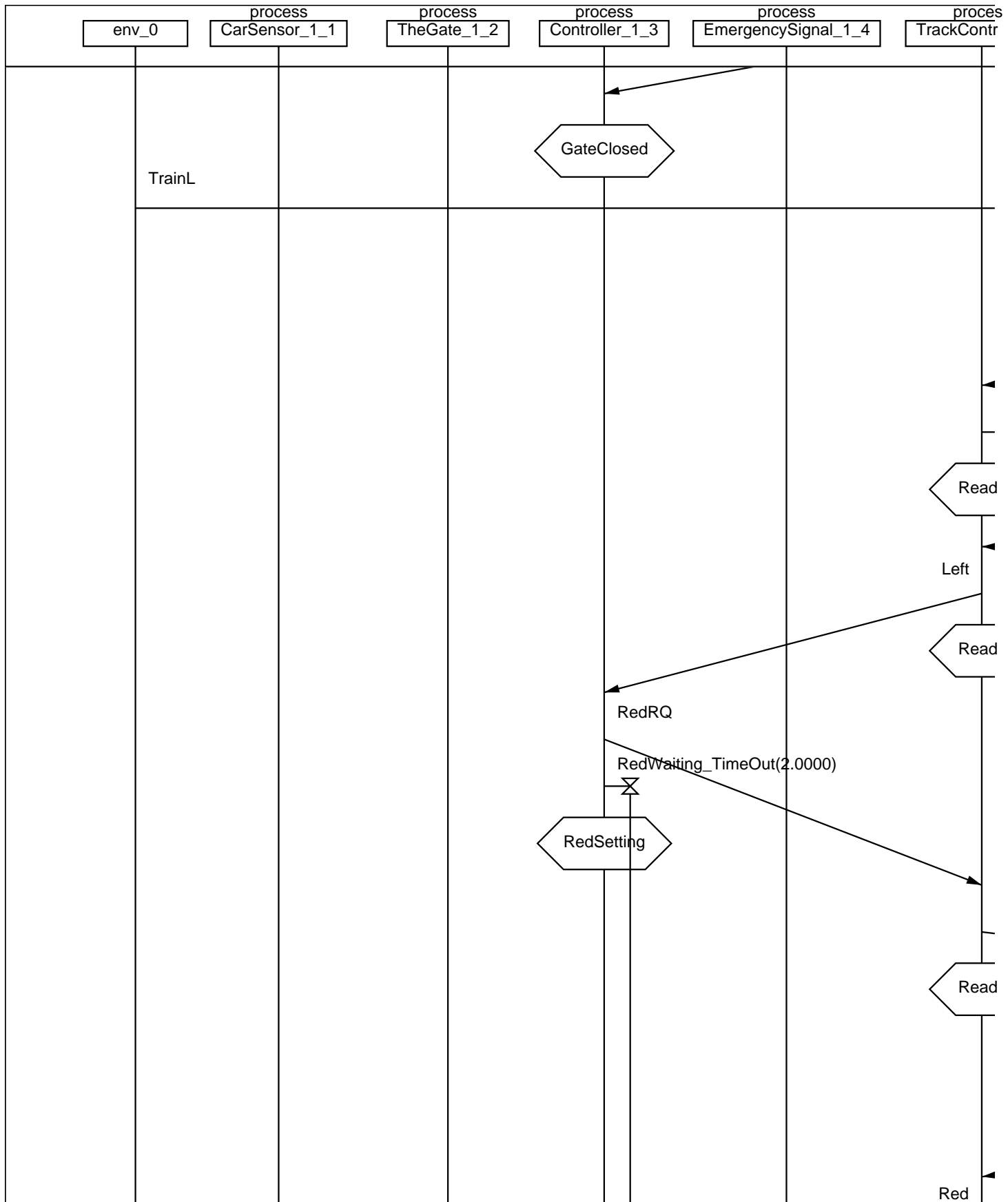


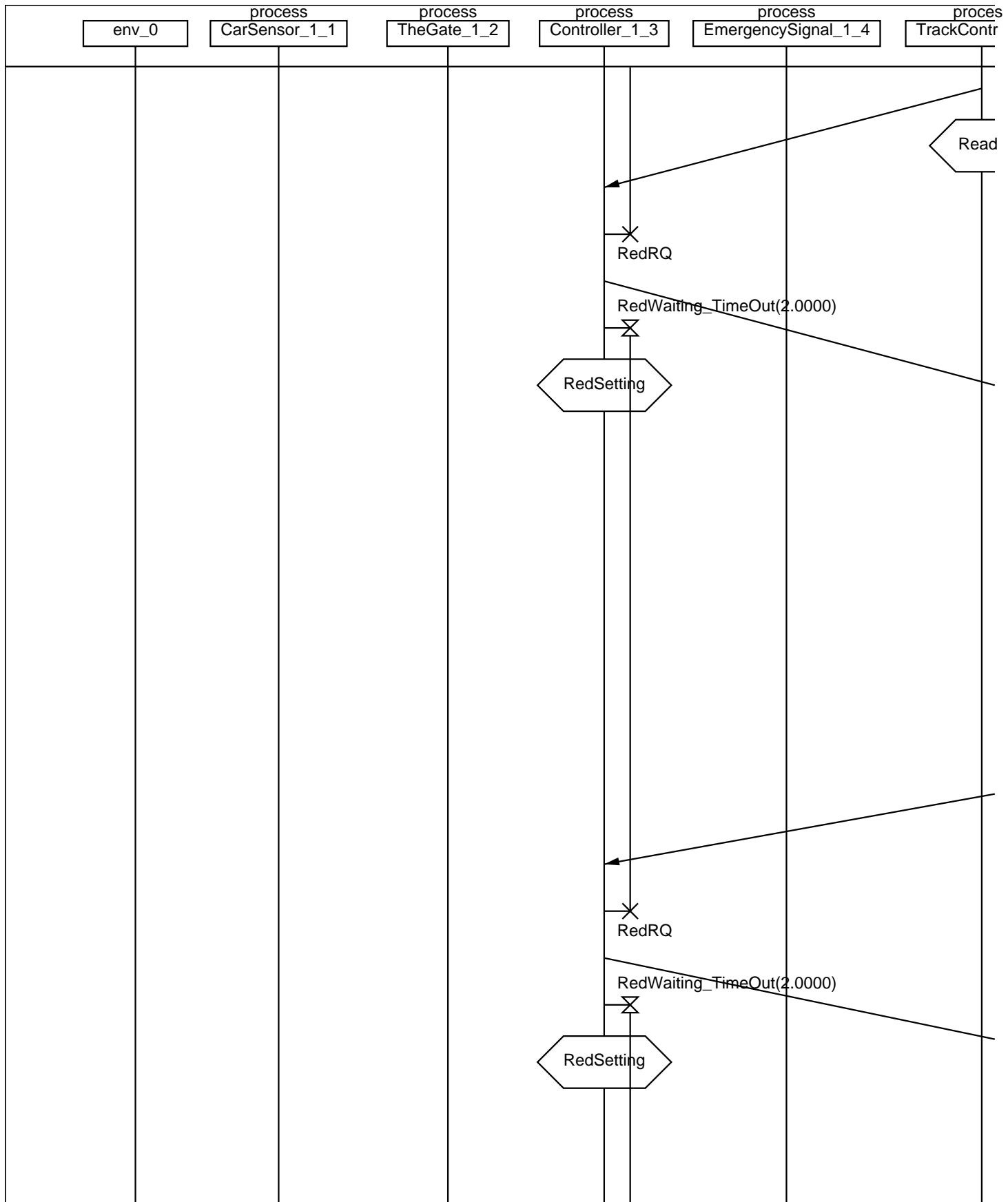


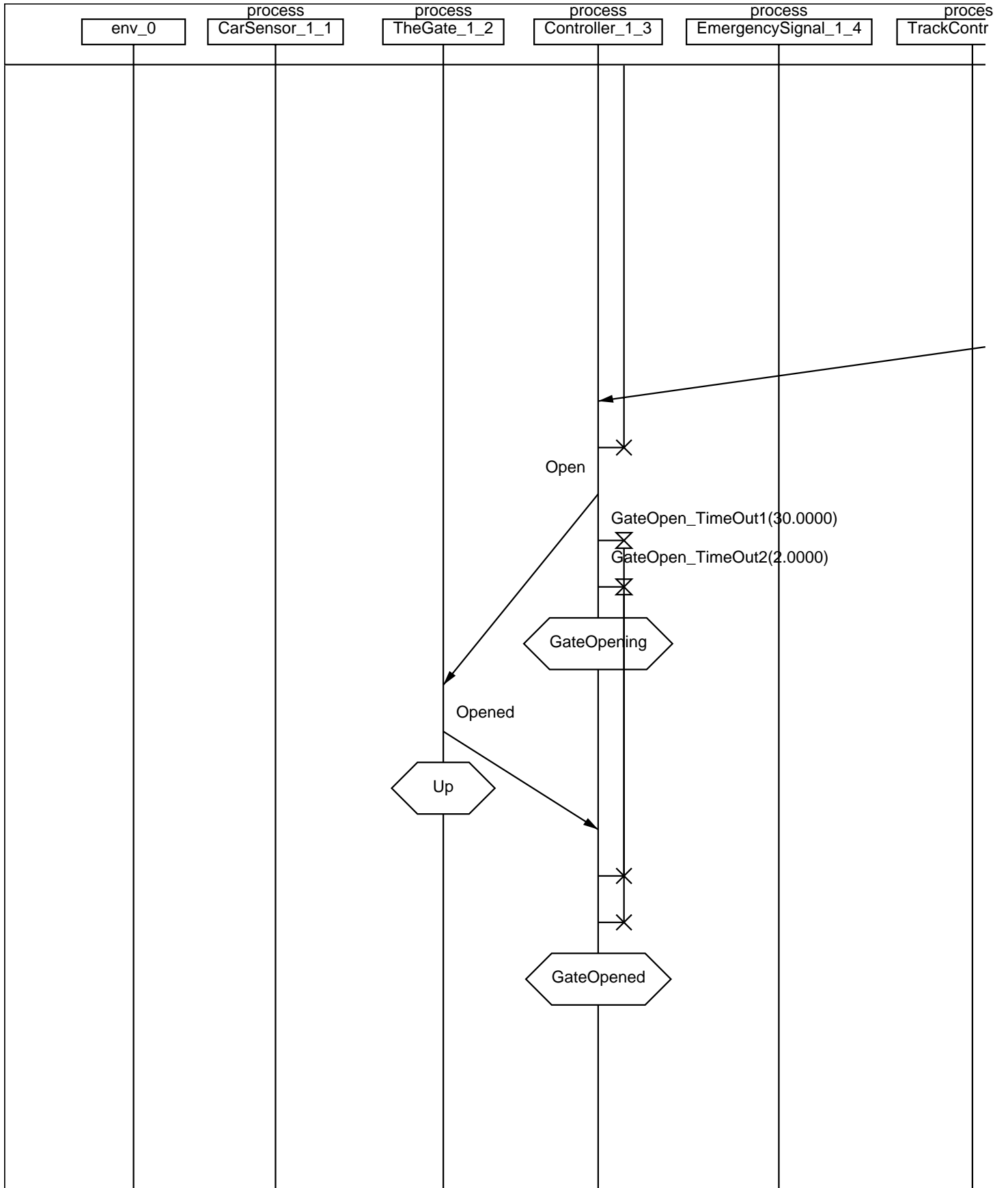


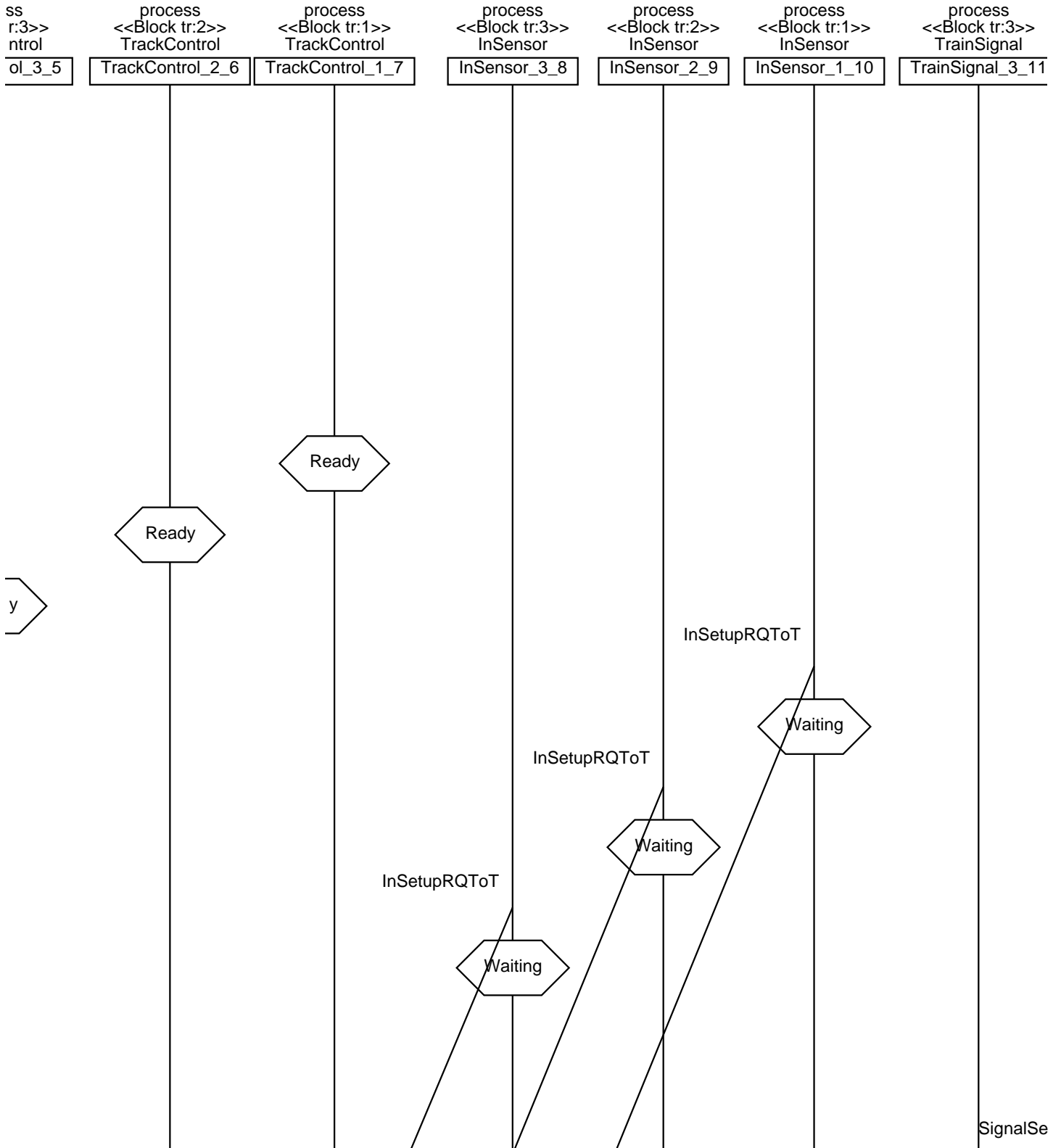


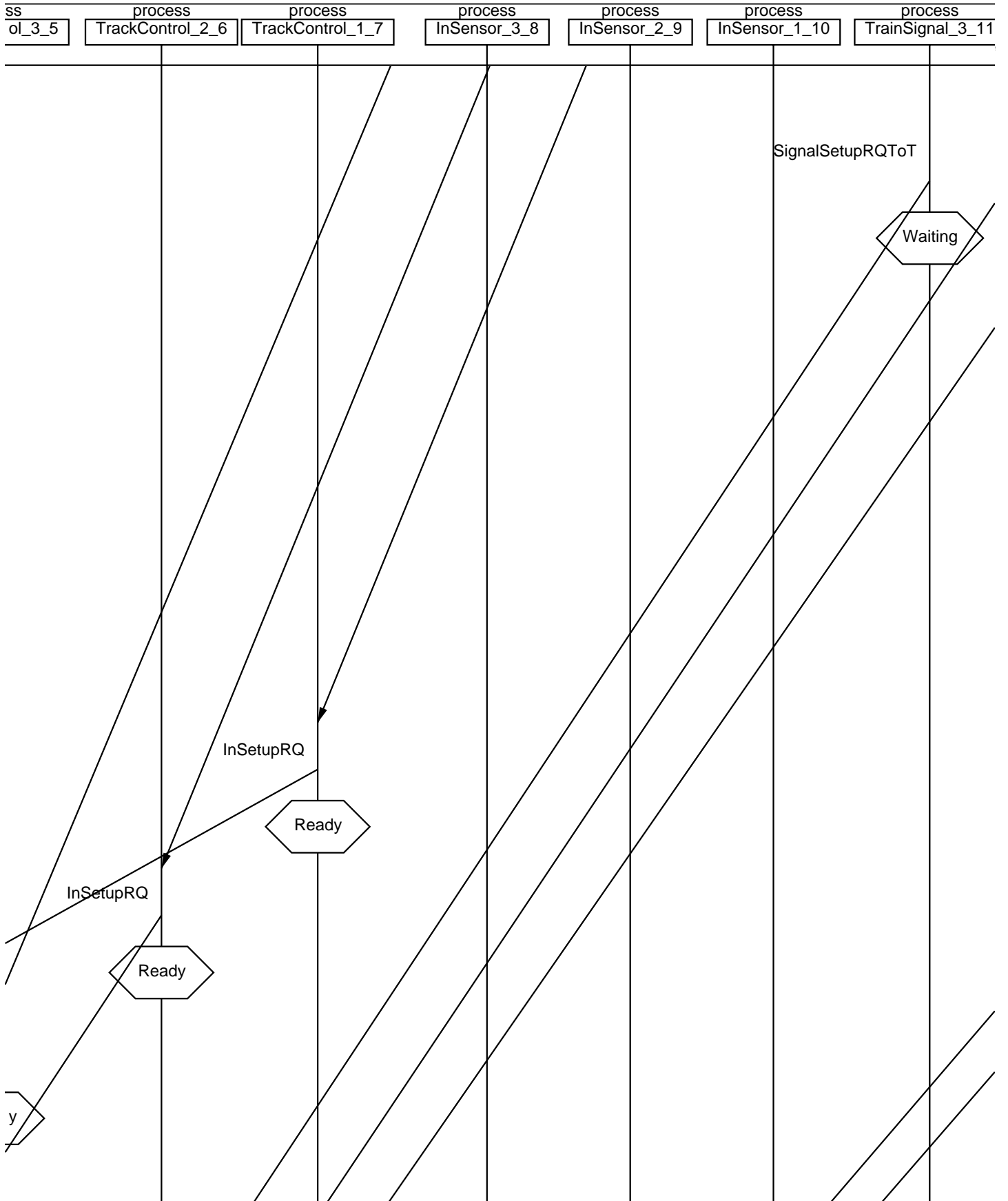


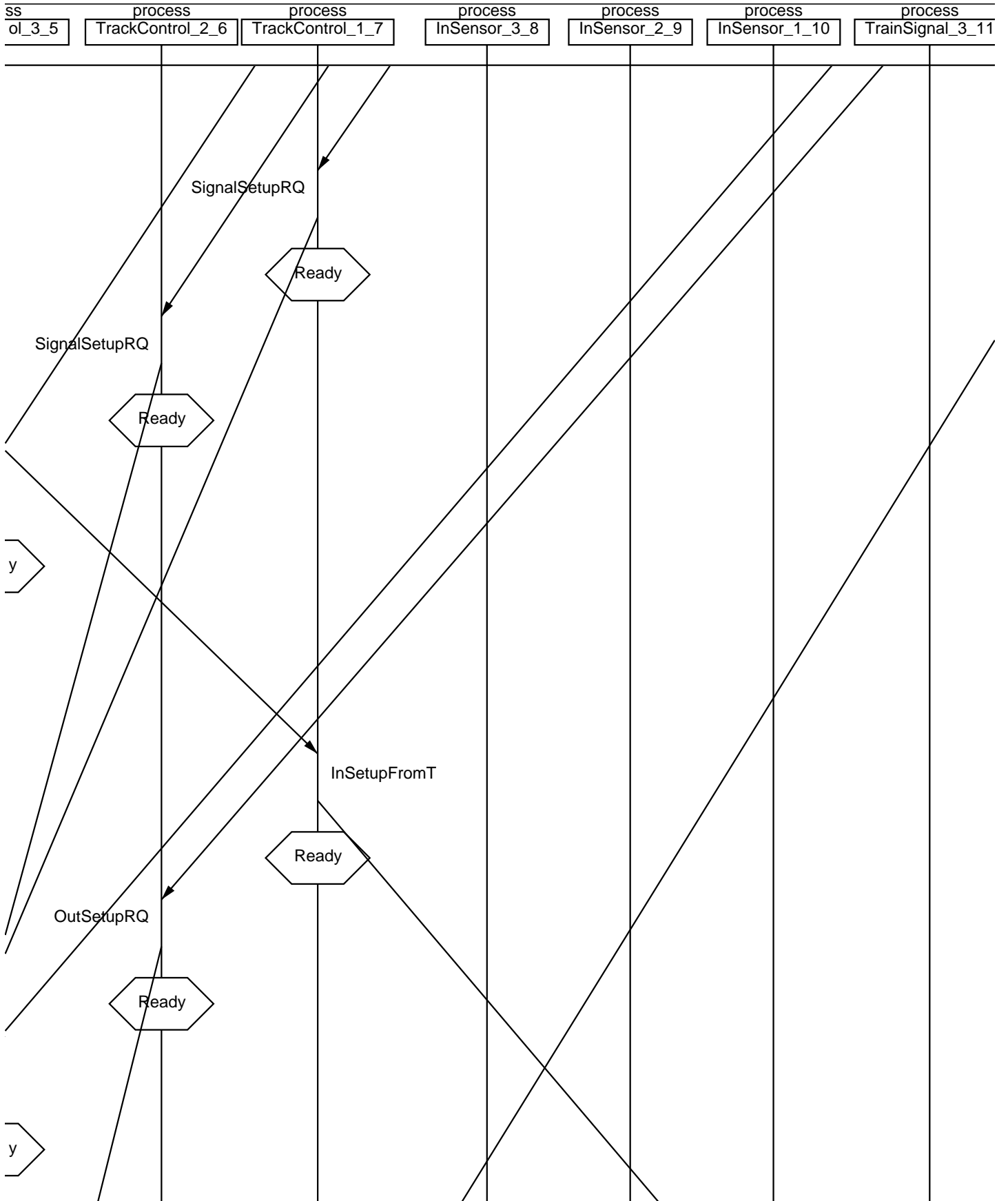


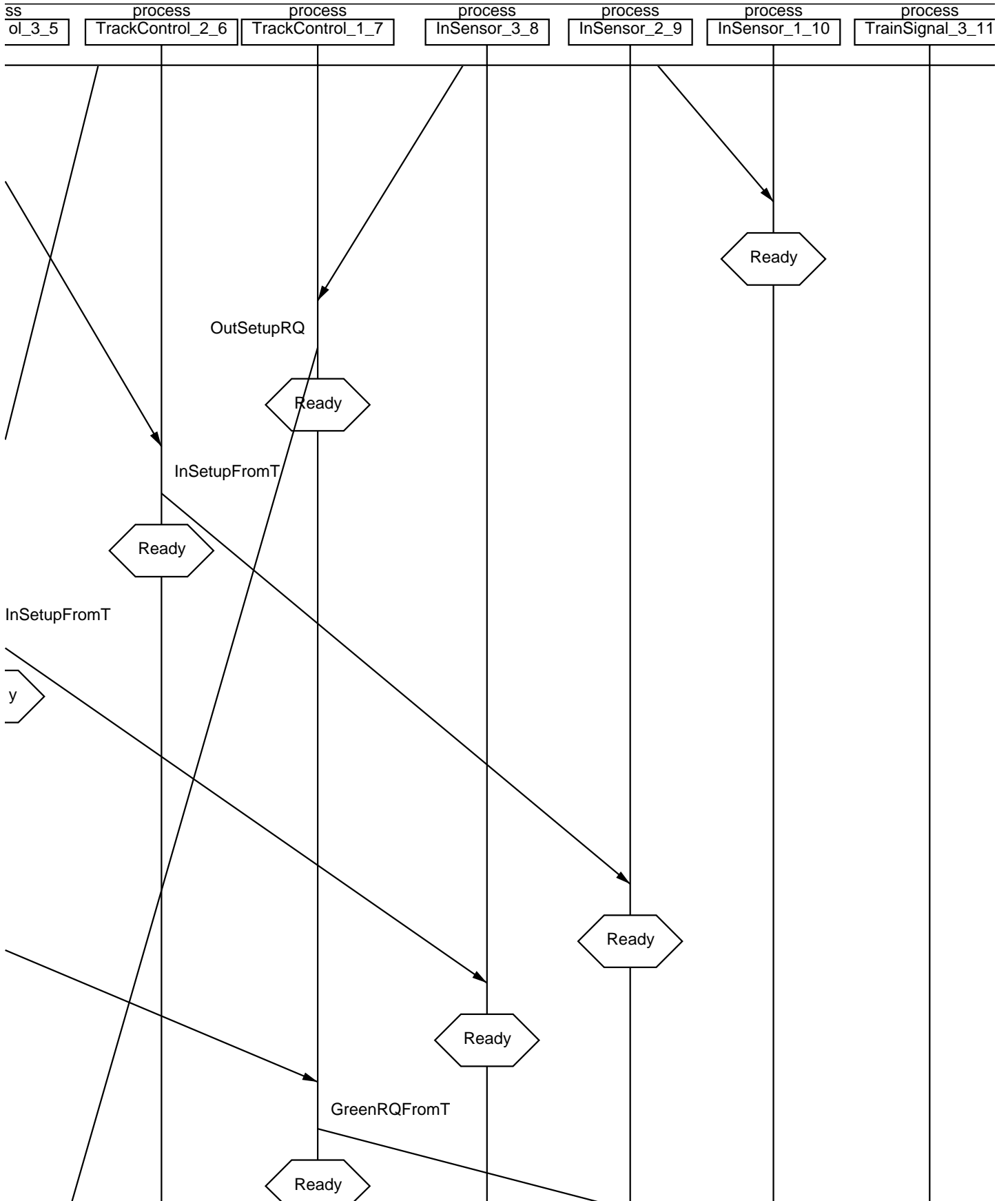


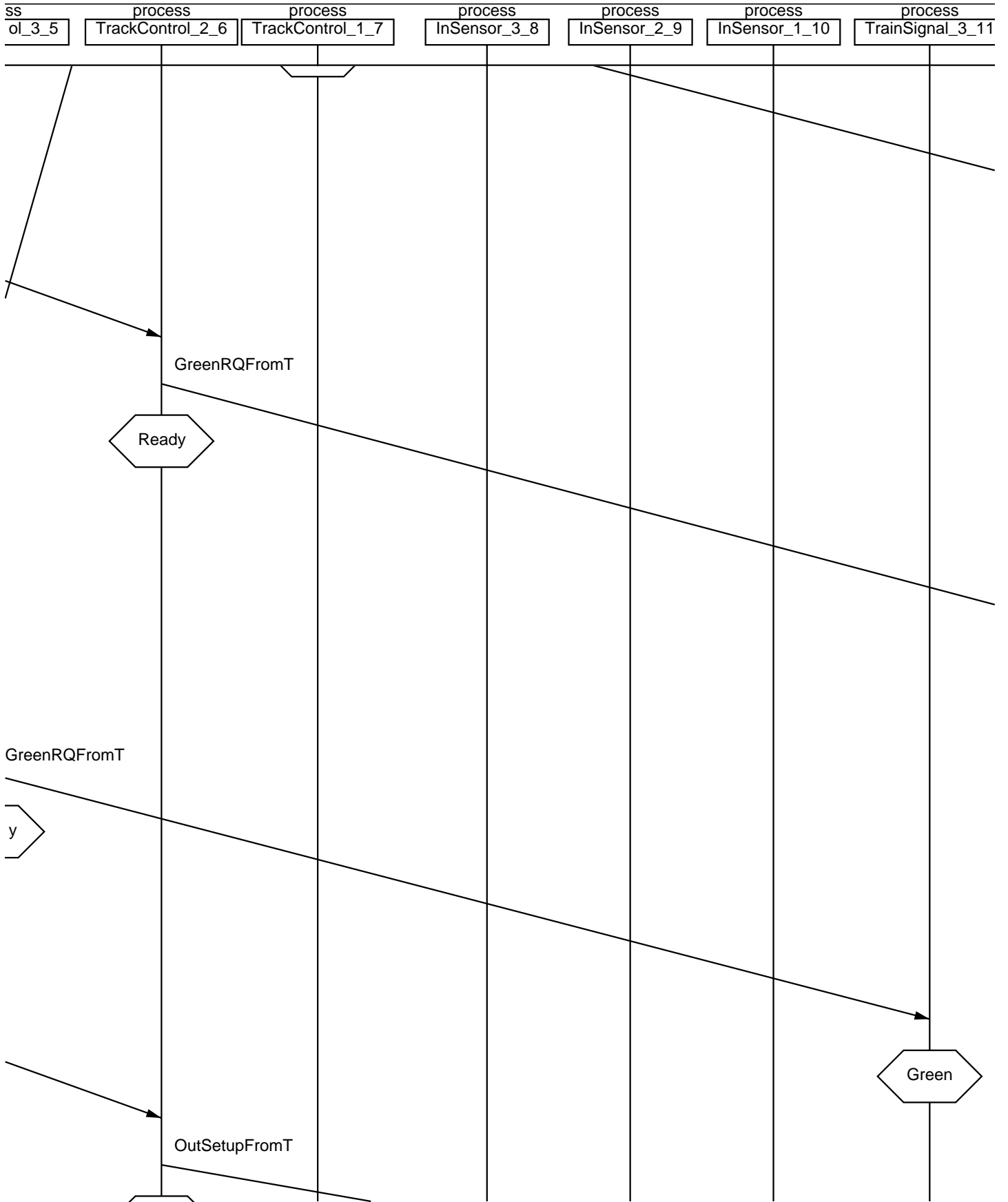


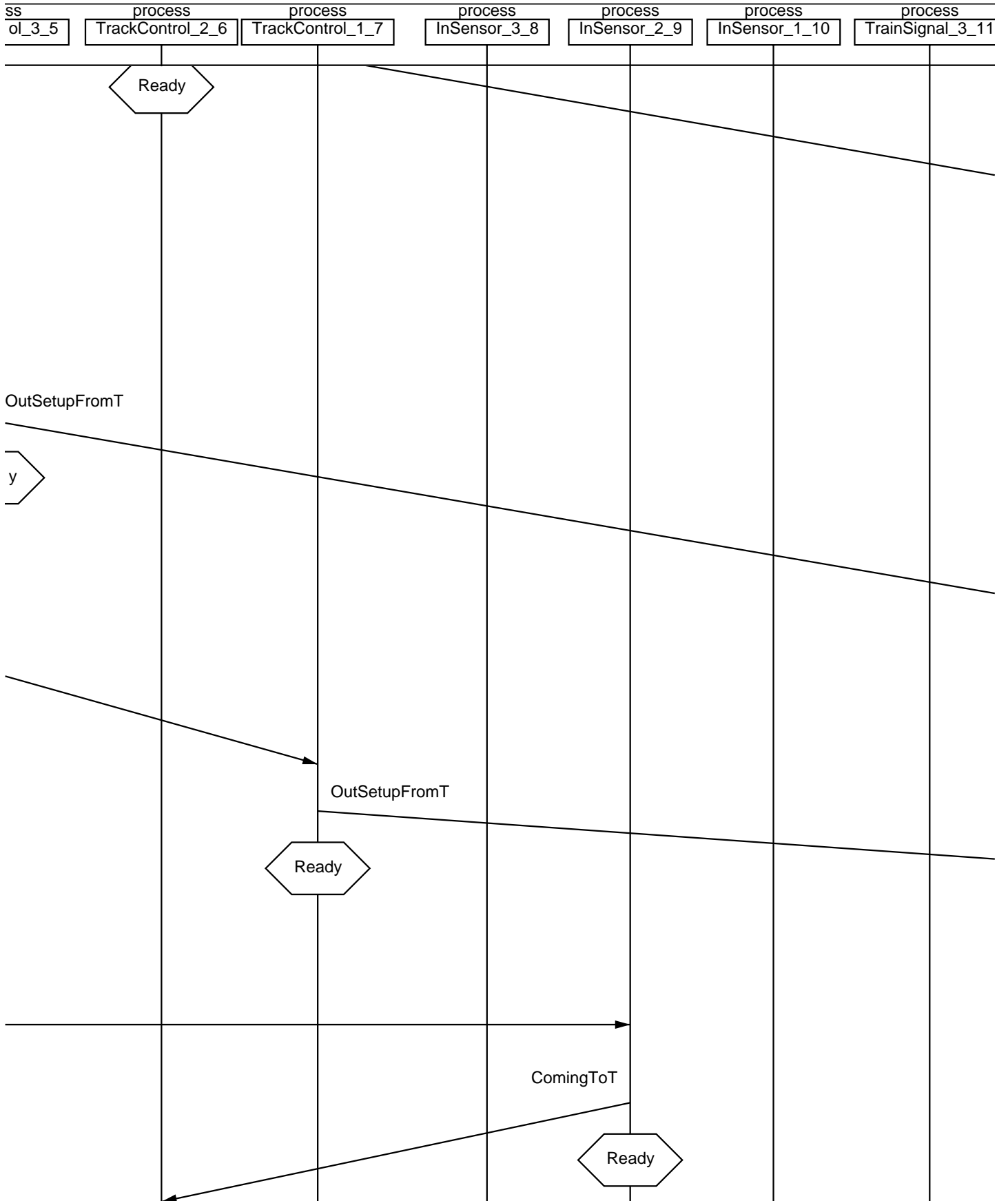


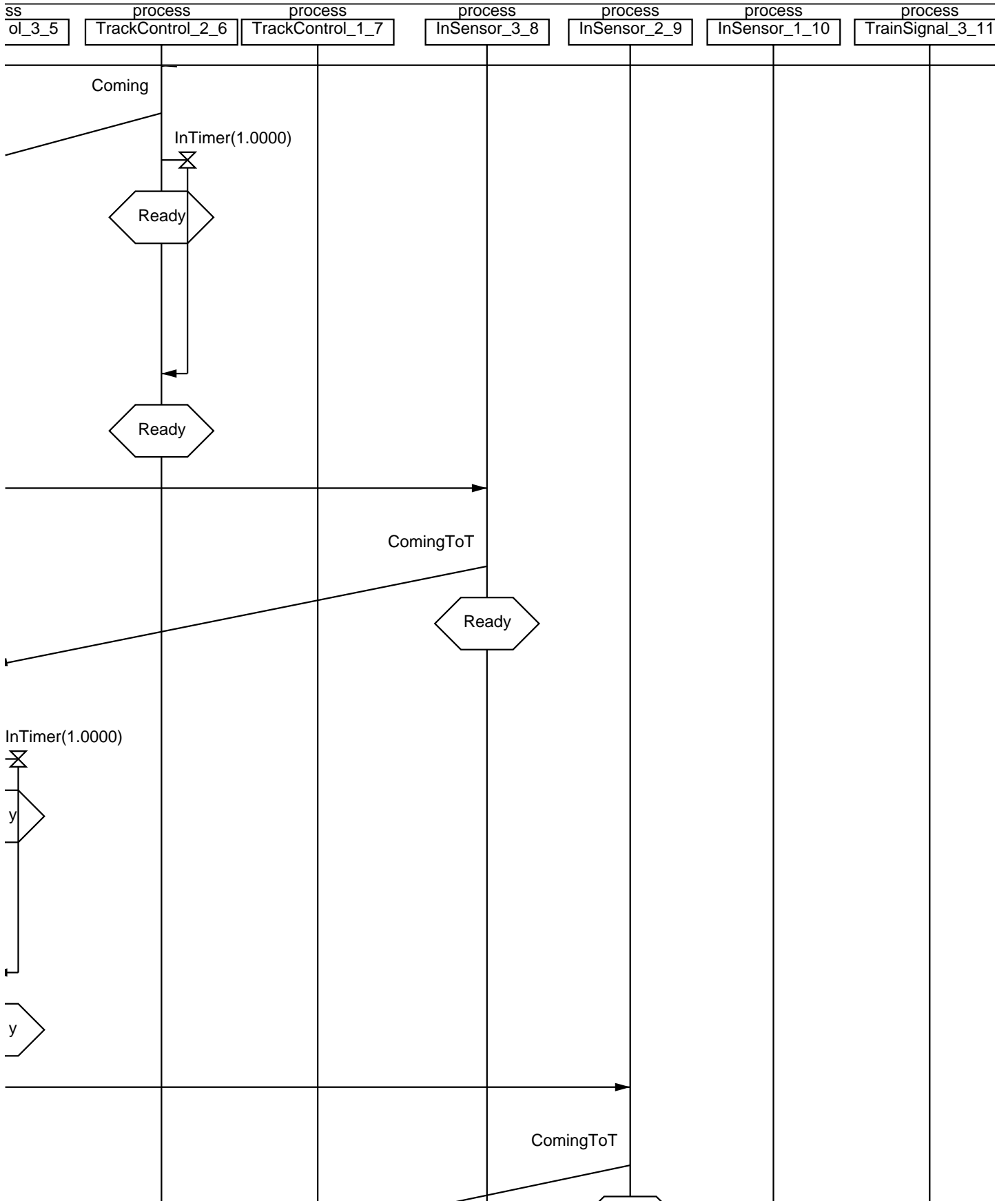


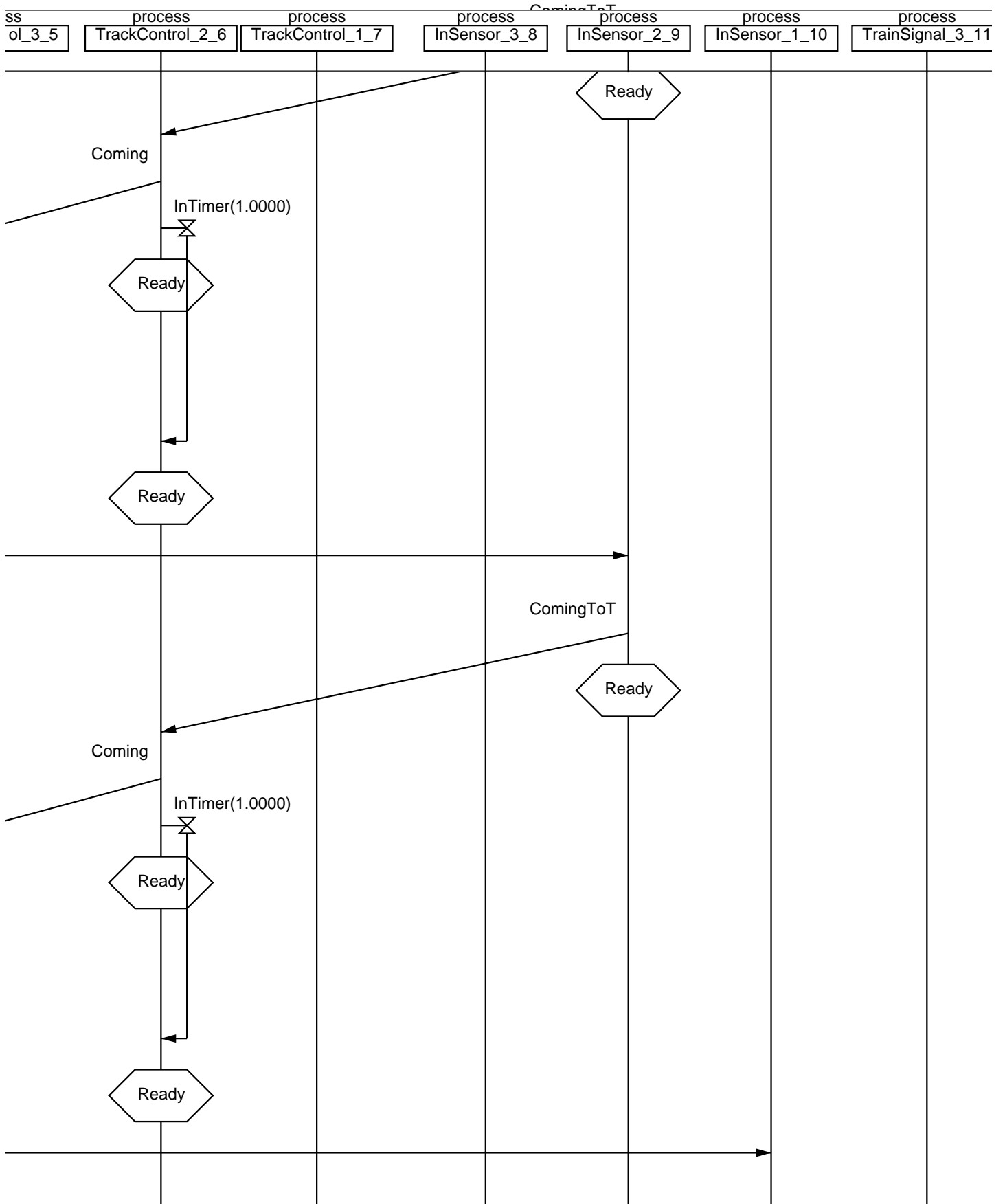


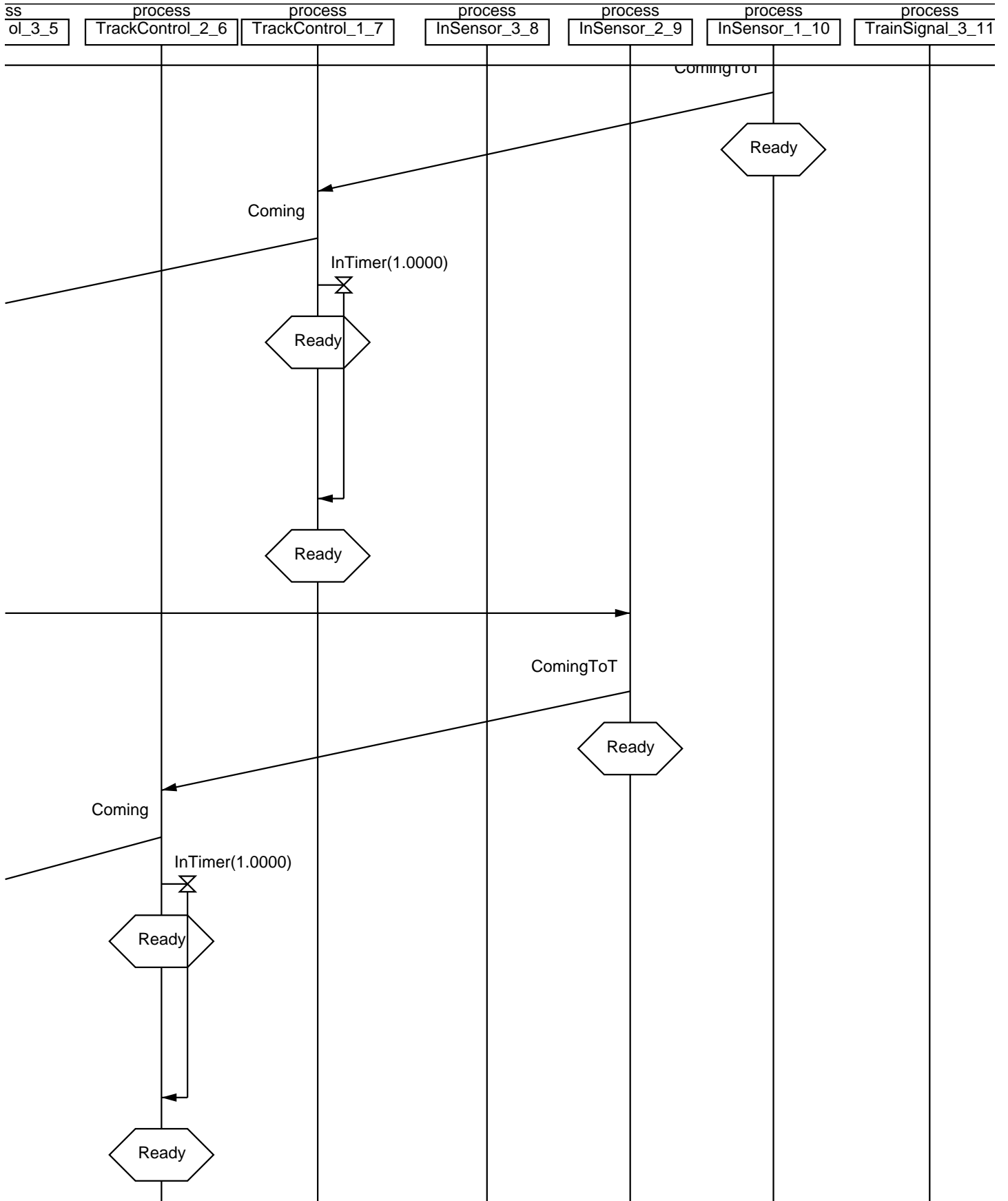


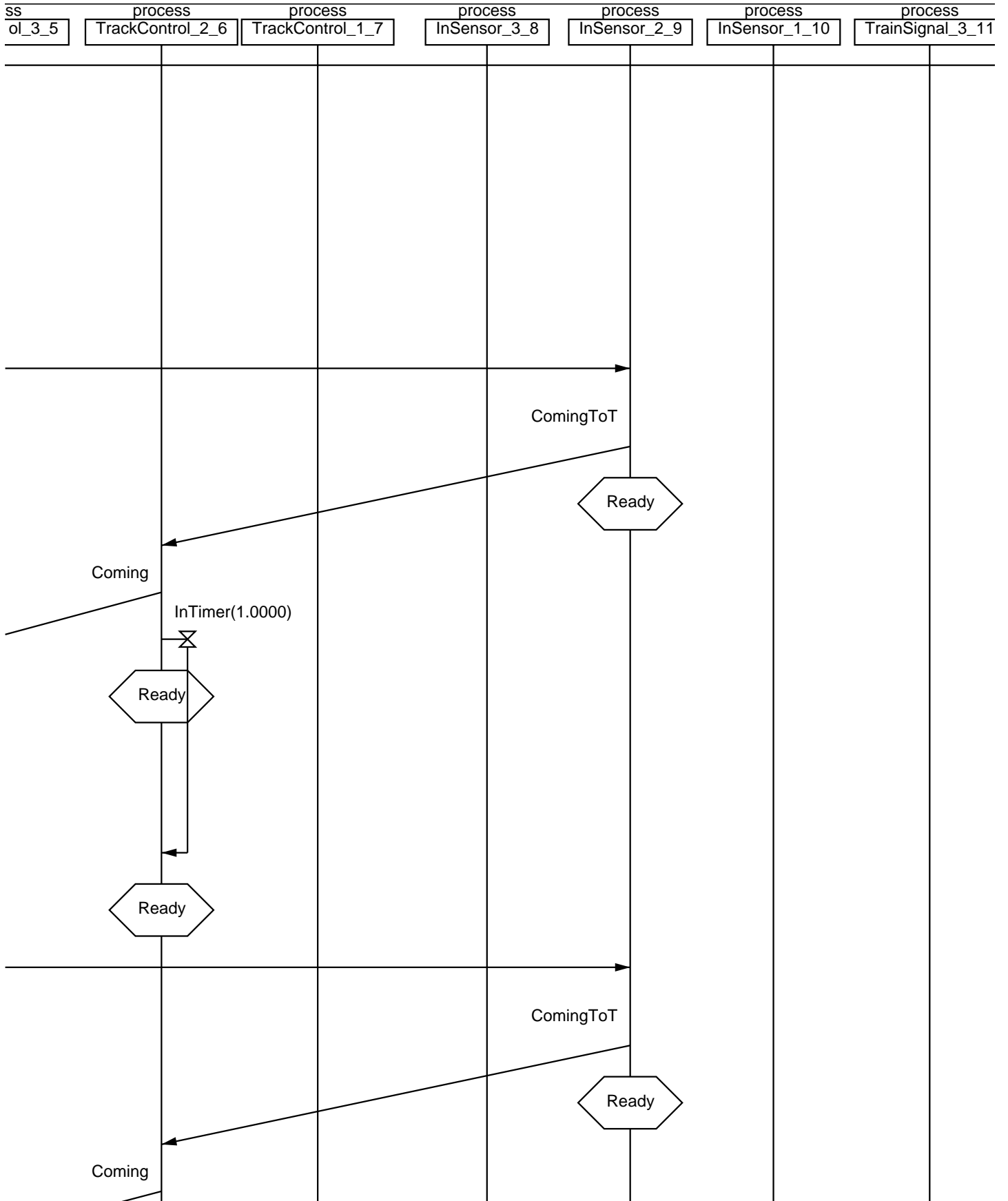


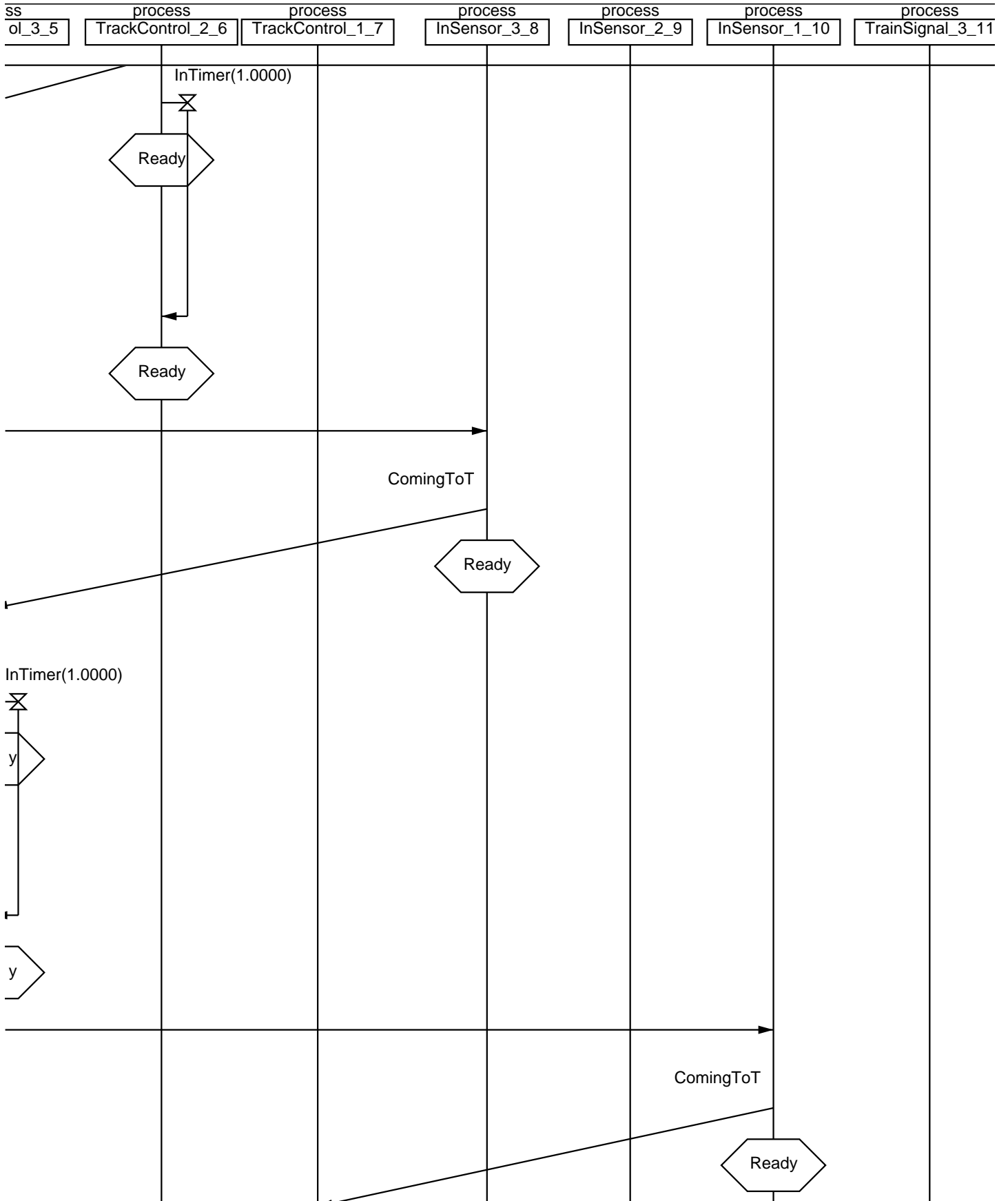


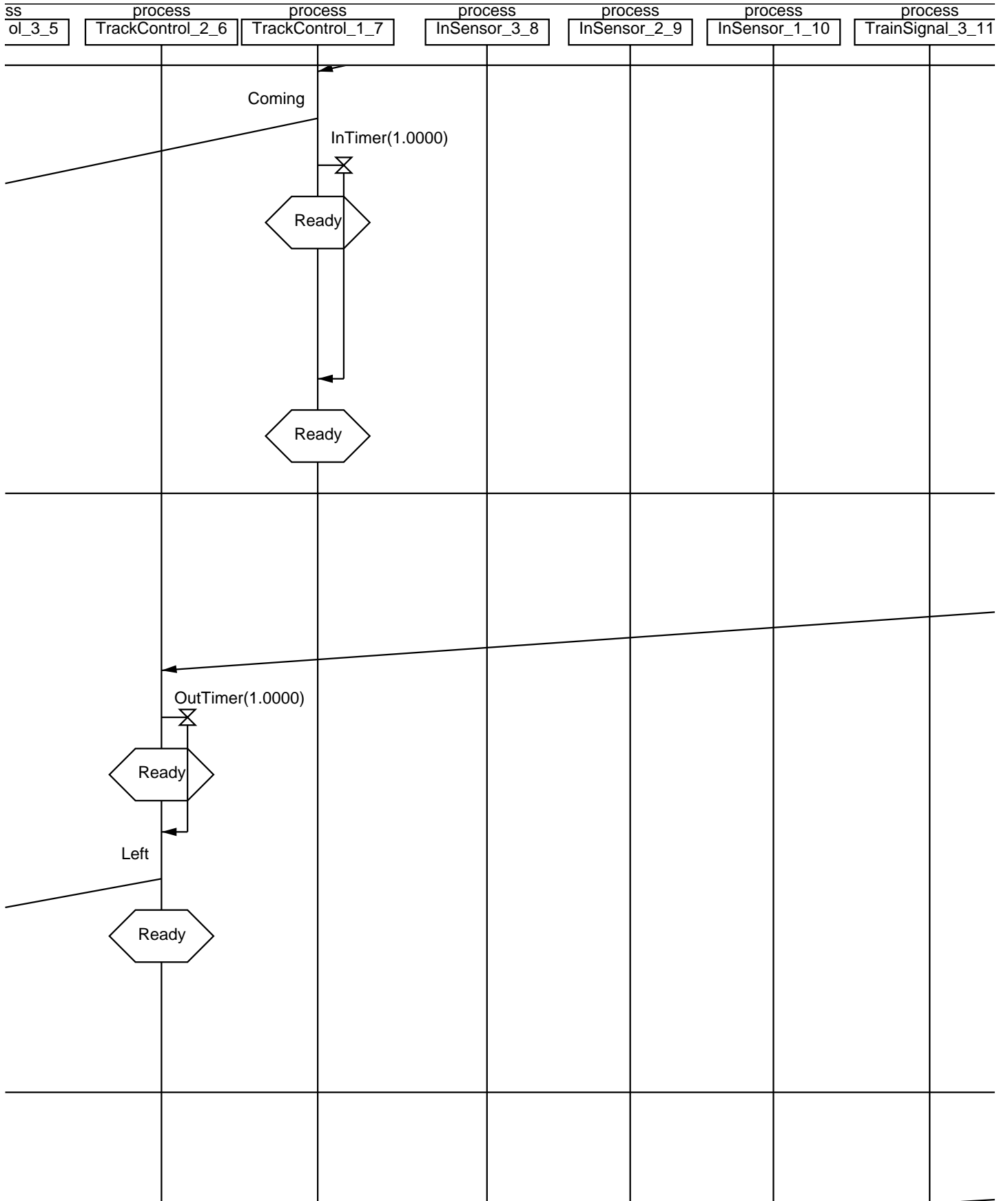


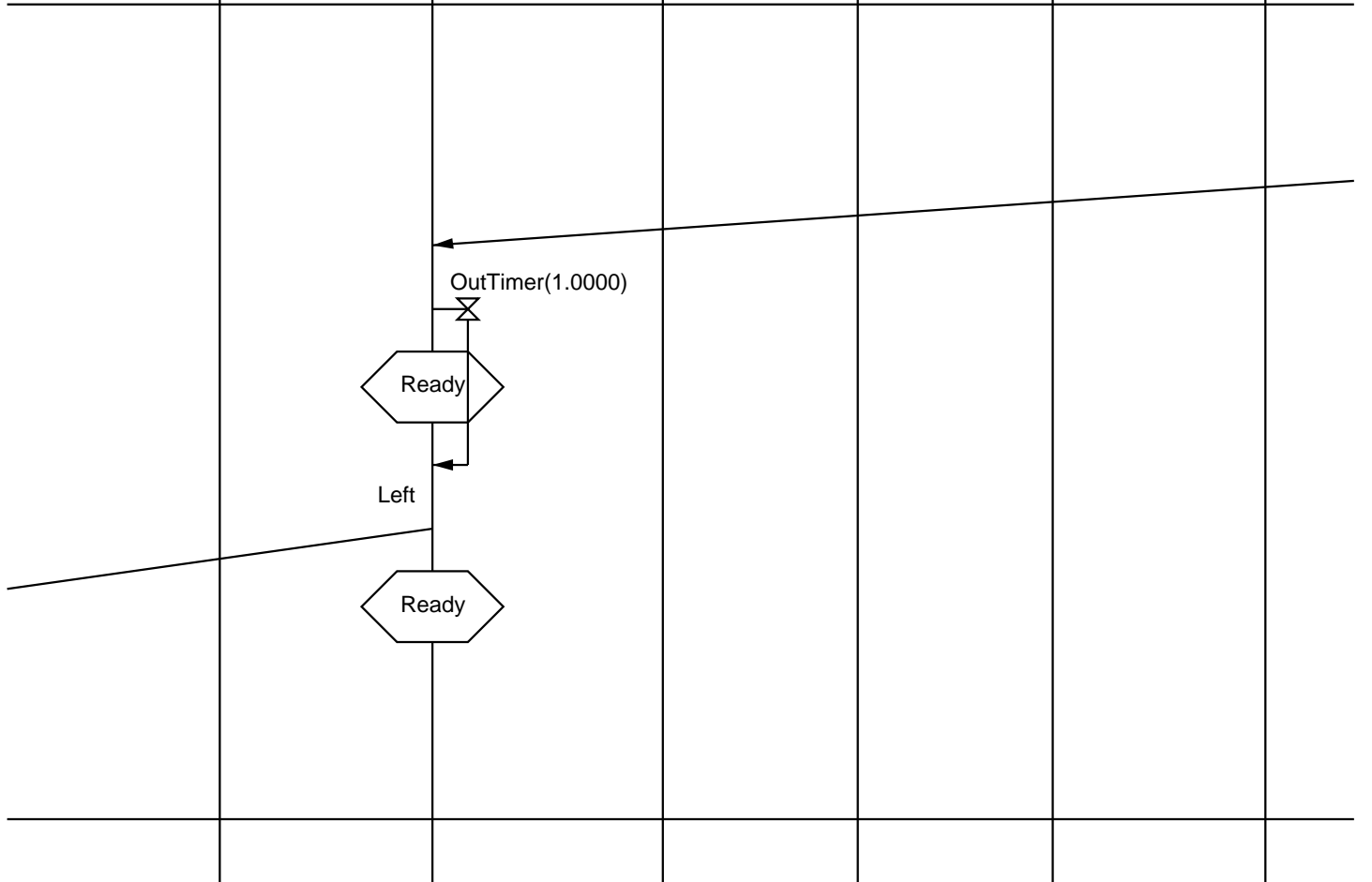
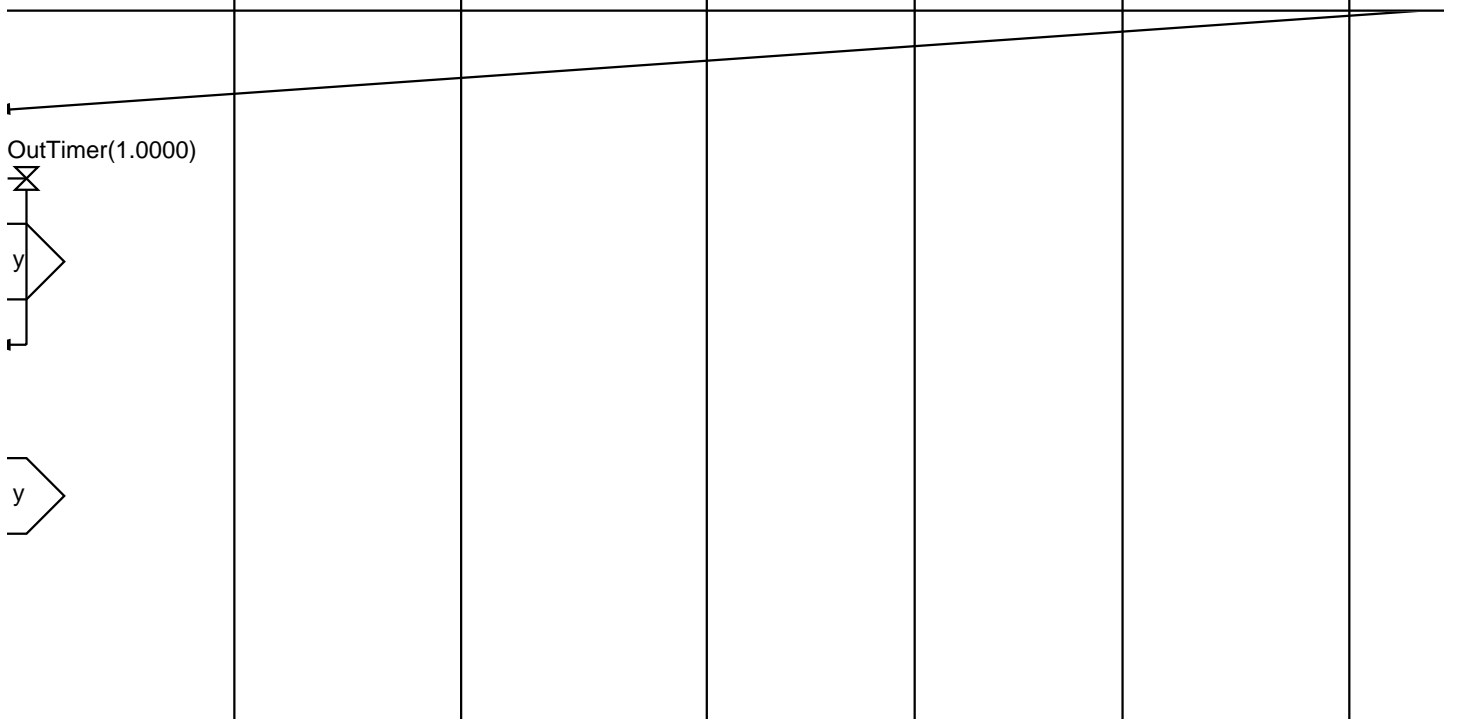
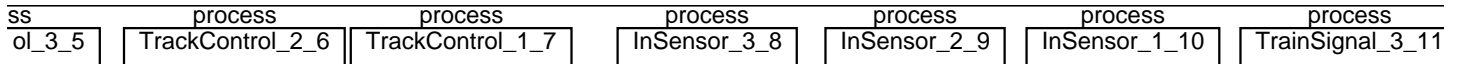


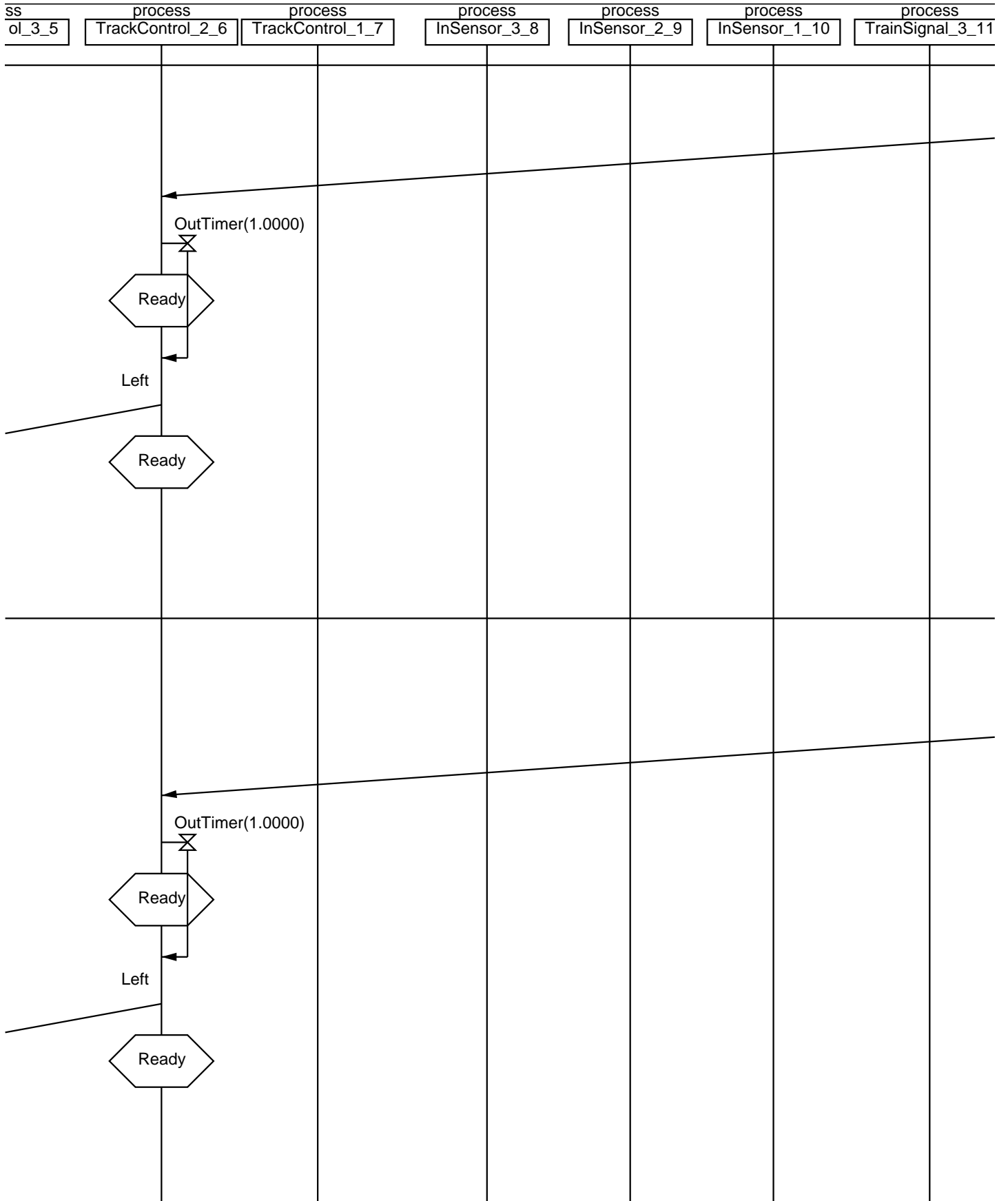


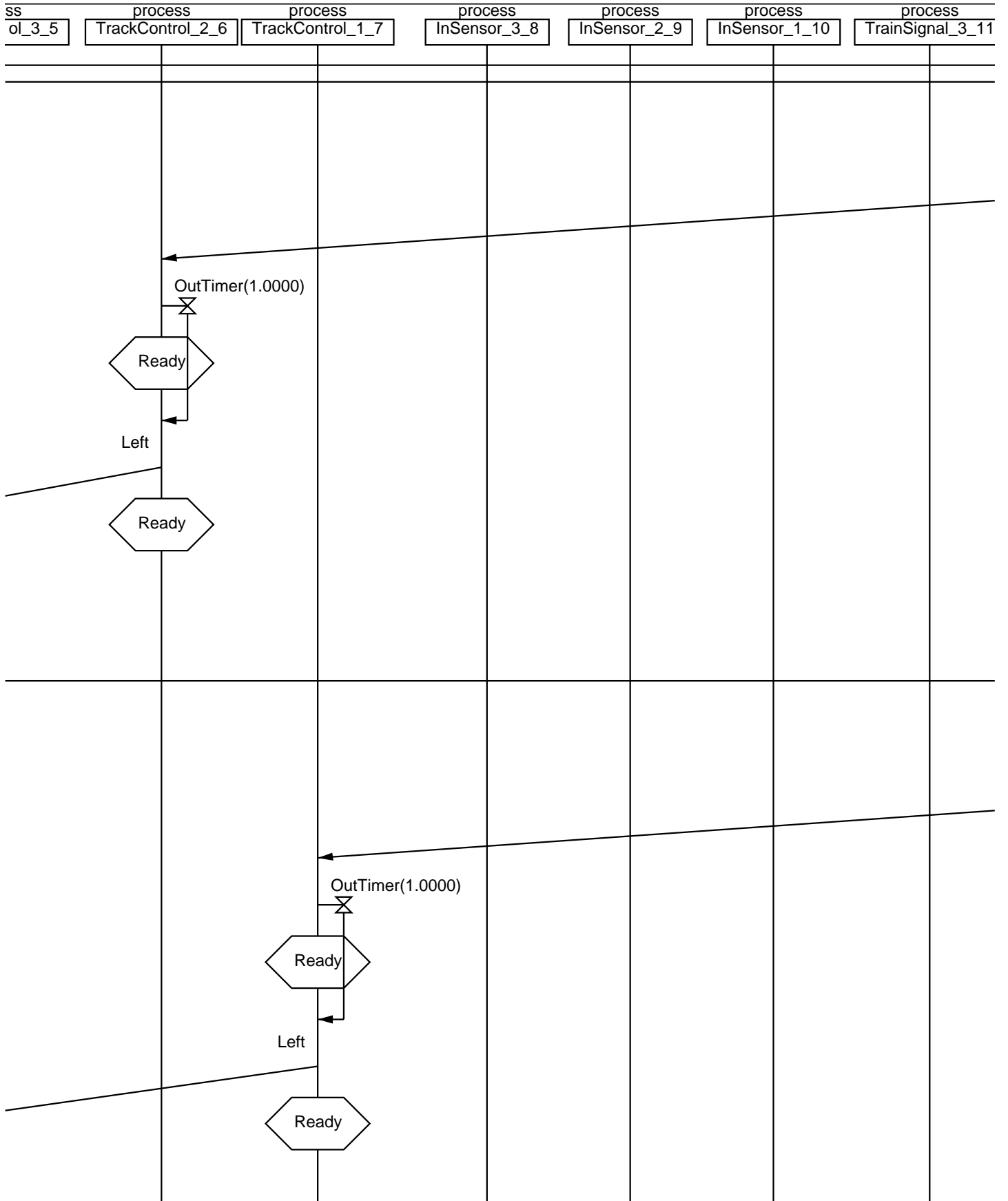


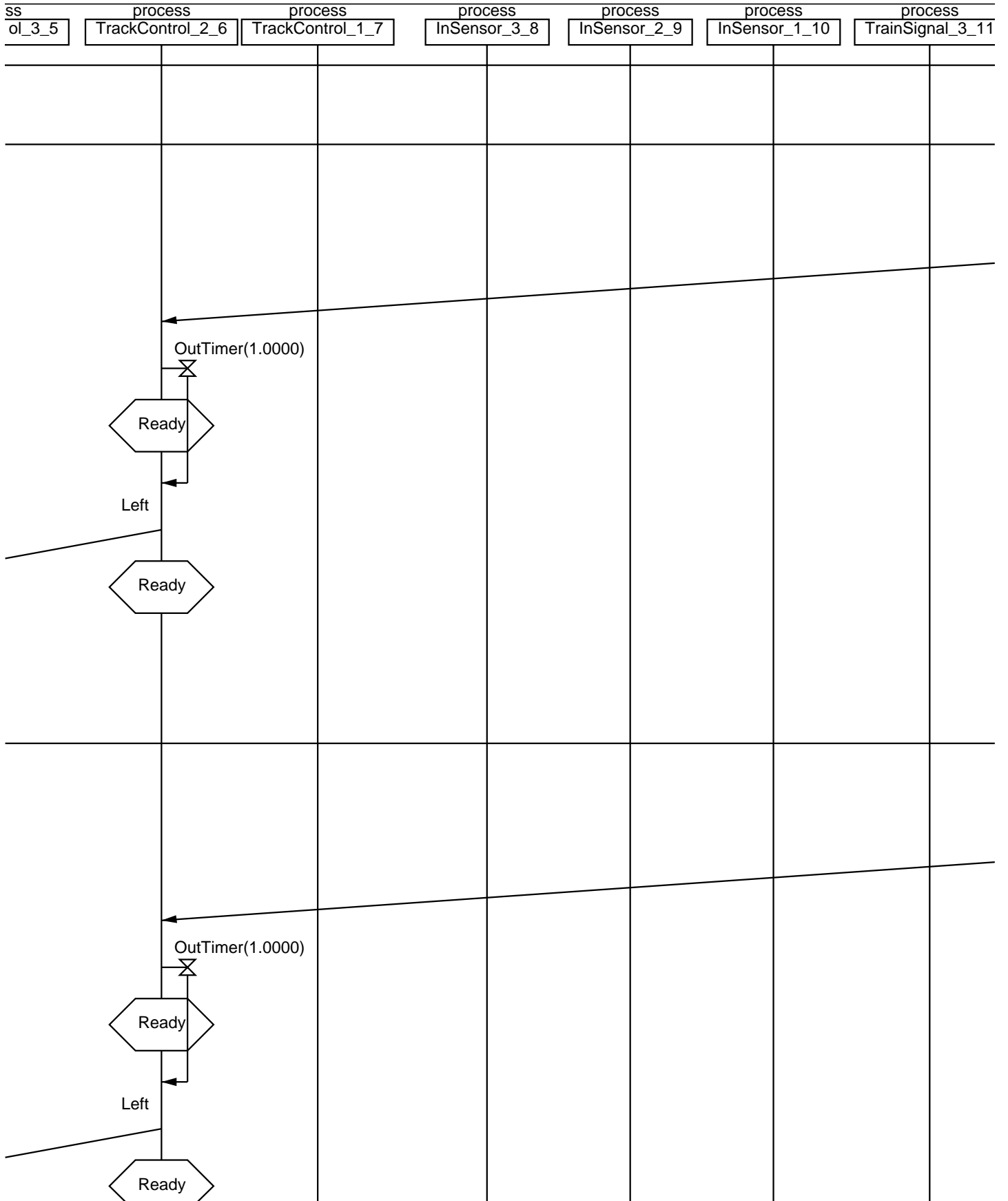


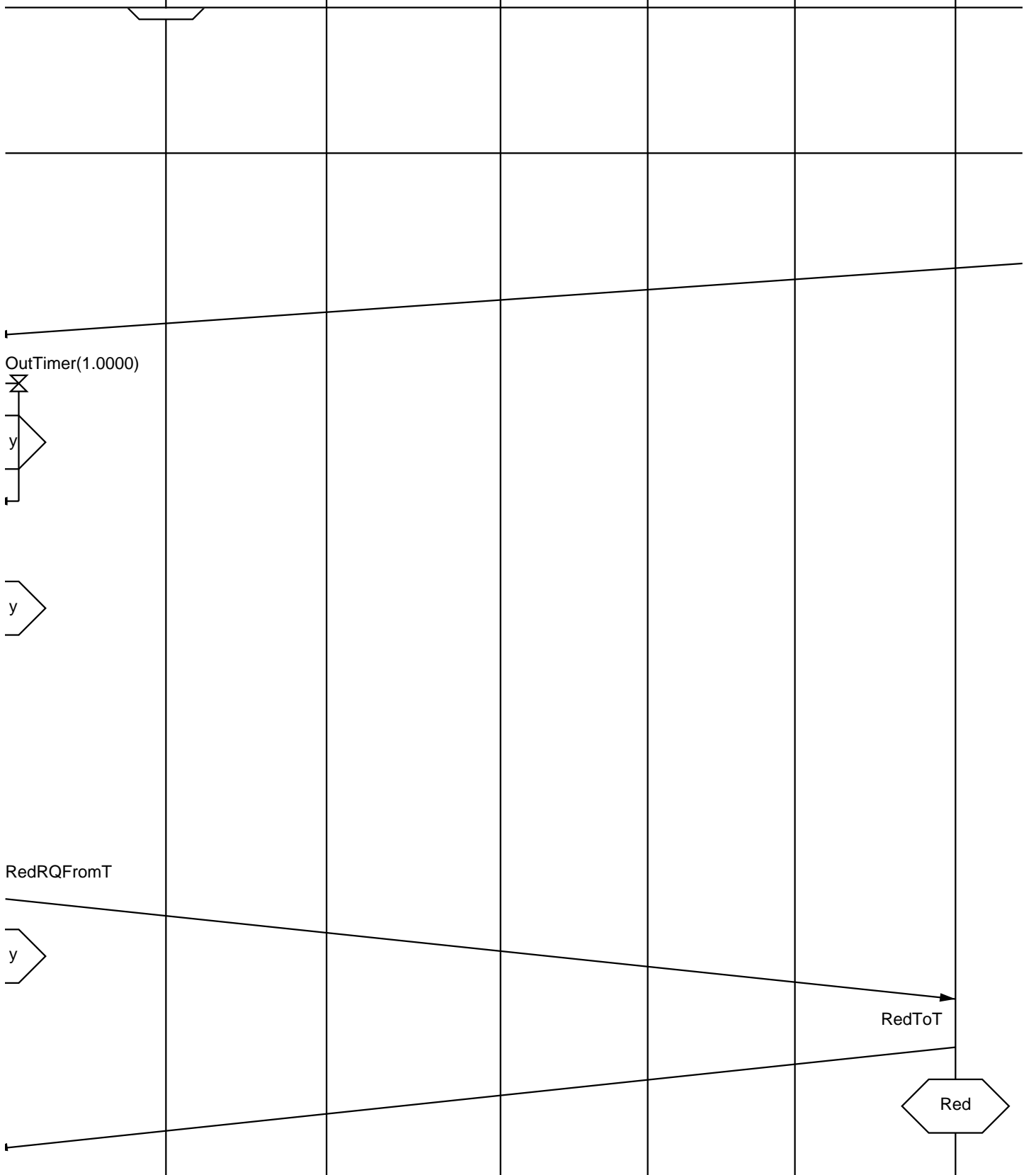
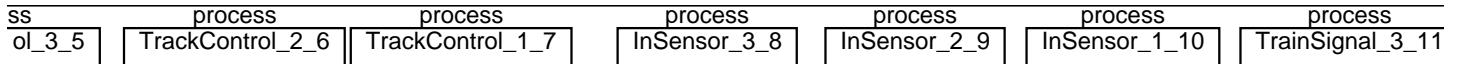


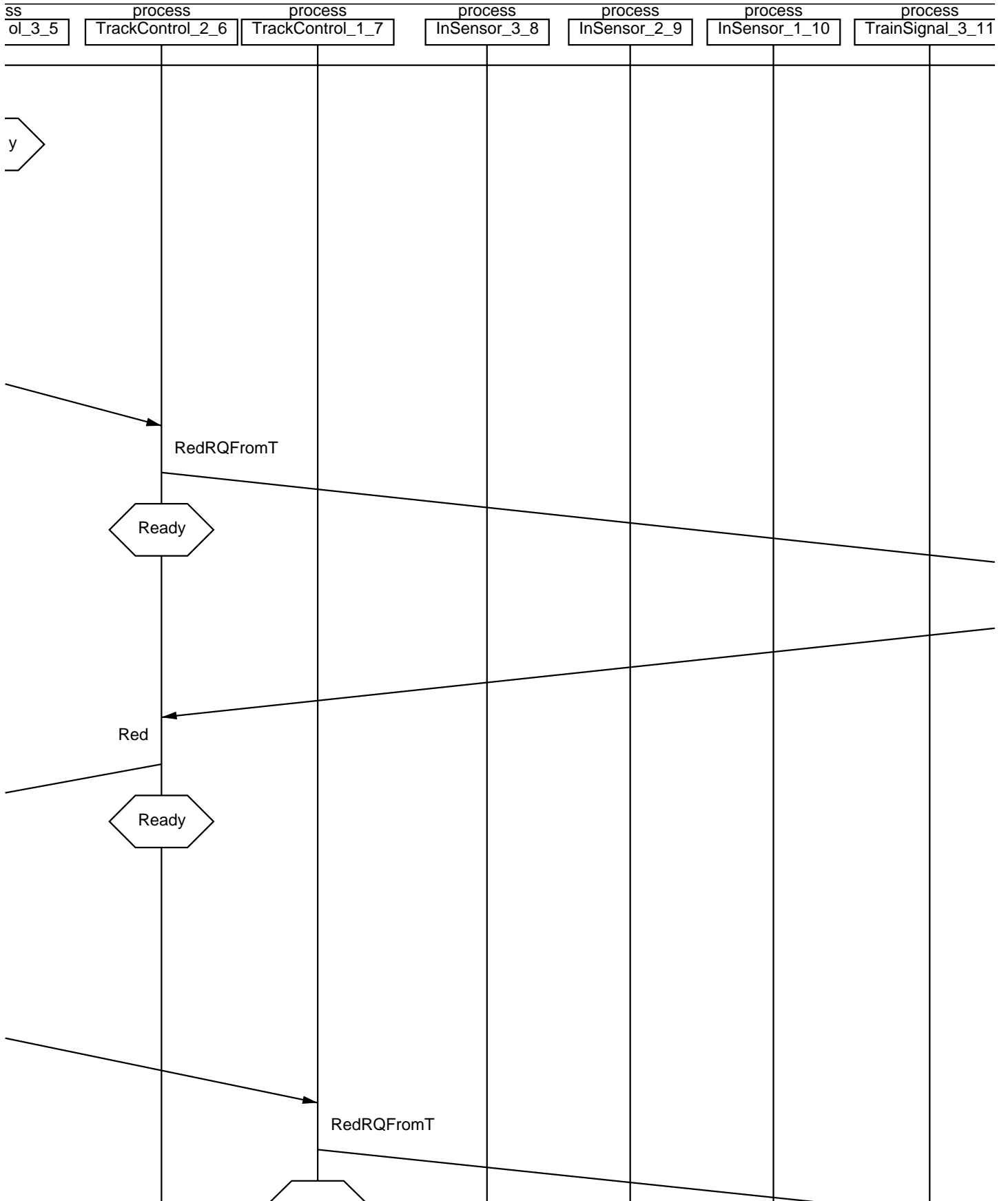


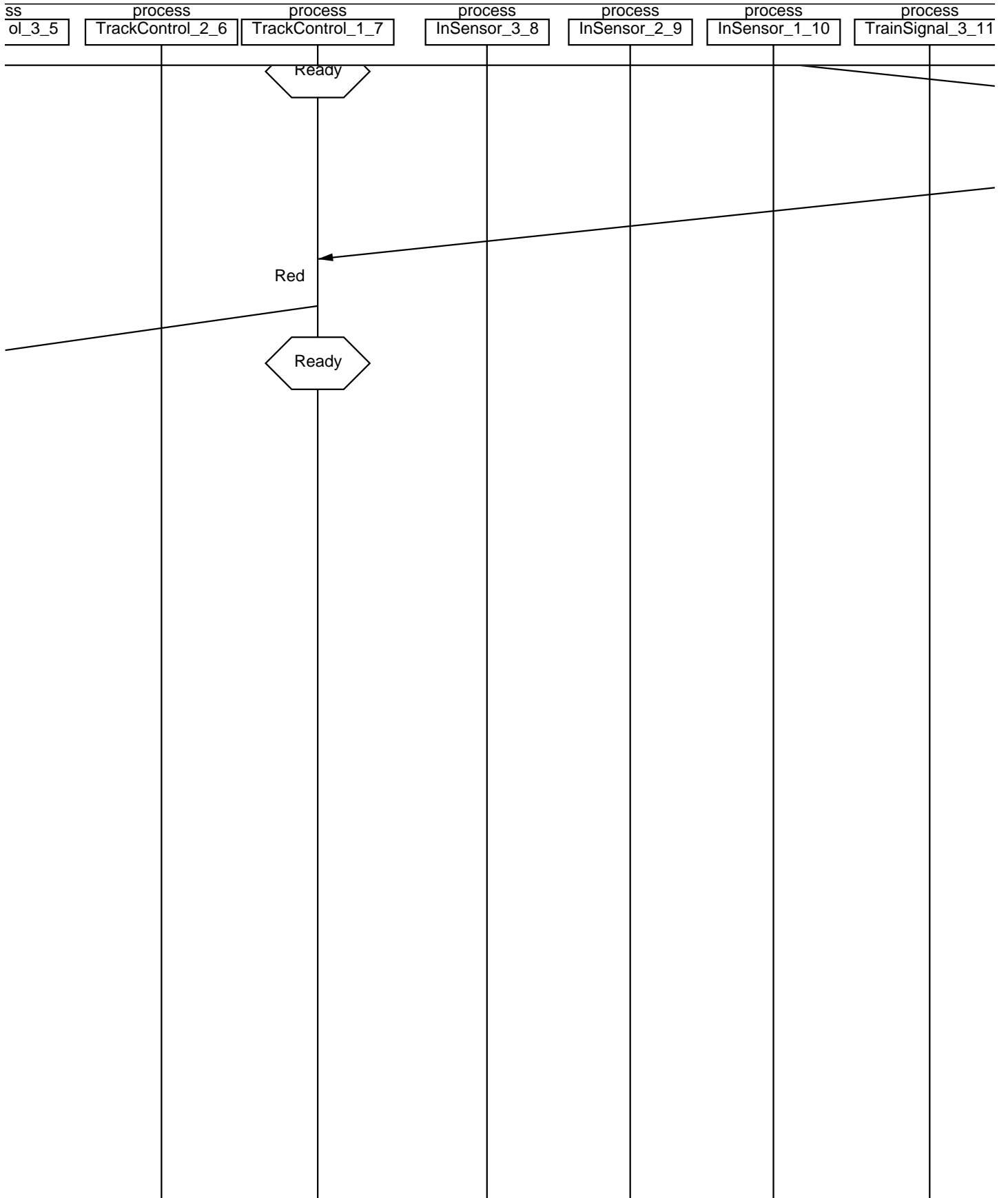


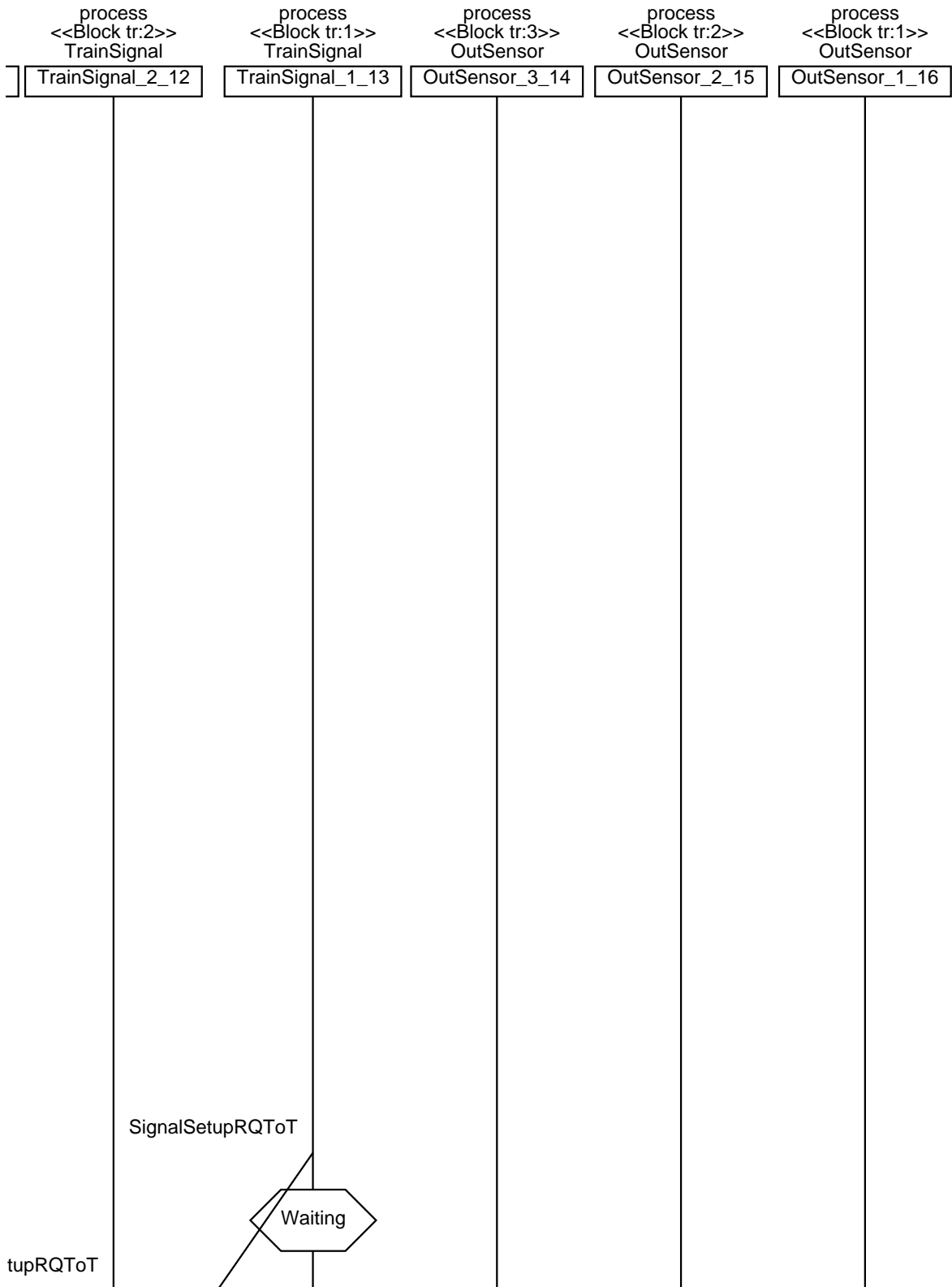


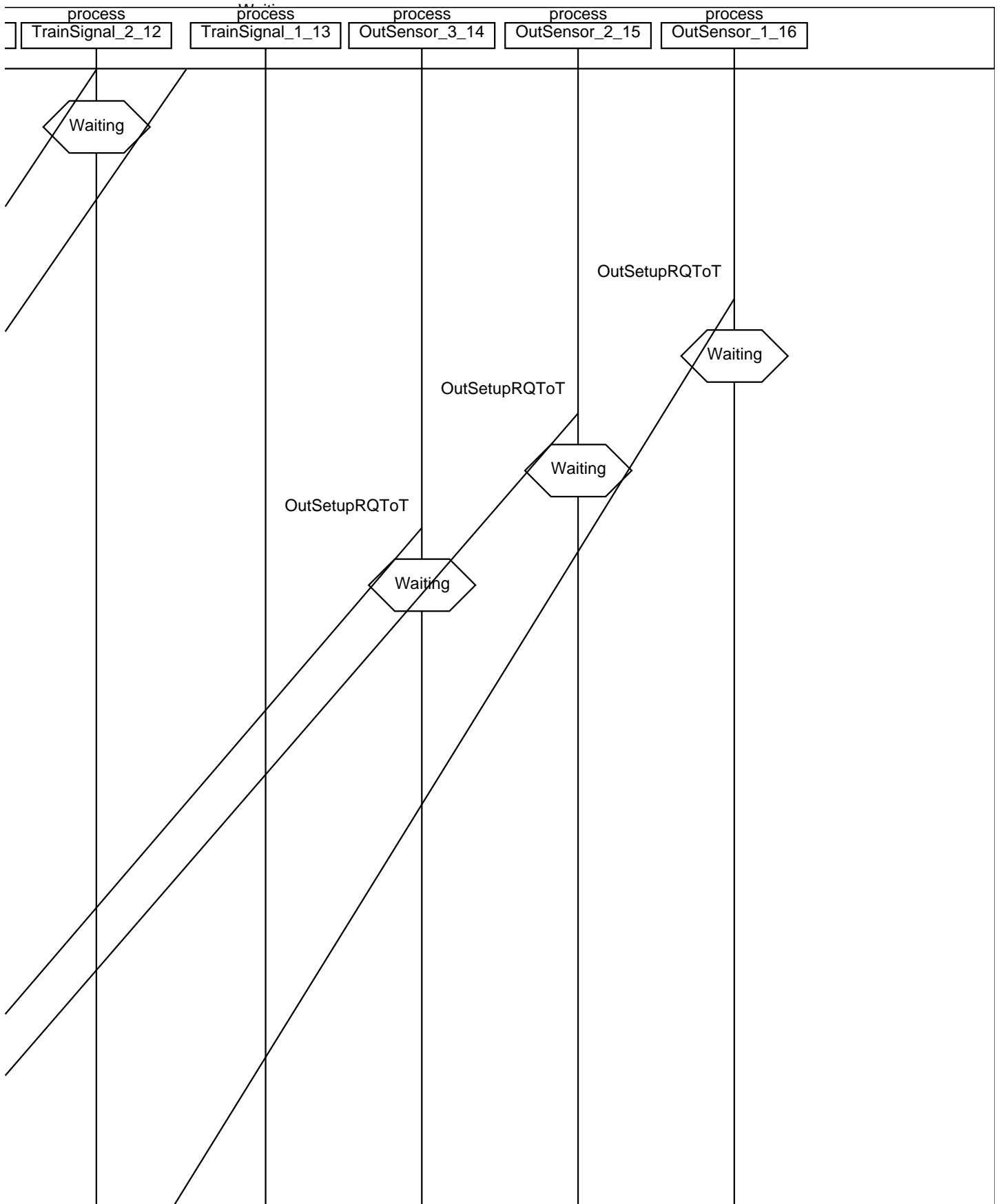




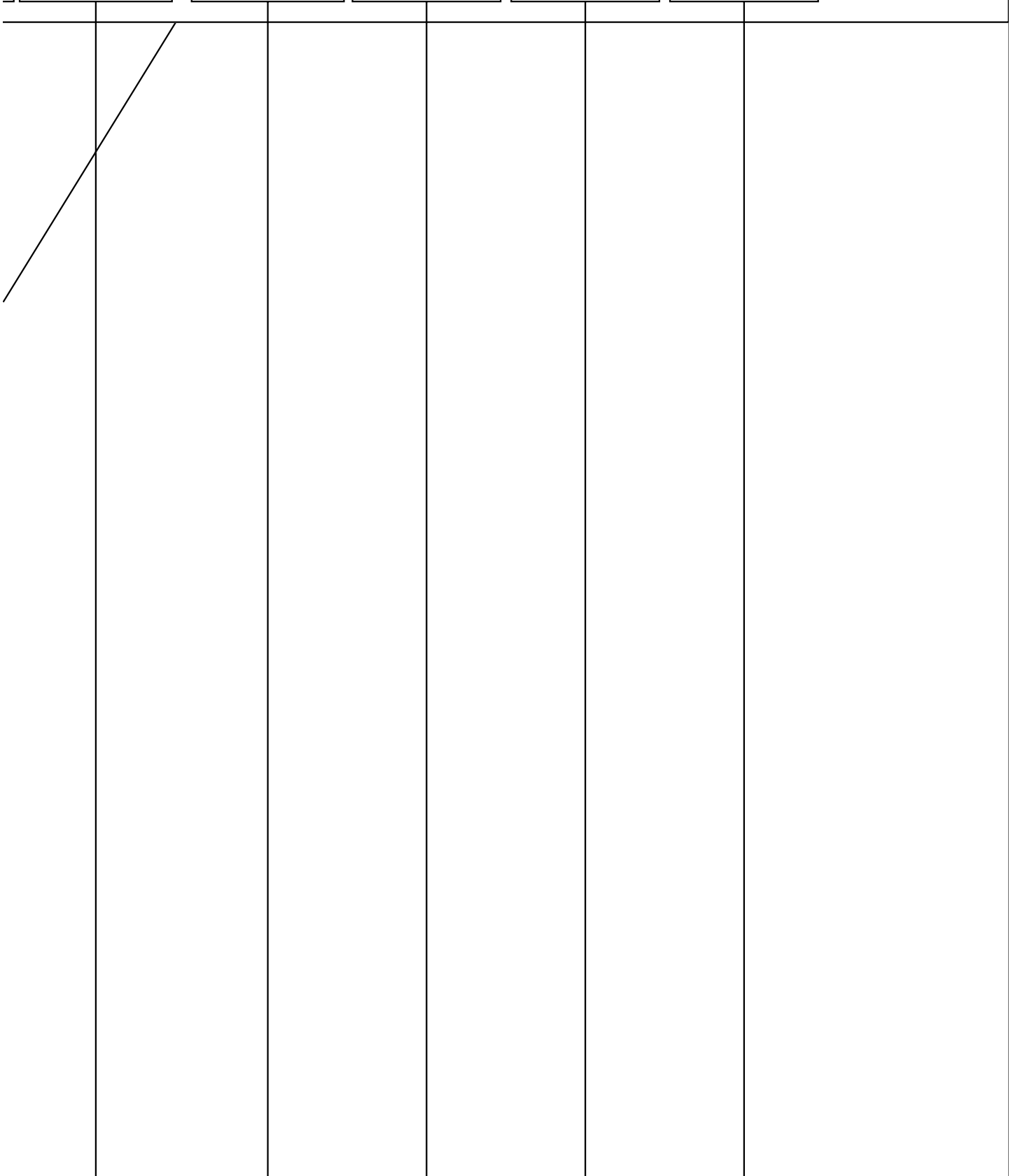






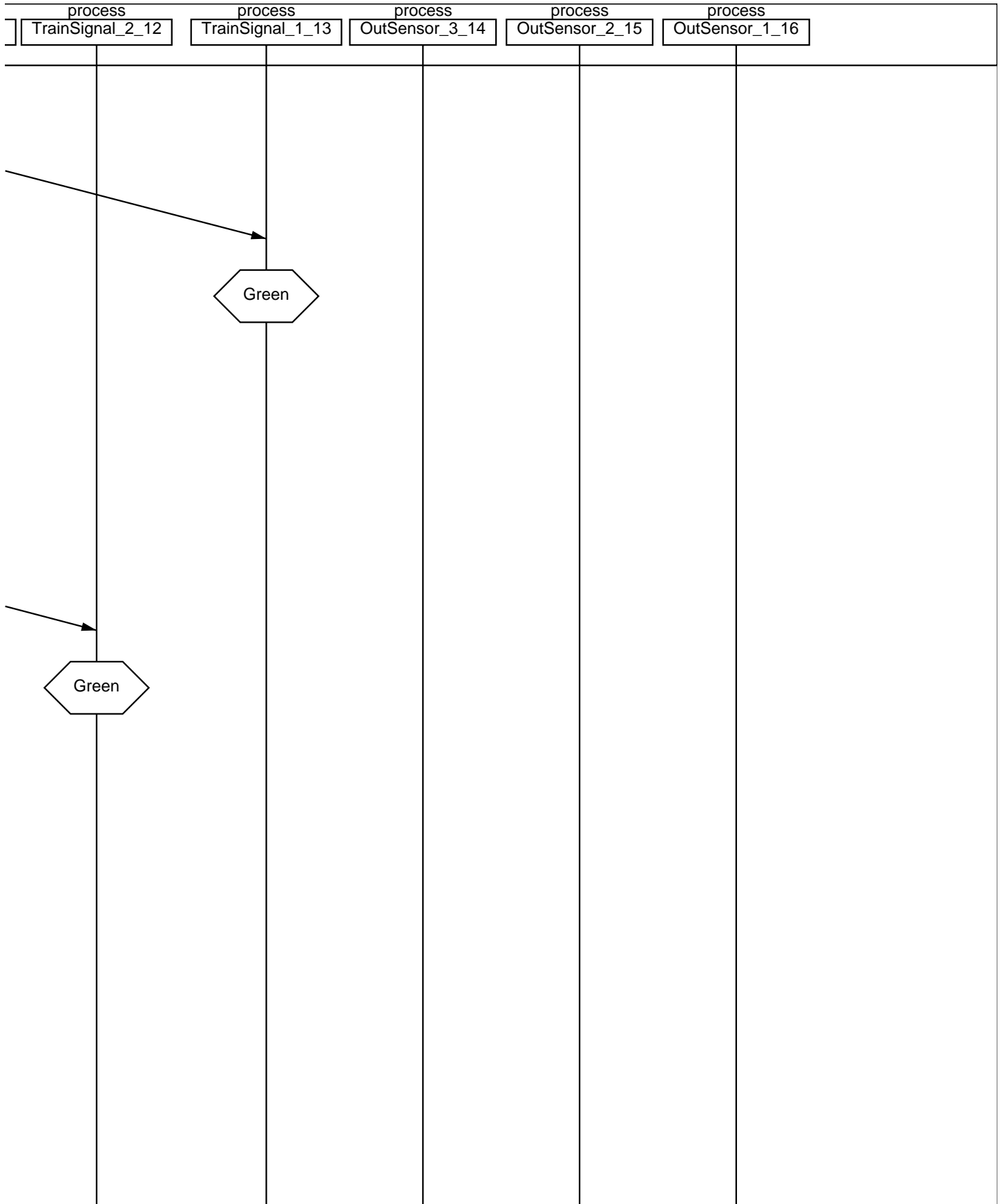


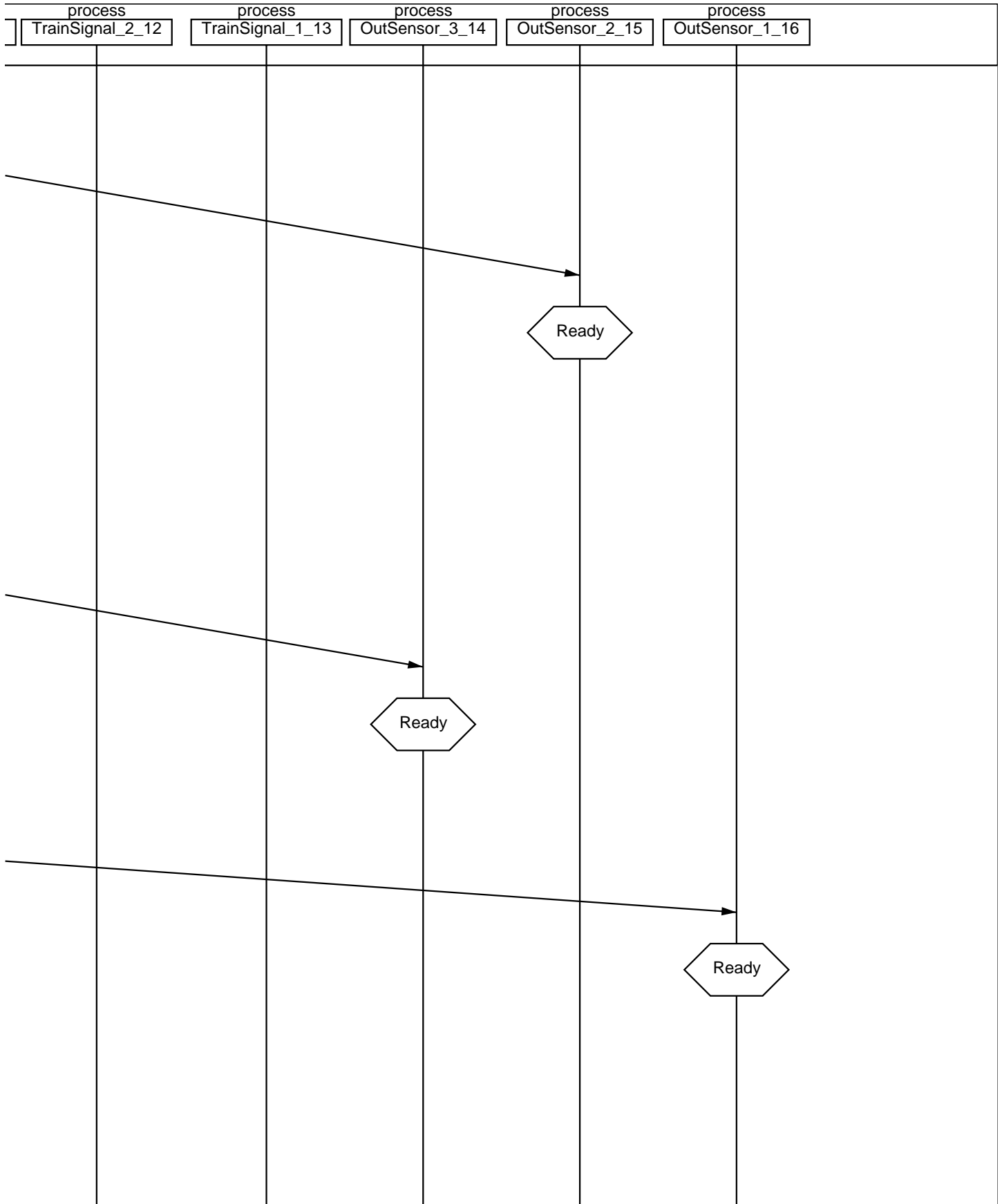
process	process	process	process	process
TrainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16



process	process	process	process	process	process	process
---------	---------	---------	---------	---------	---------	---------

TrainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16		
------------------	------------------	----------------	----------------	----------------	--	--





process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------

--	--	--	--	--

process	process	process	process	process	process	process
---------	---------	---------	---------	---------	---------	---------

TrainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16		
------------------	------------------	----------------	----------------	----------------	--	--

process	process	process	process	process	process	process
---------	---------	---------	---------	---------	---------	---------

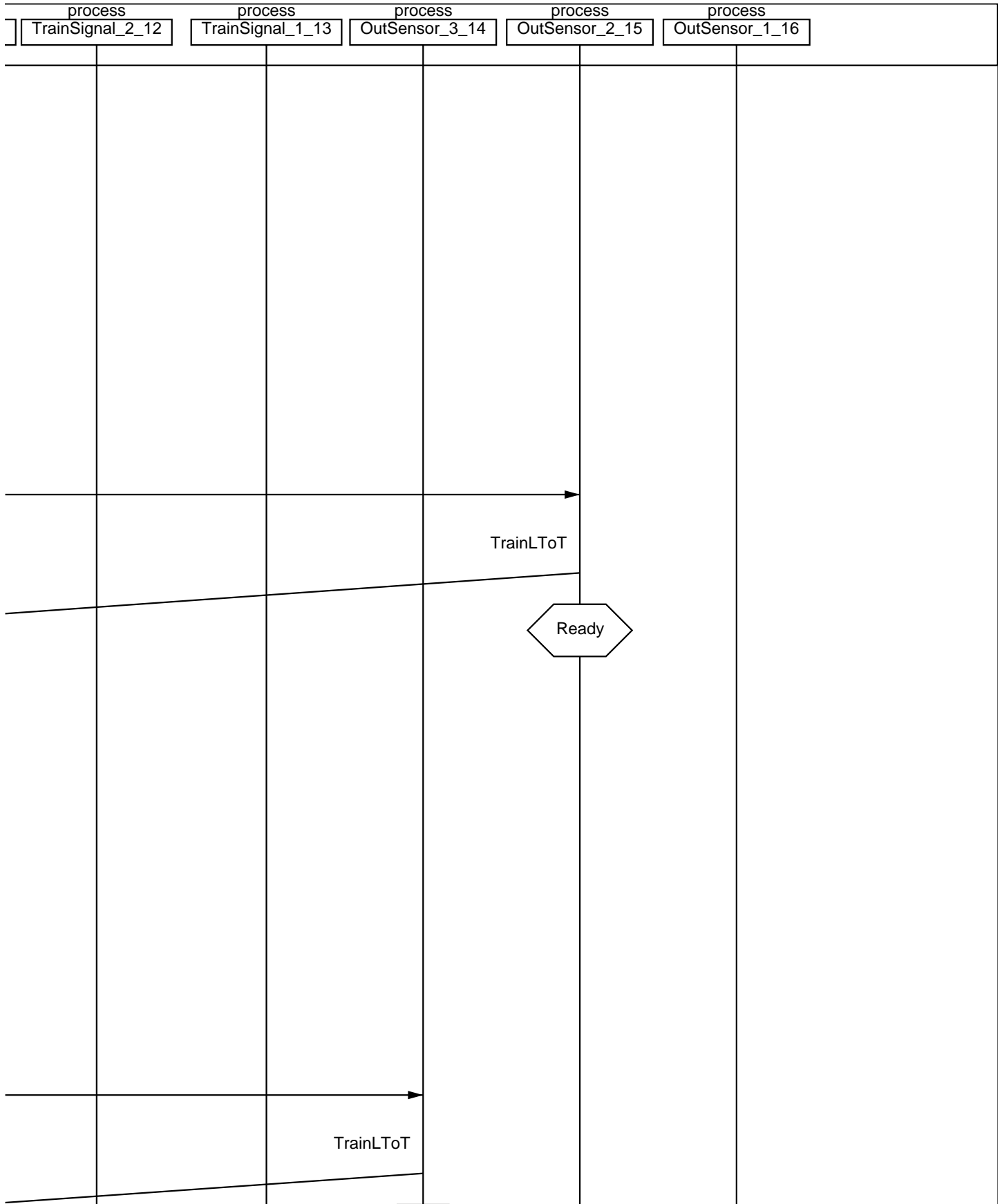
TrainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16		
------------------	------------------	----------------	----------------	----------------	--	--

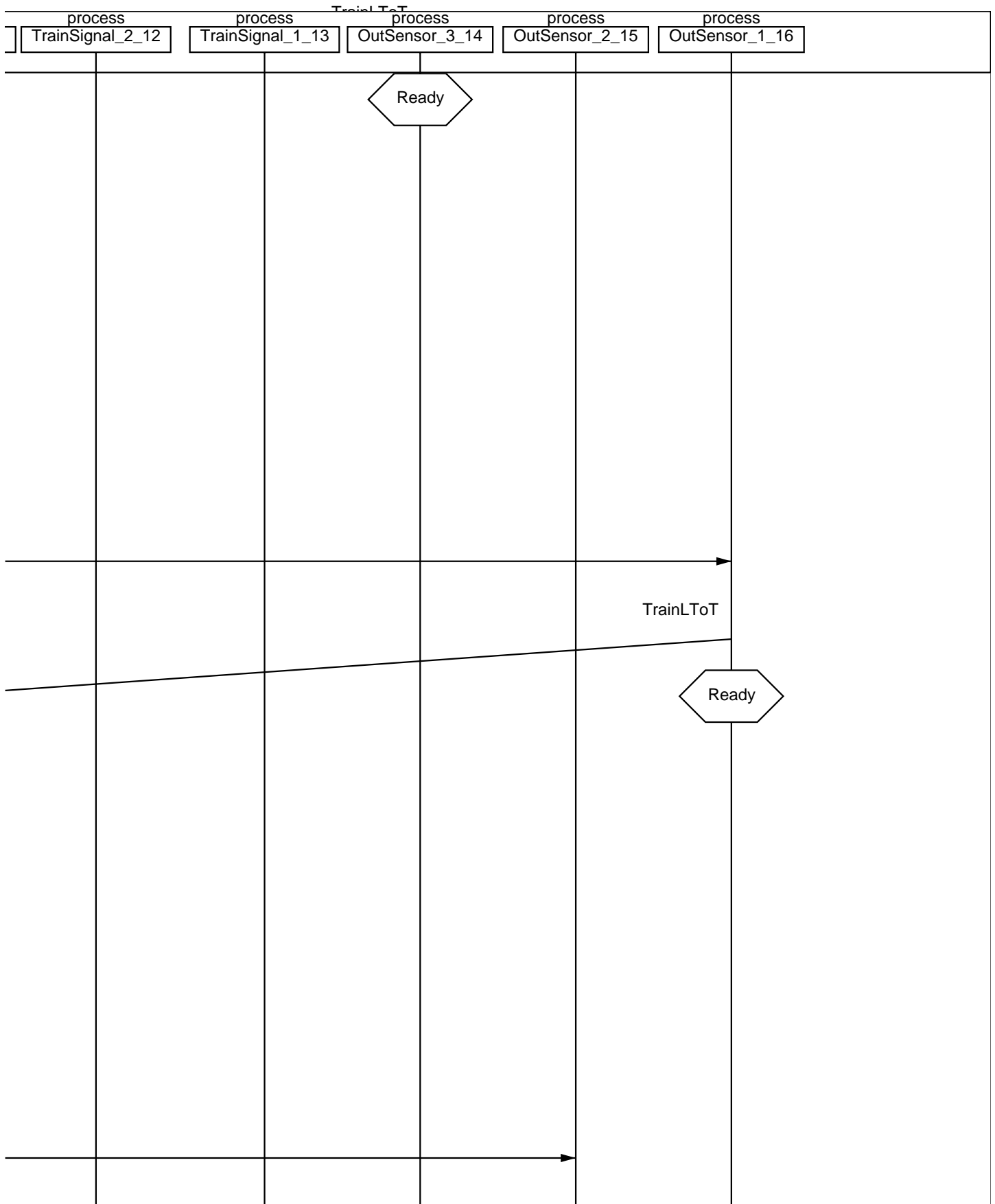
process	process	process	process	process	process	process
---------	---------	---------	---------	---------	---------	---------

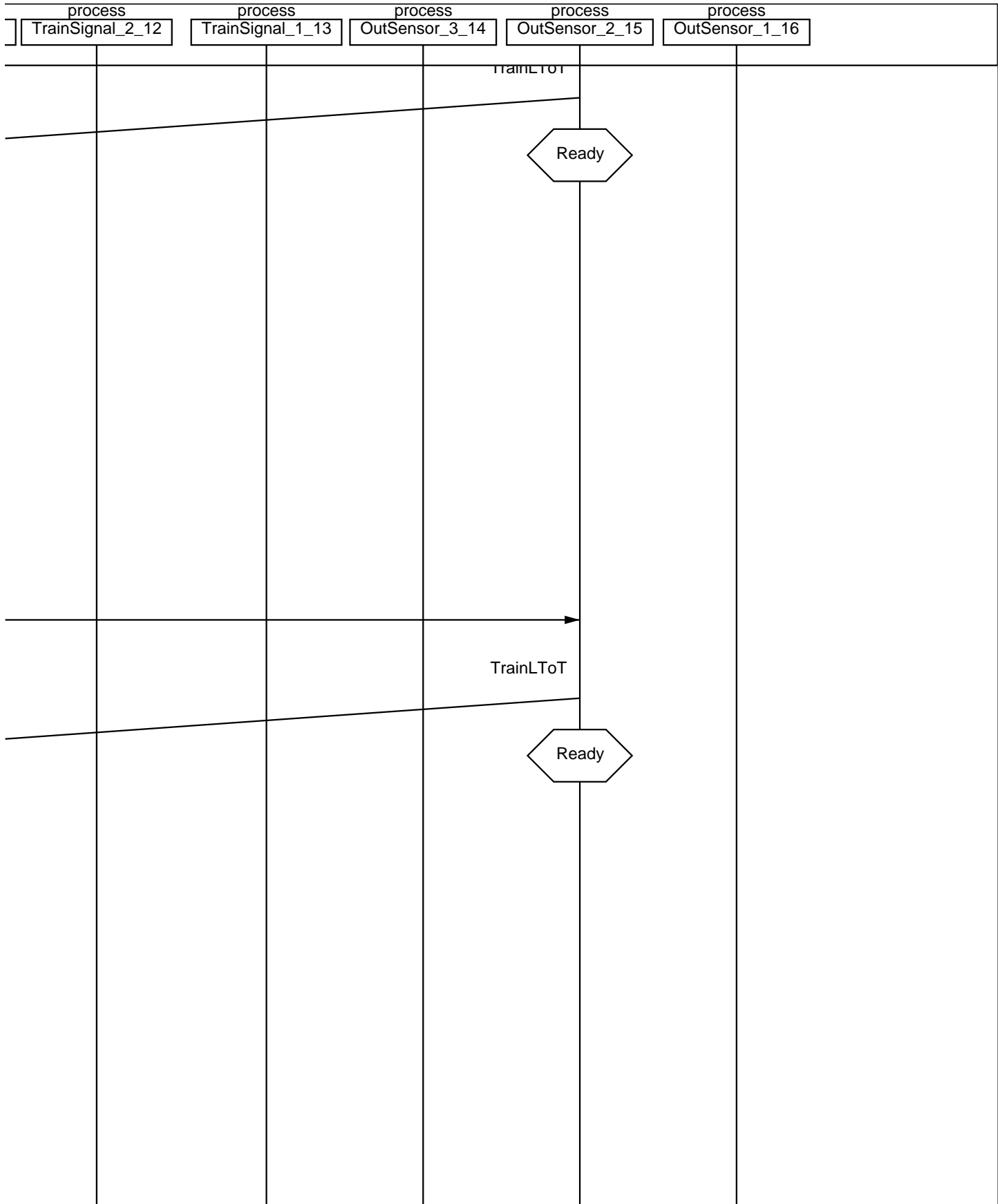
TrainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16		
------------------	------------------	----------------	----------------	----------------	--	--

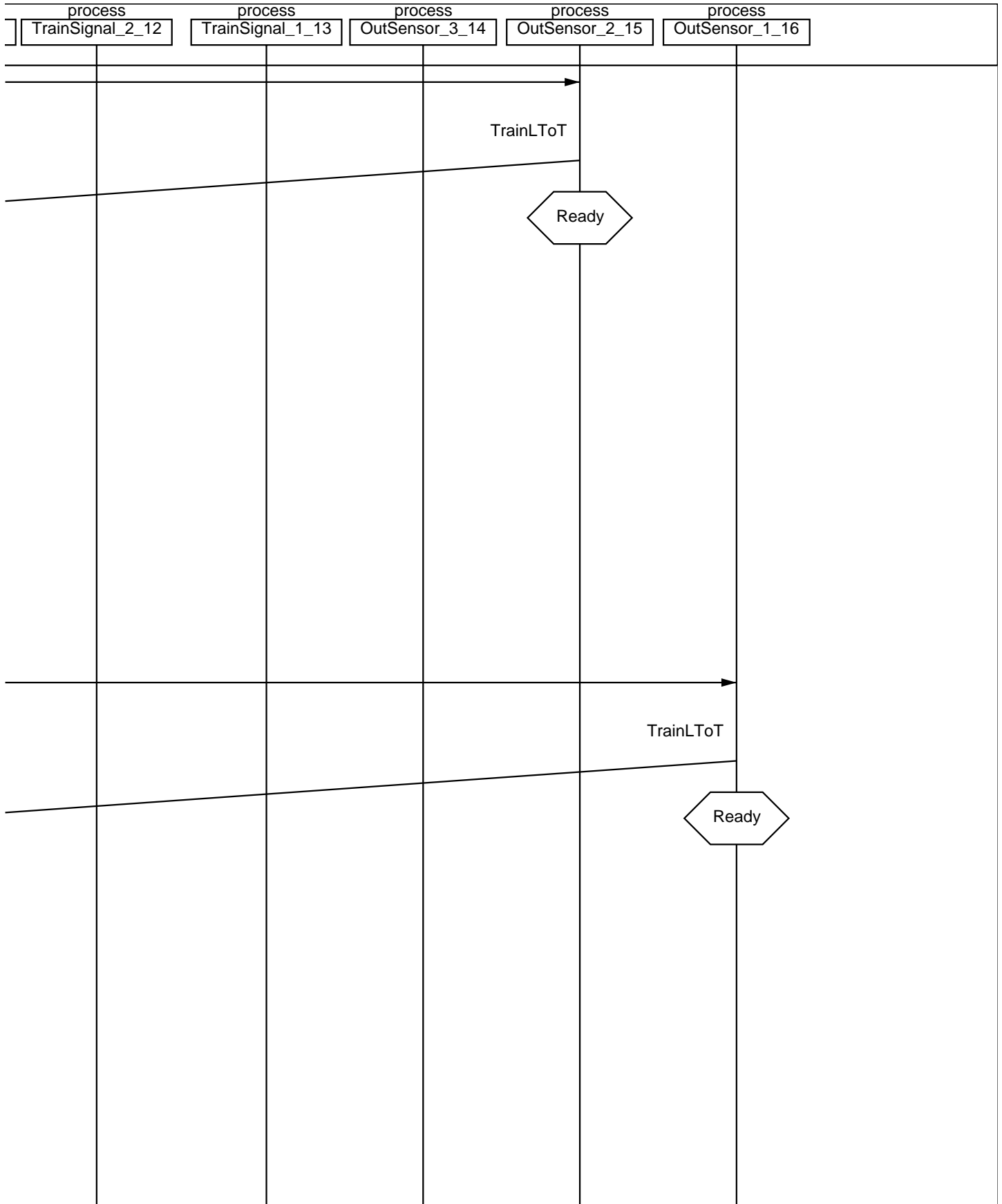
process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------

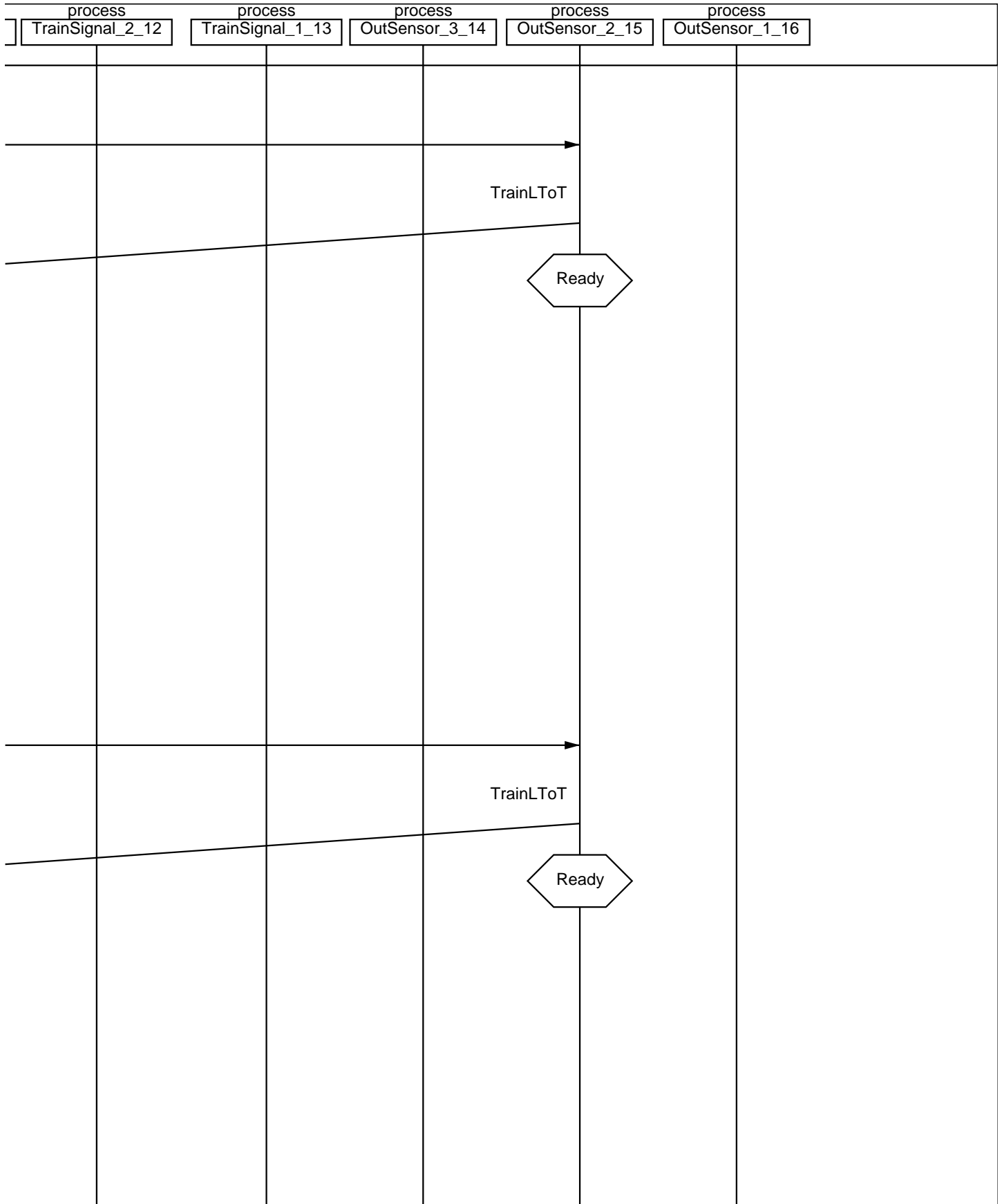
--	--	--	--	--

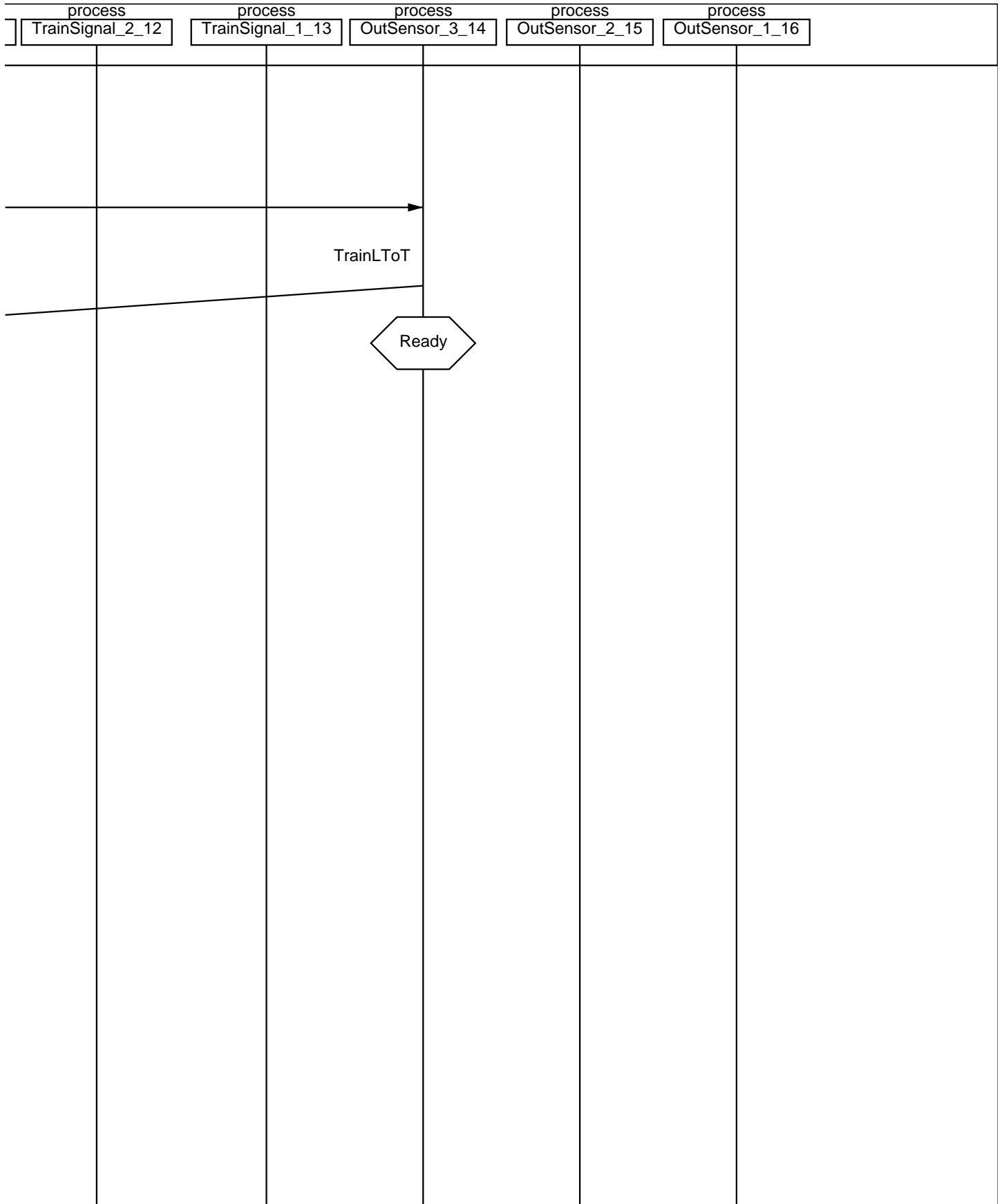


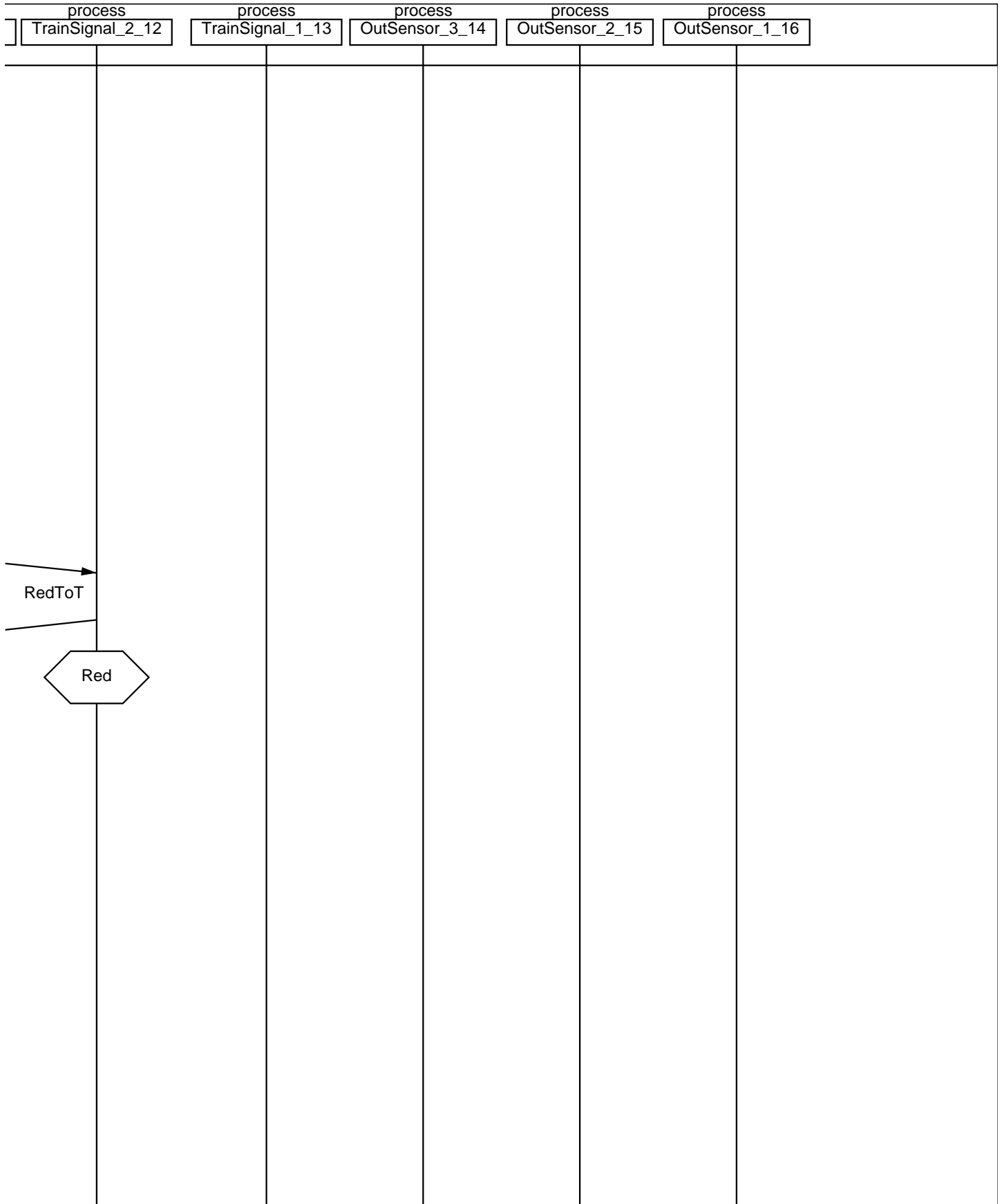


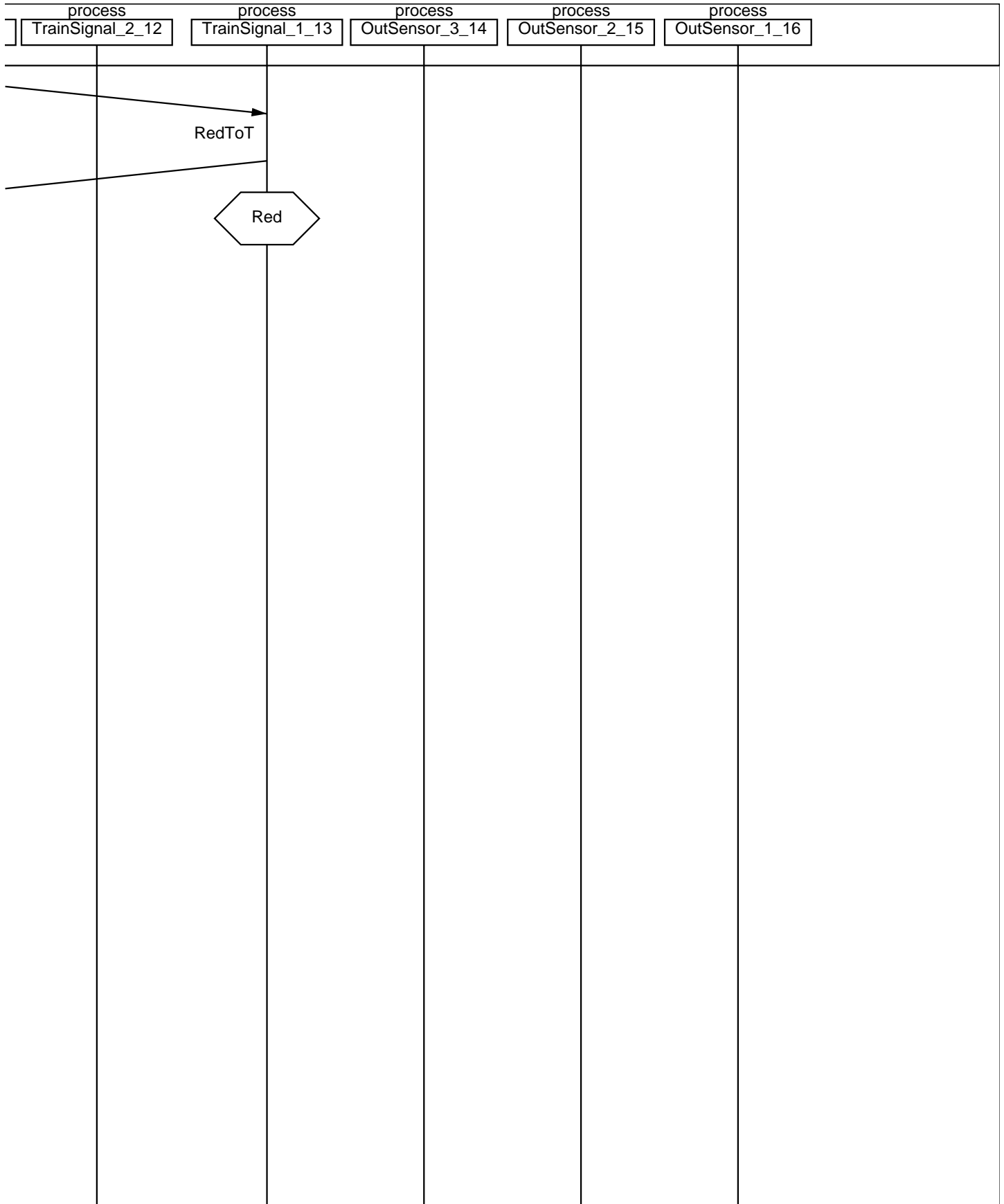






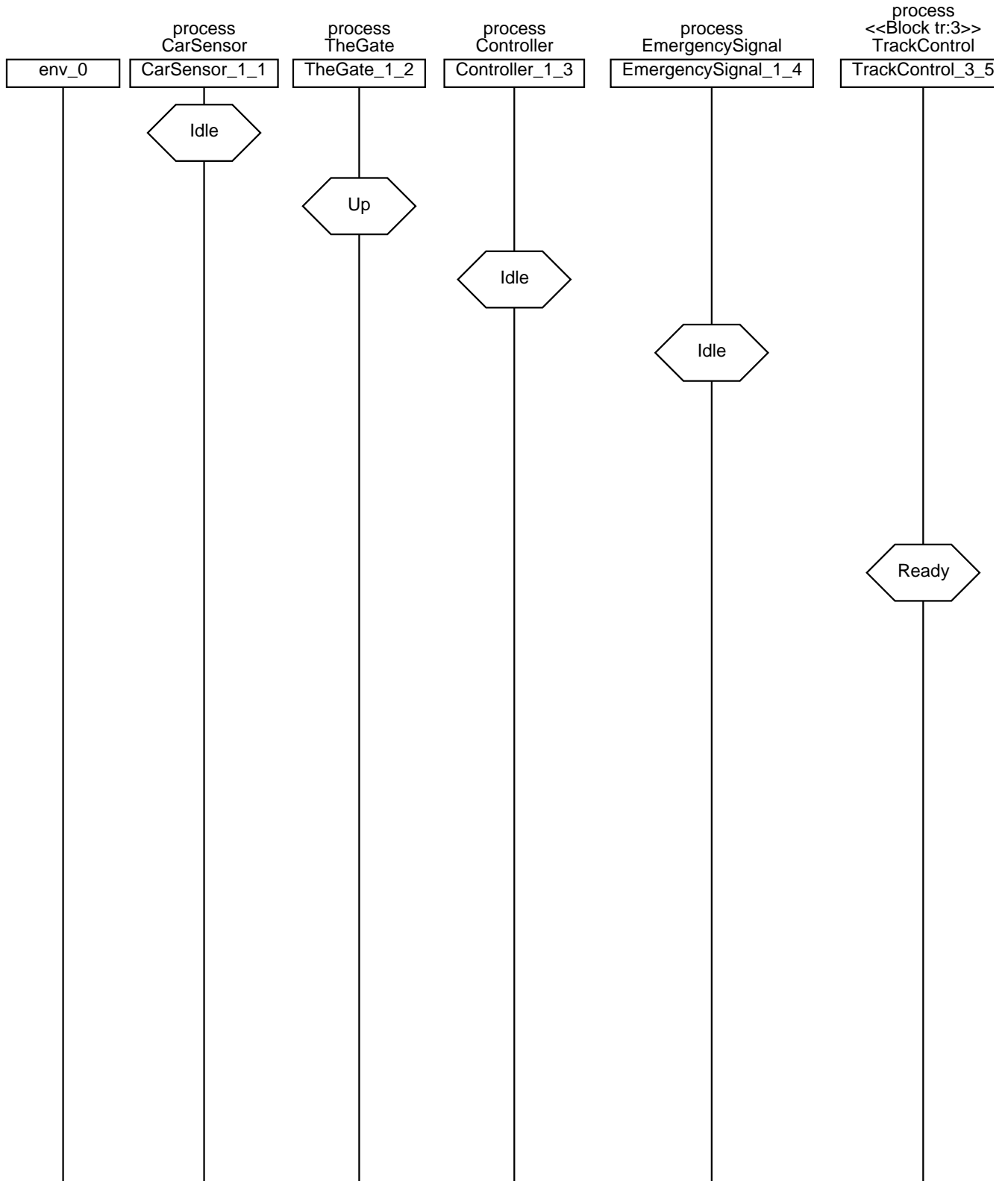


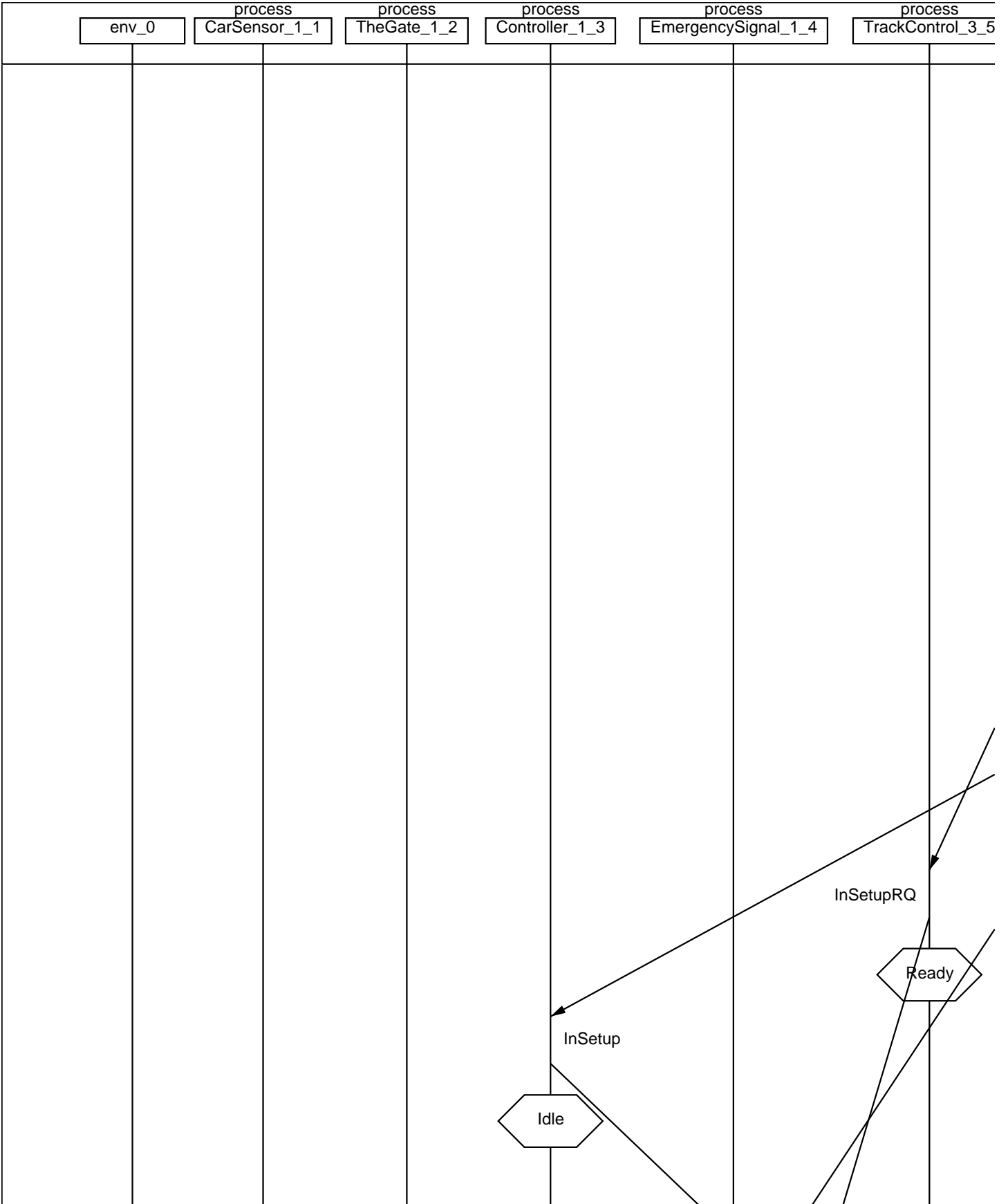


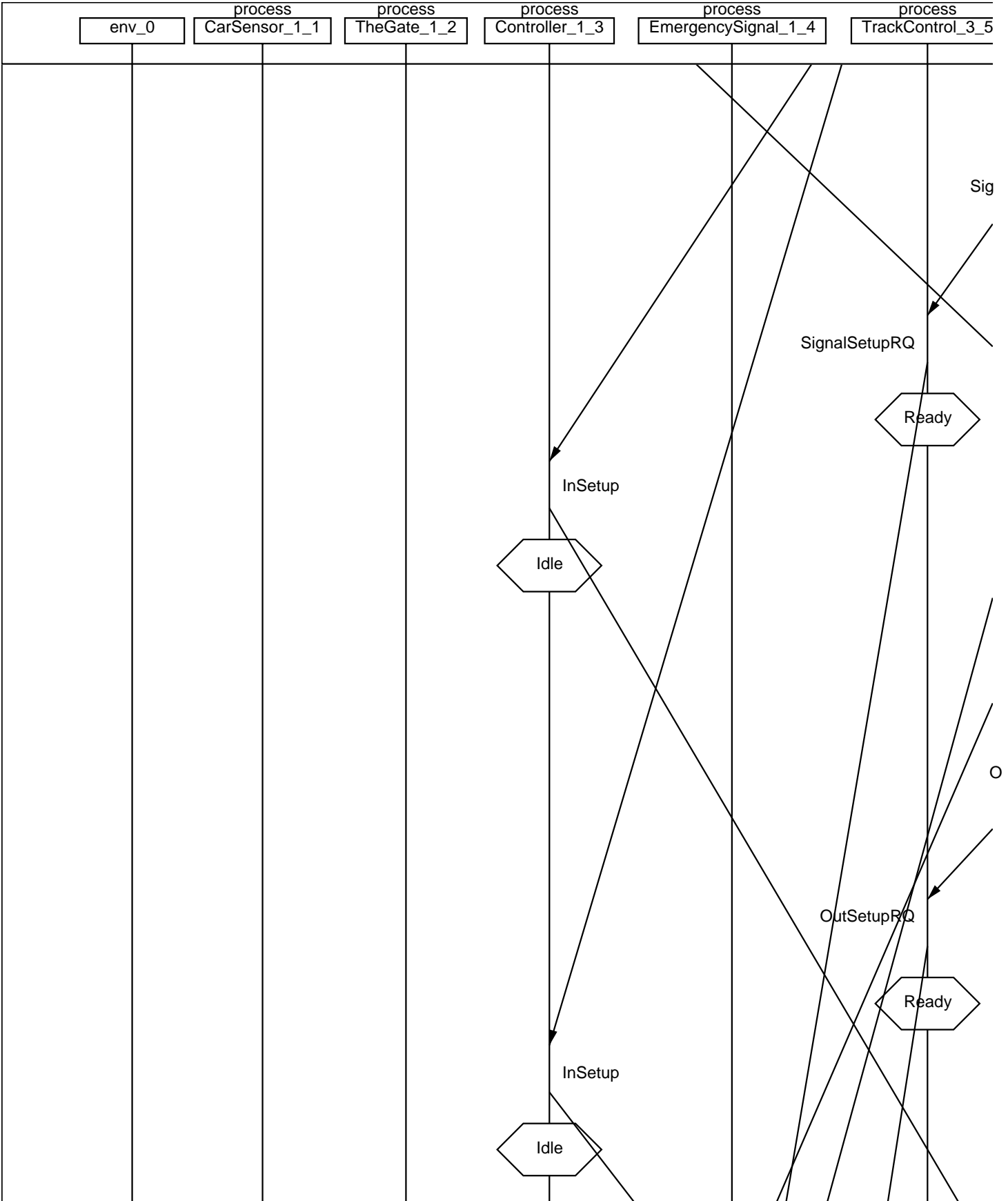


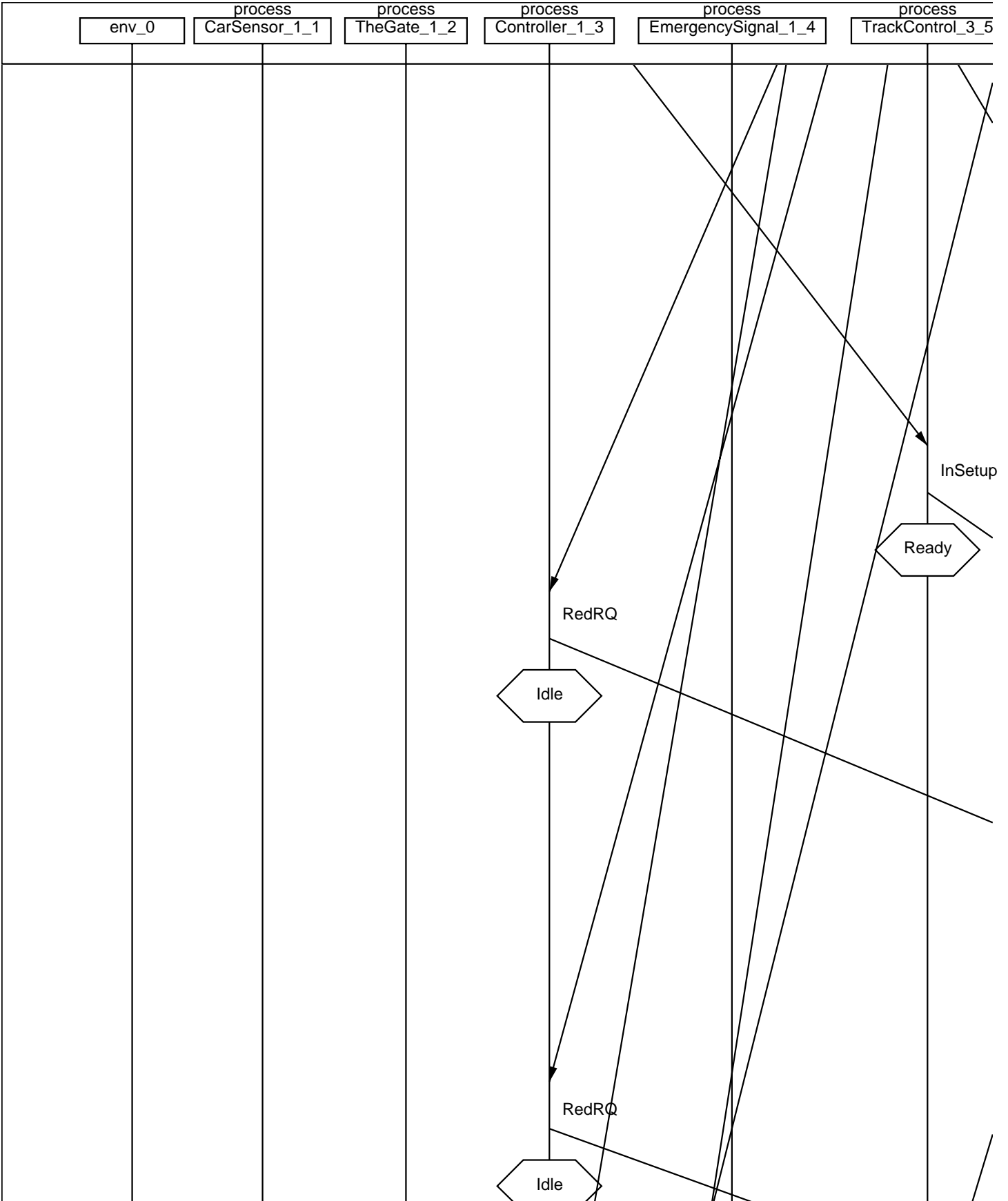
MSC CompleteMSC_TestCaseD_Strategy3

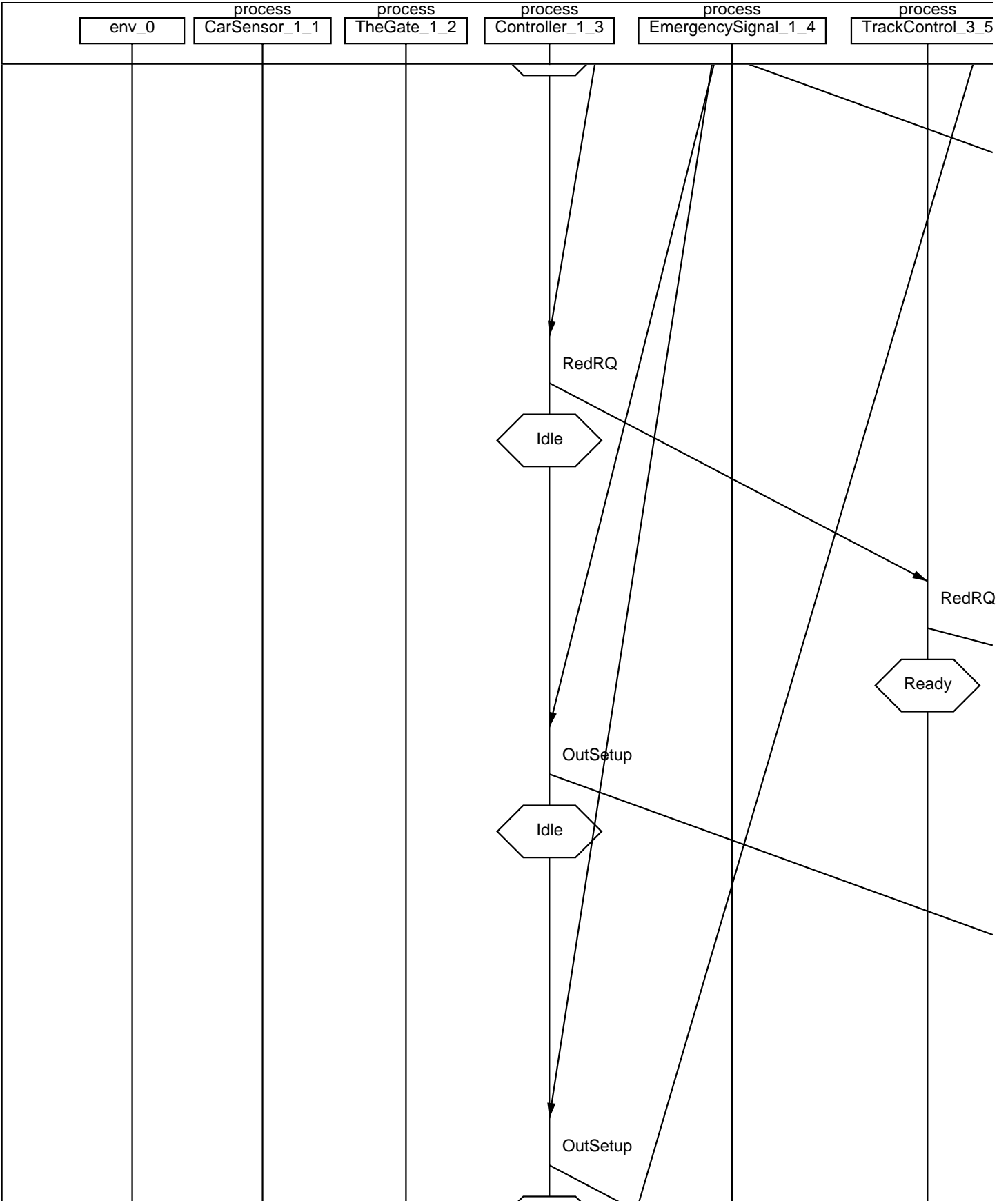
Simulation trace
generated by
SDL Simulator 4.3

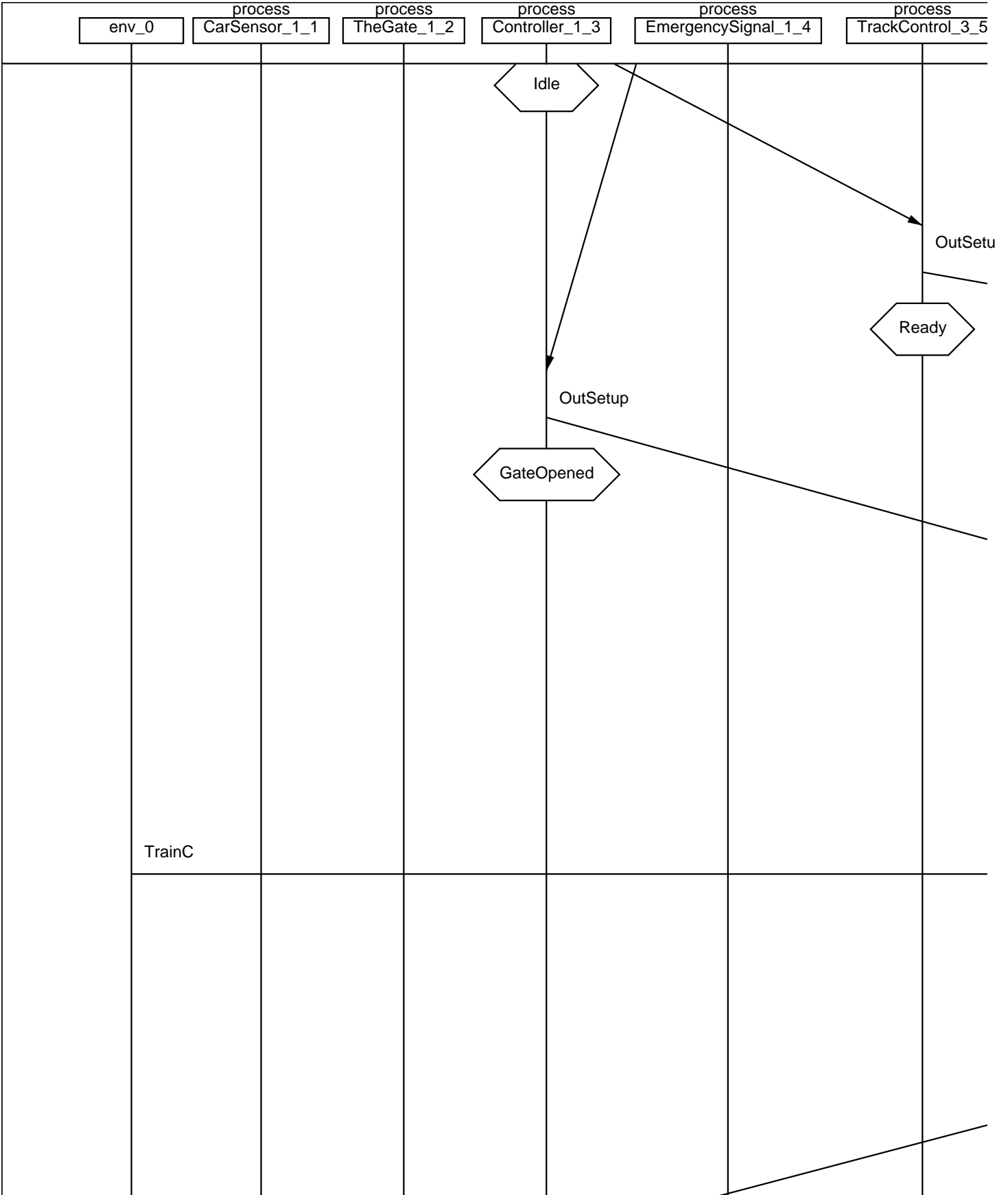


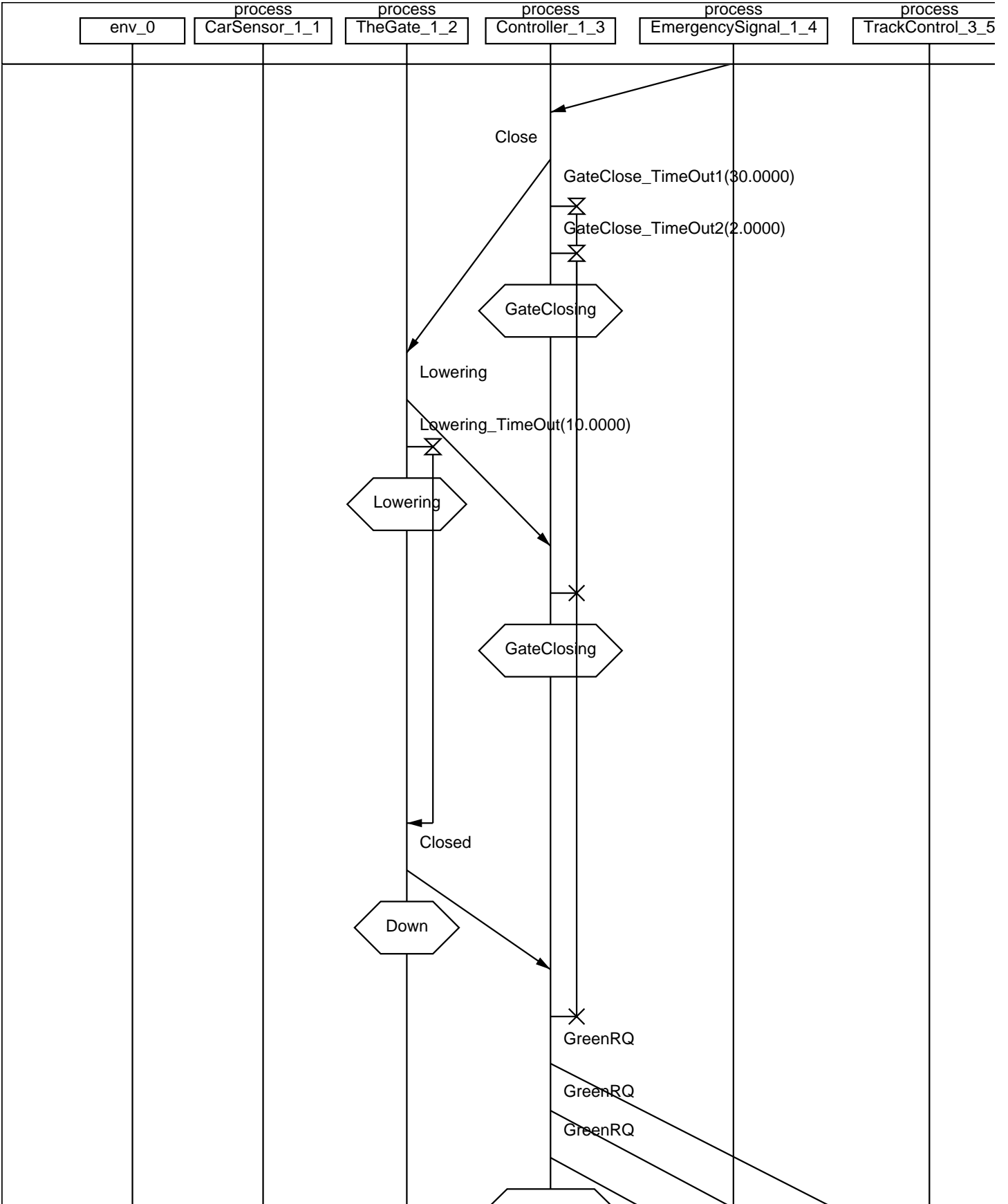


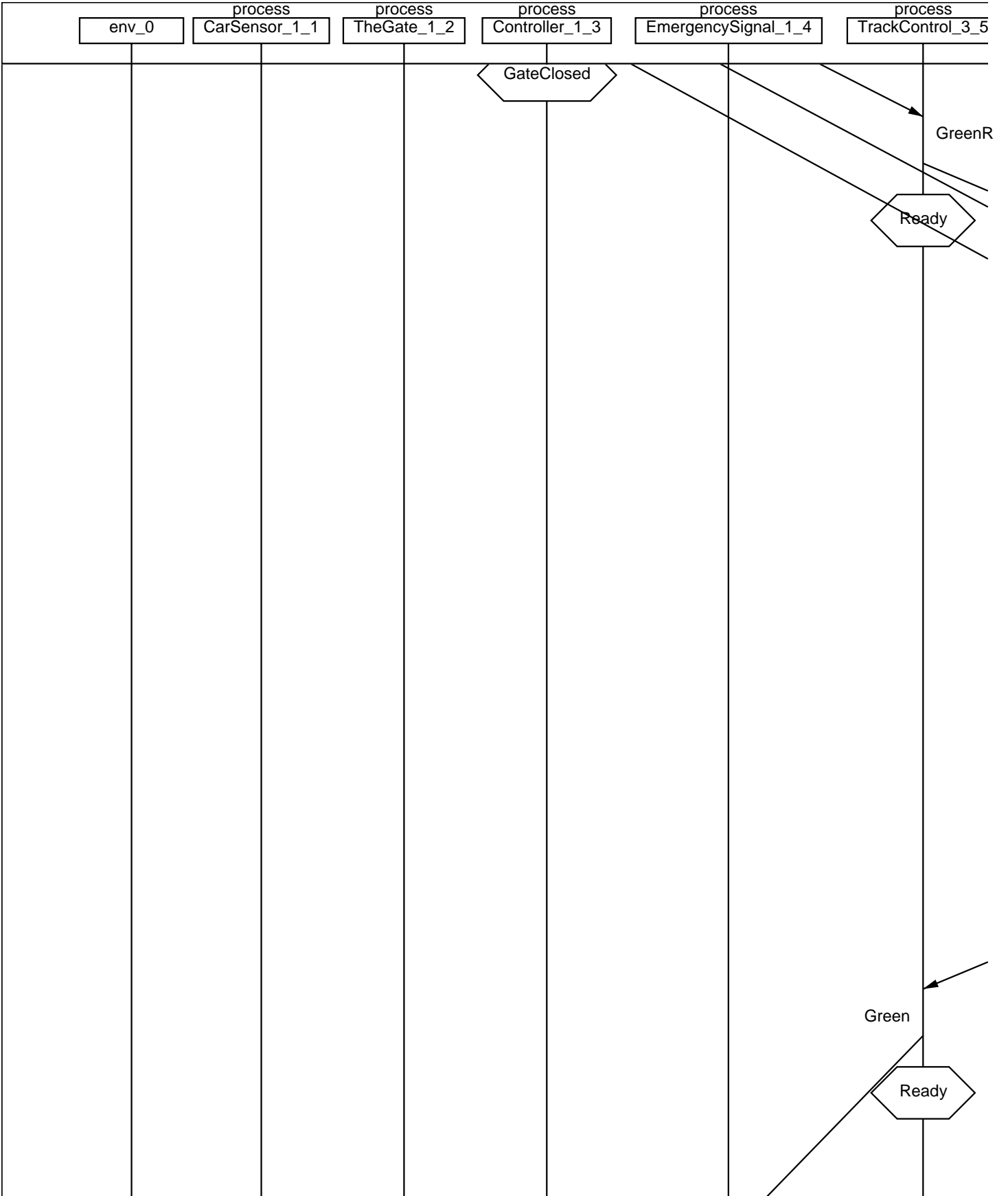


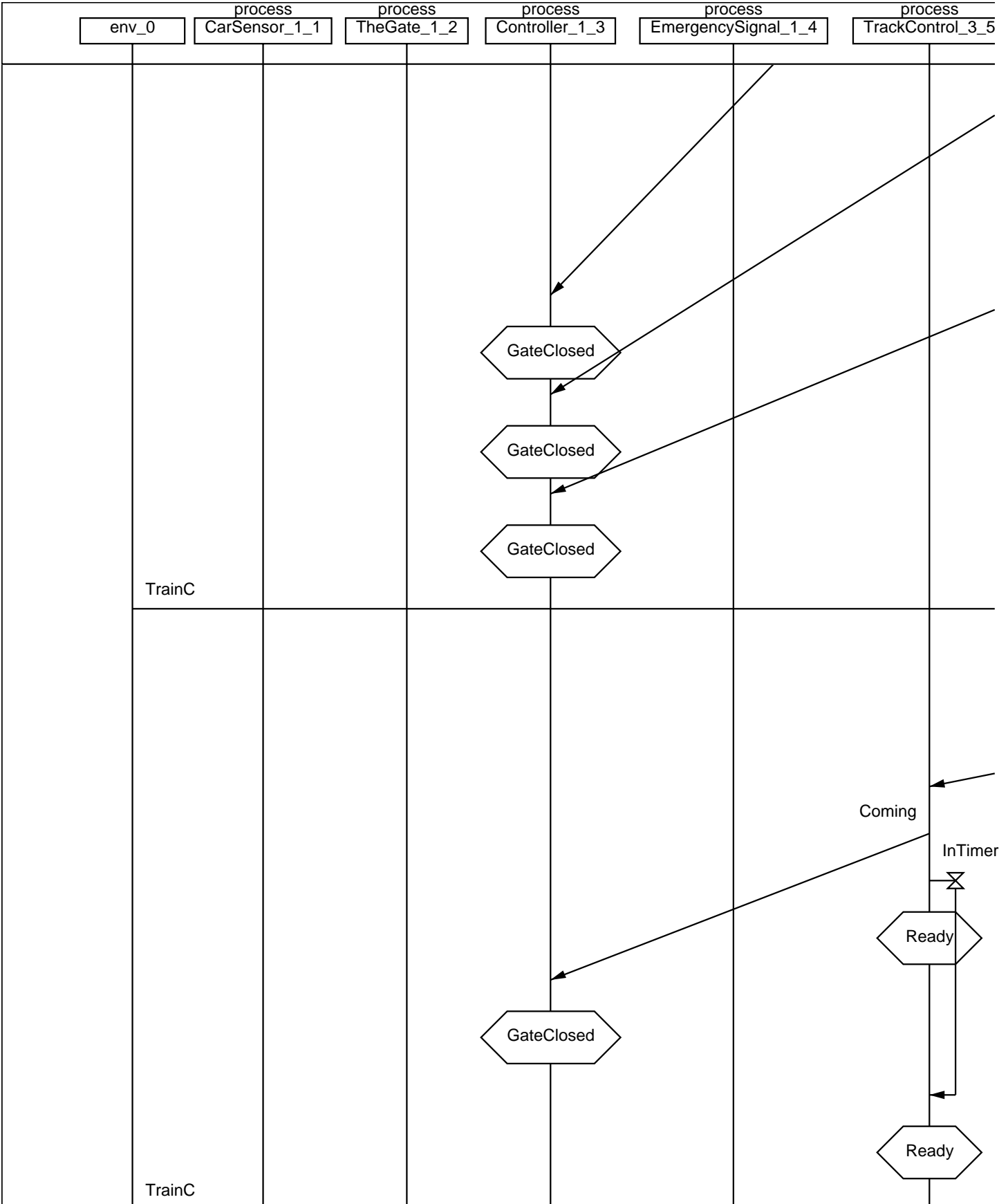


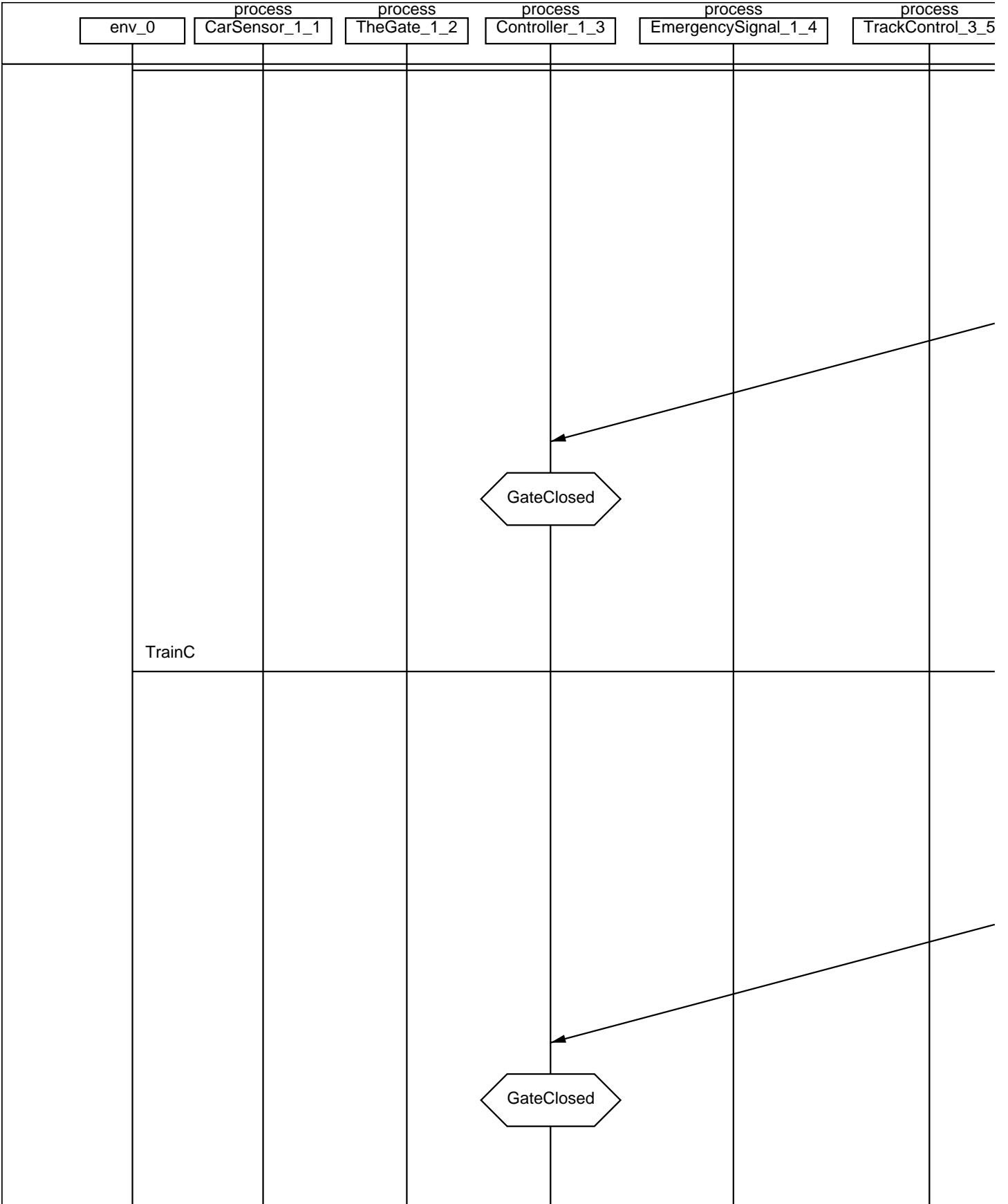


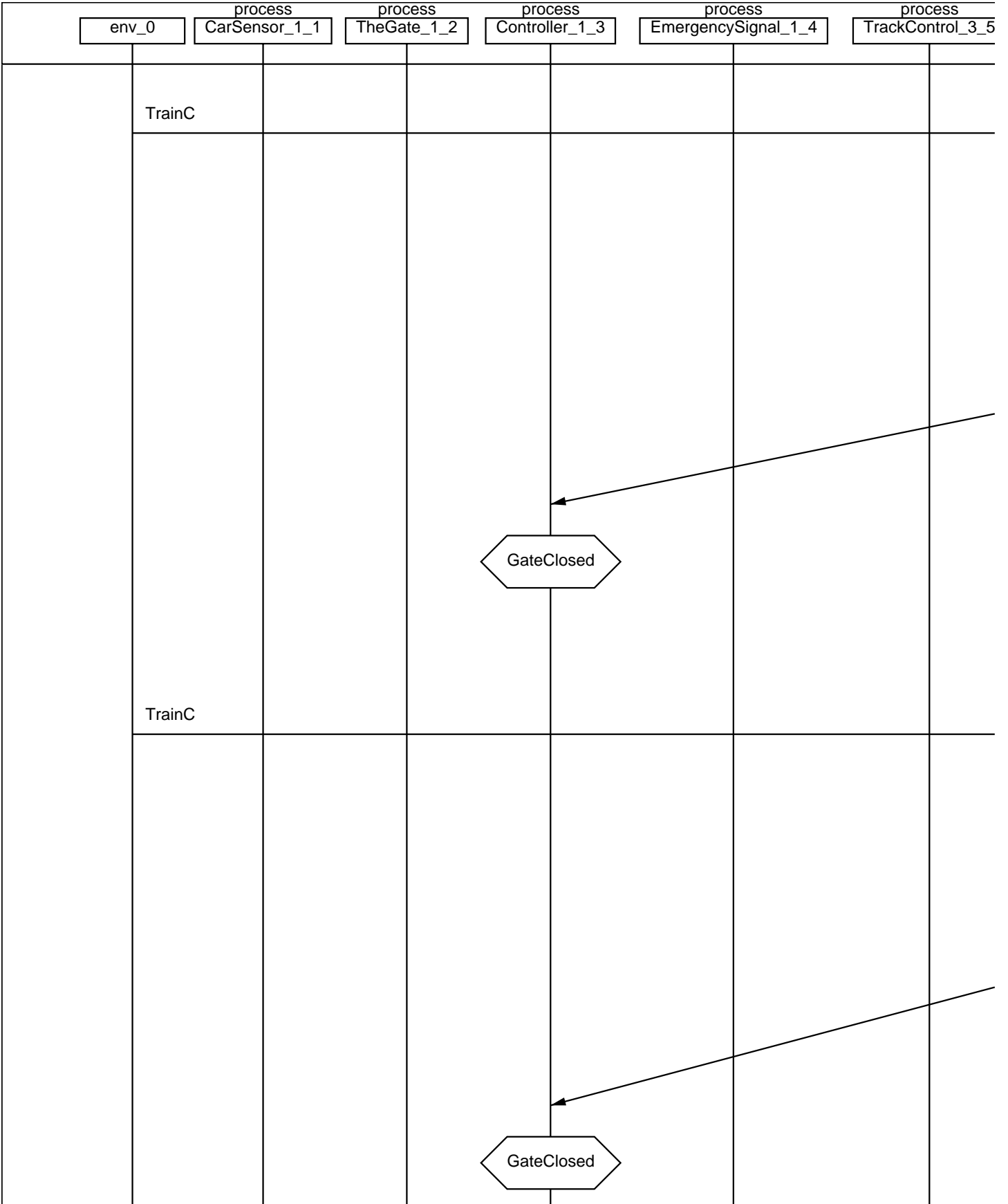


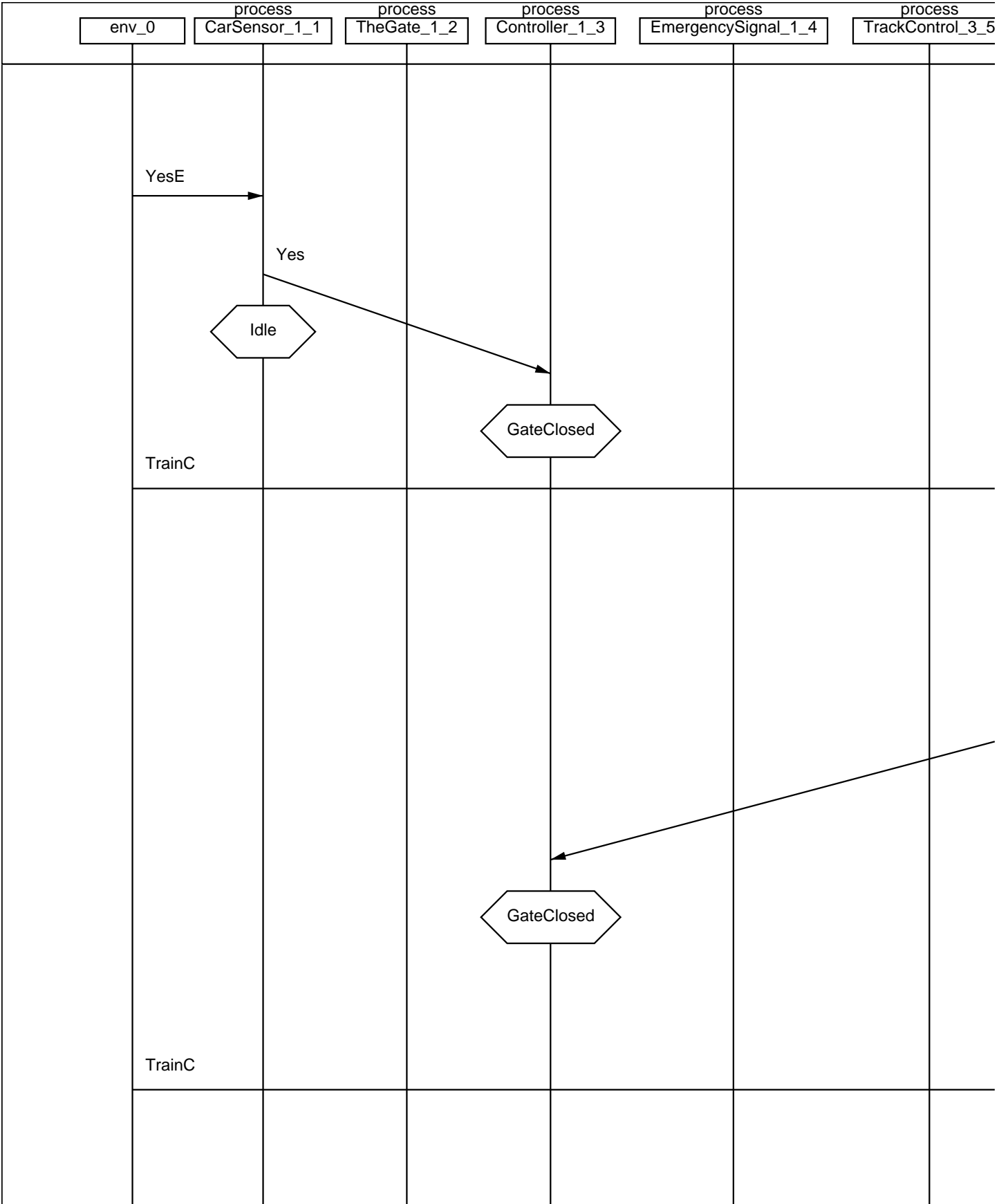


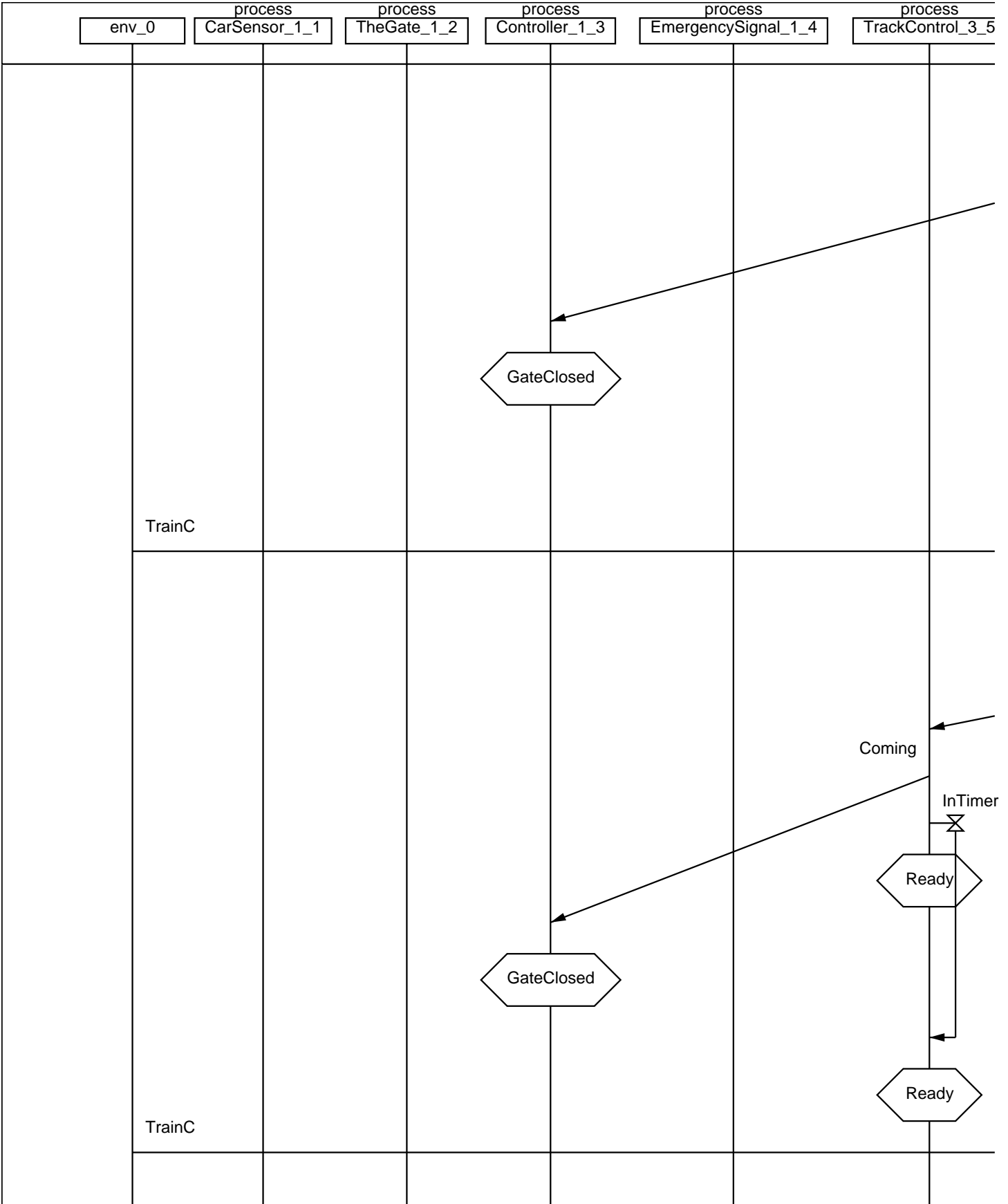


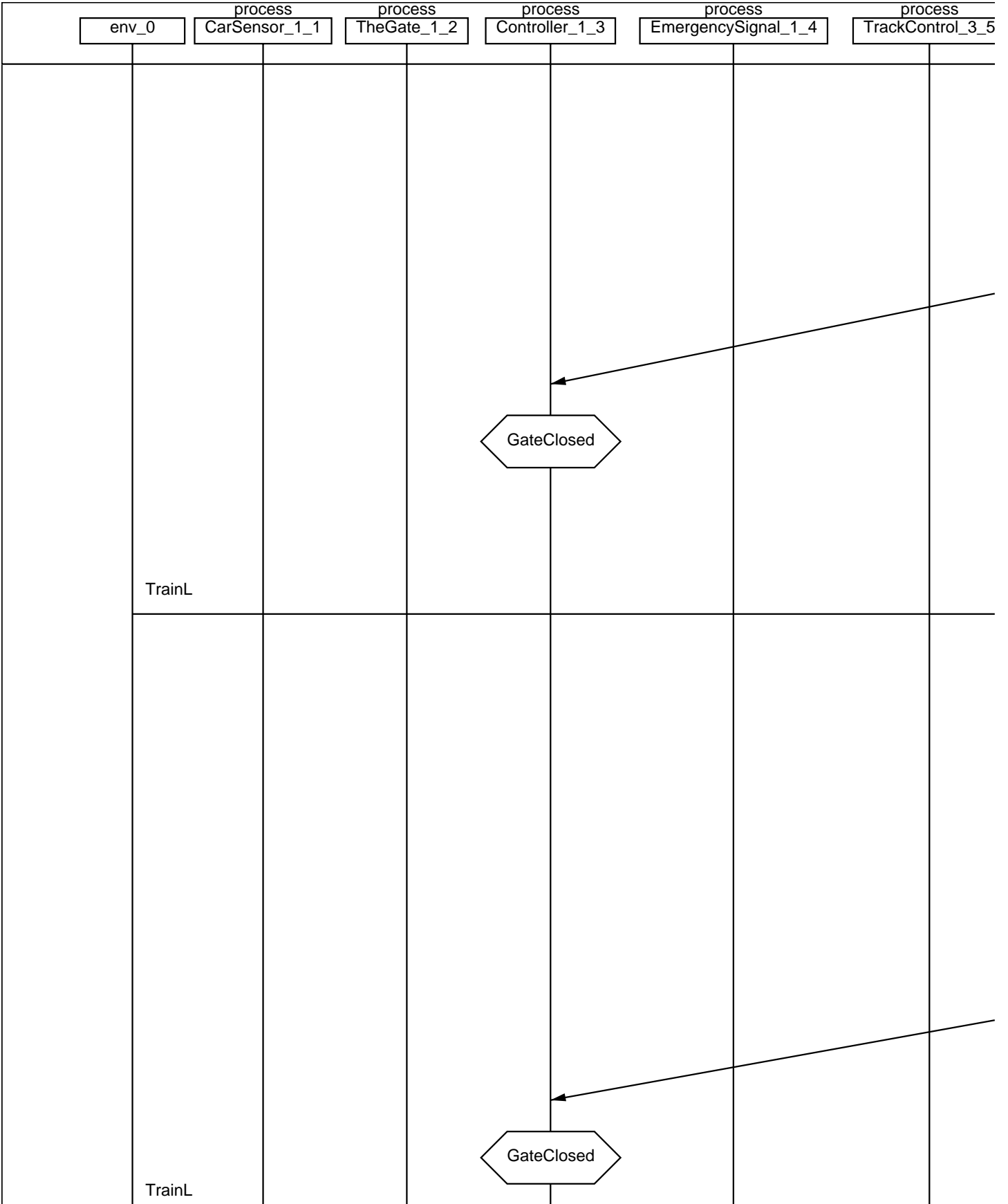


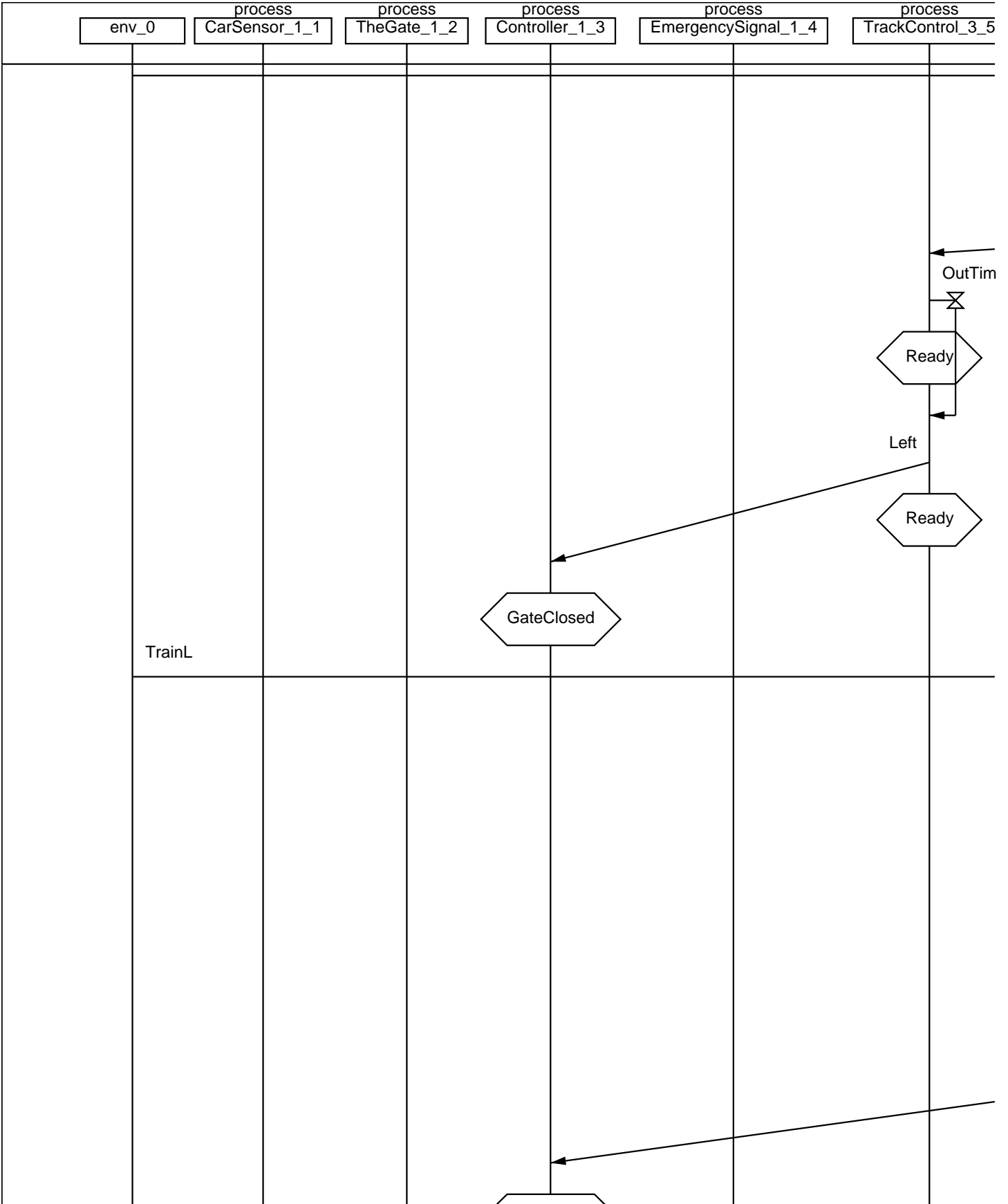


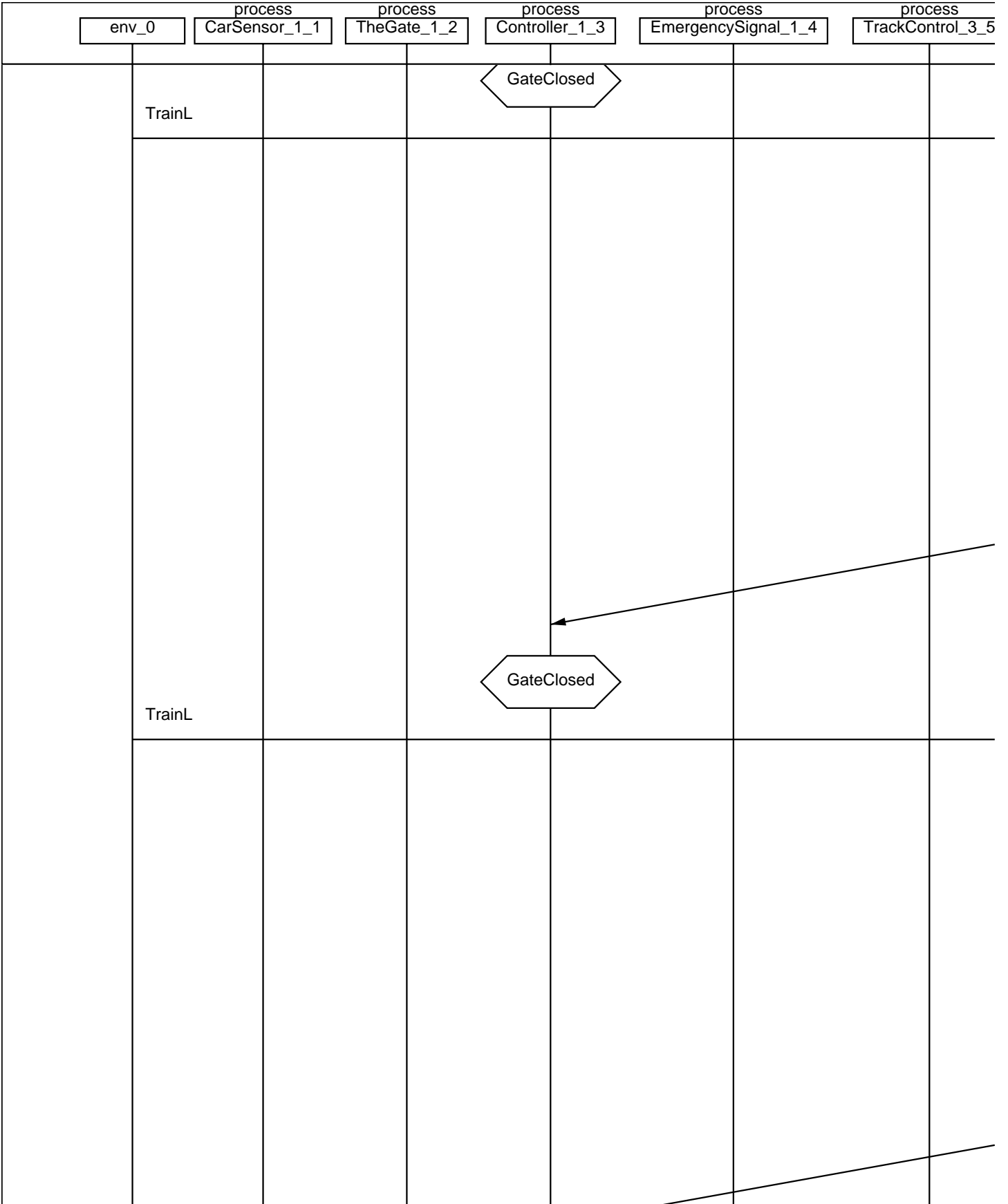


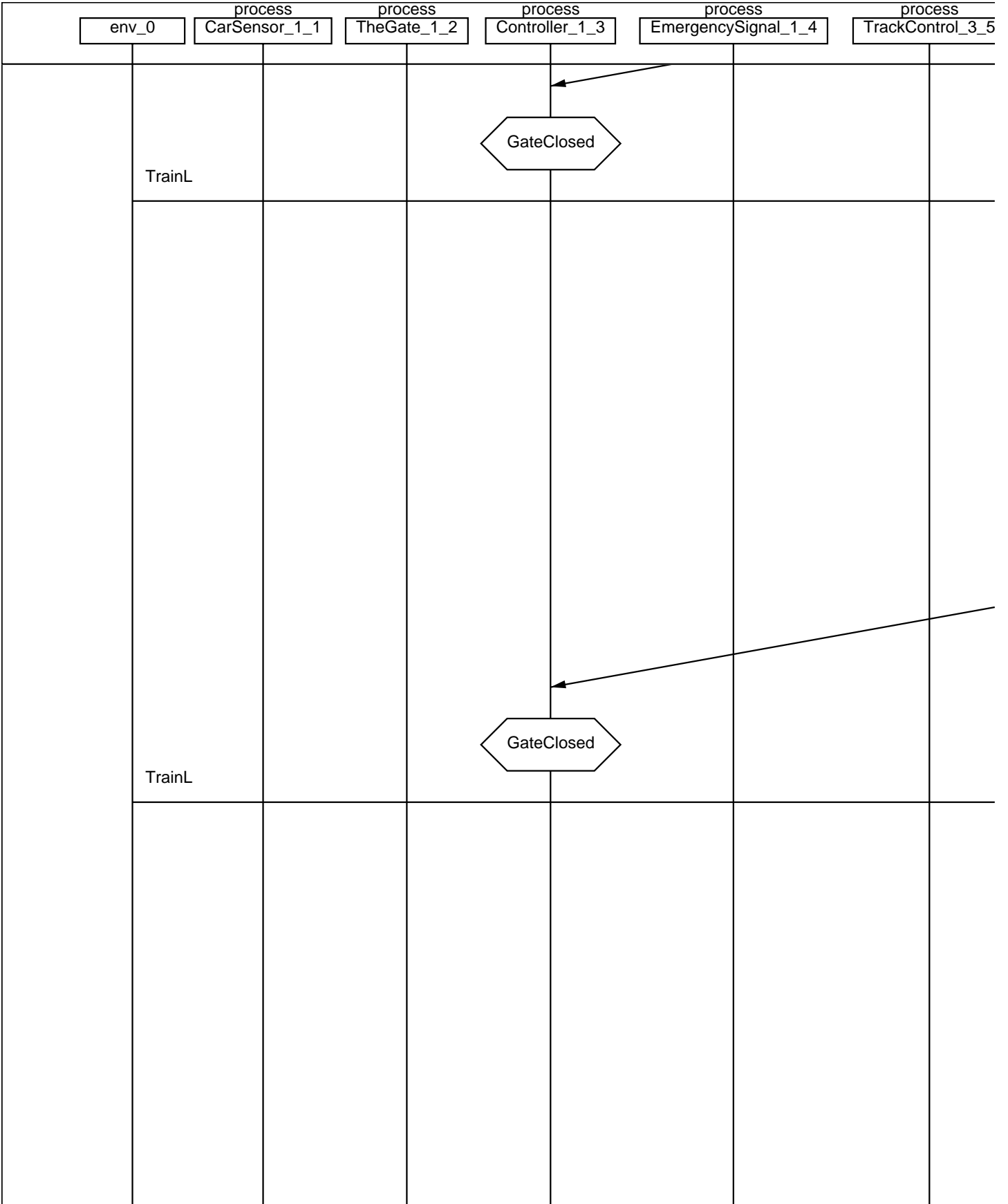


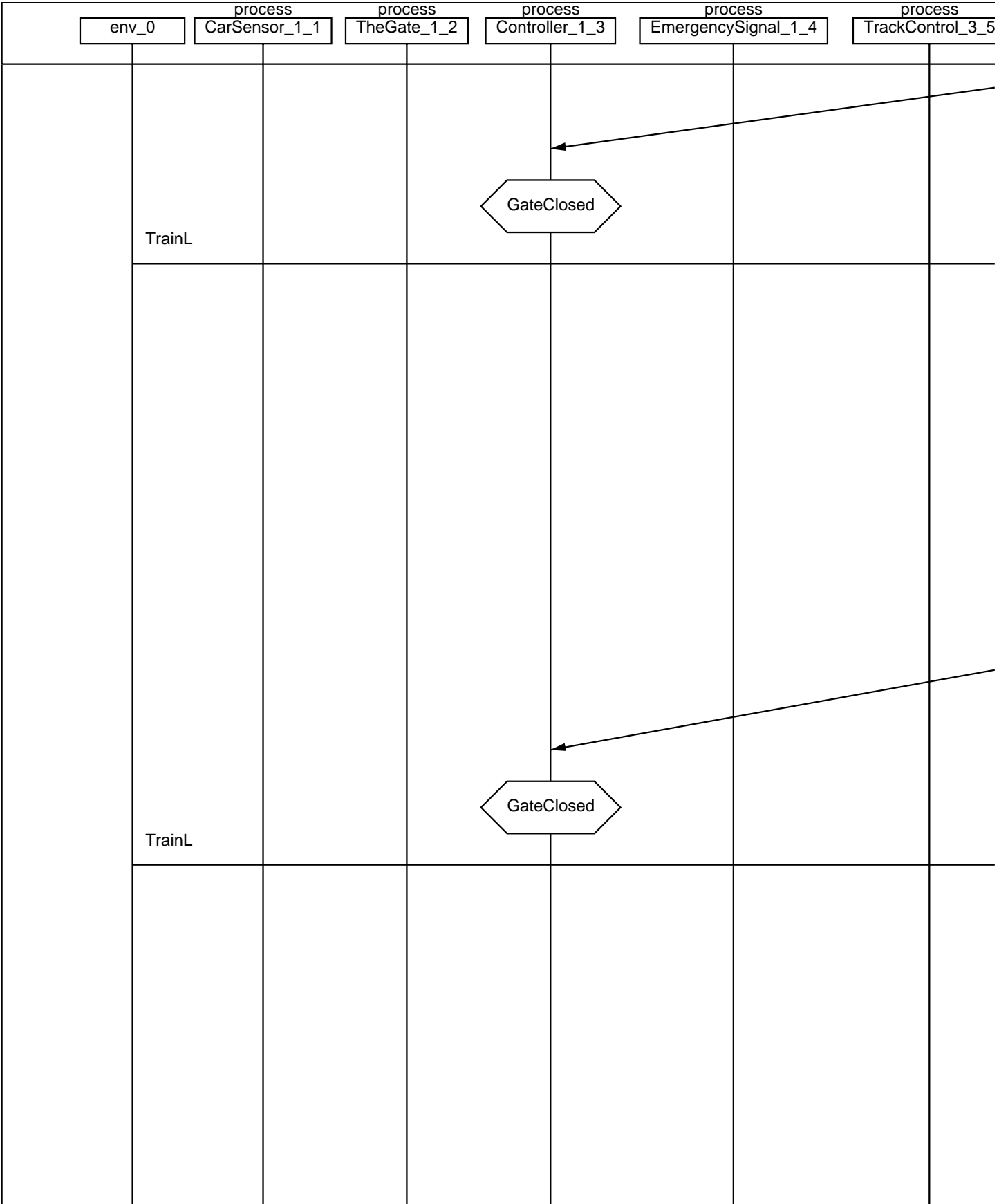


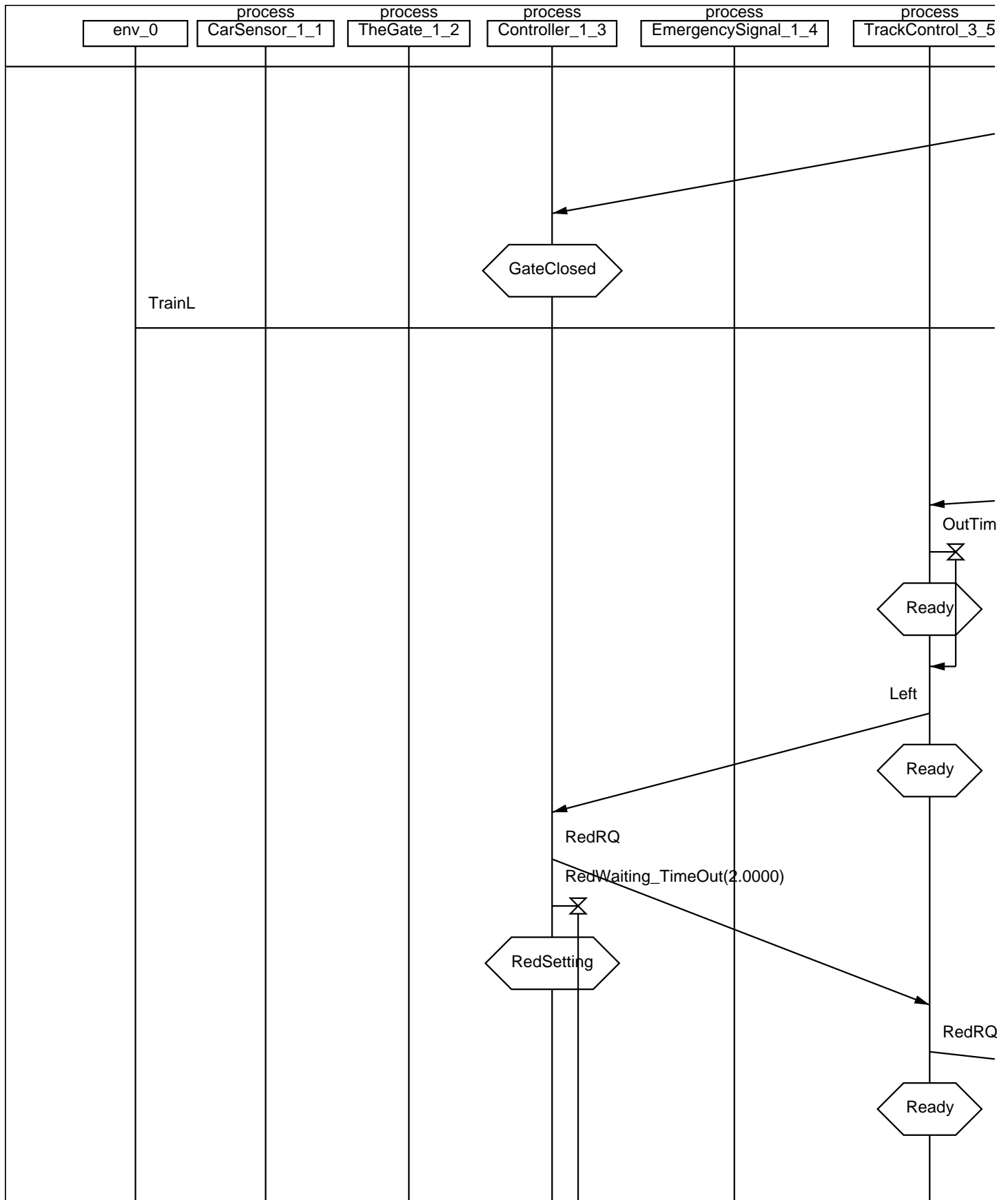


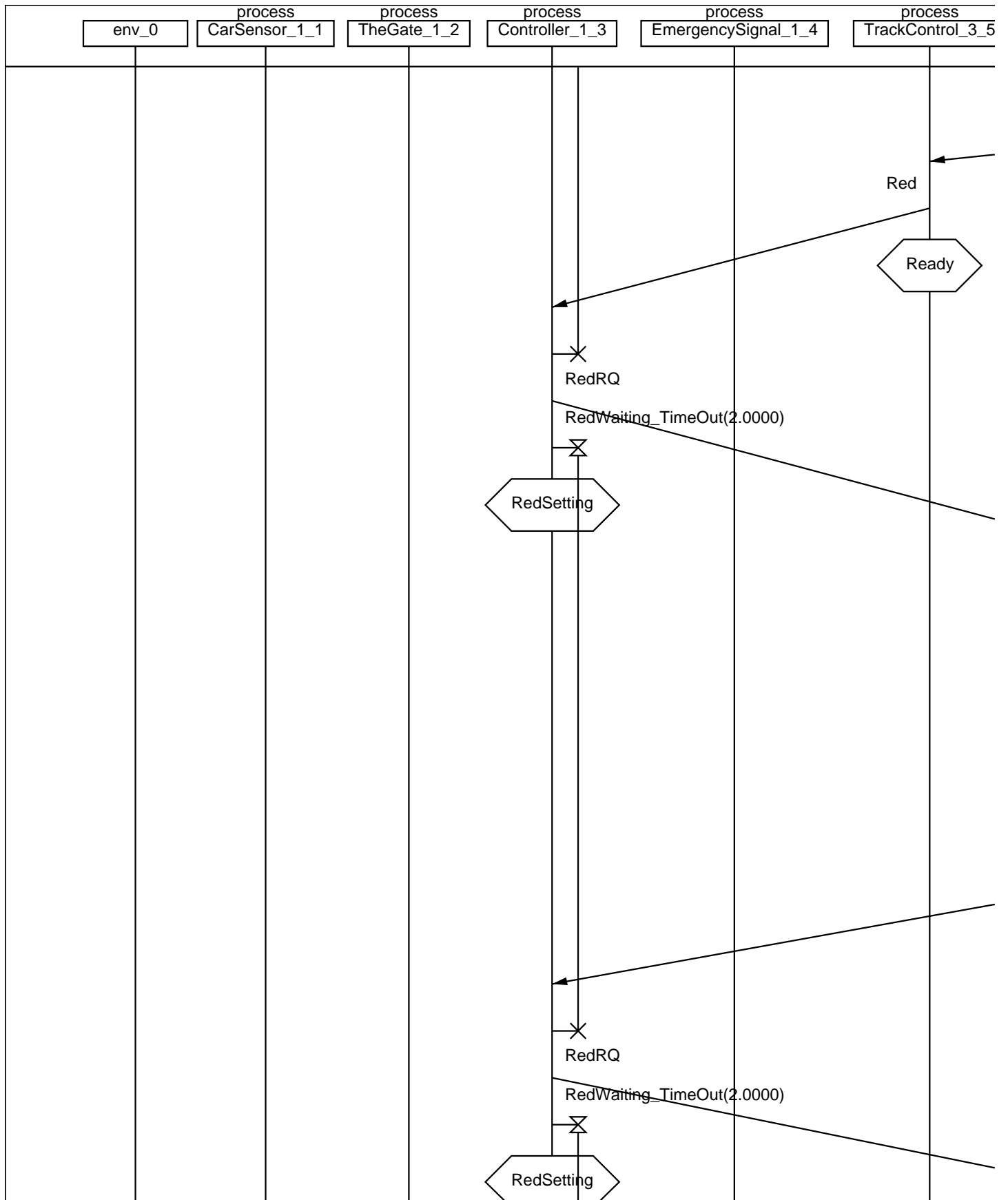


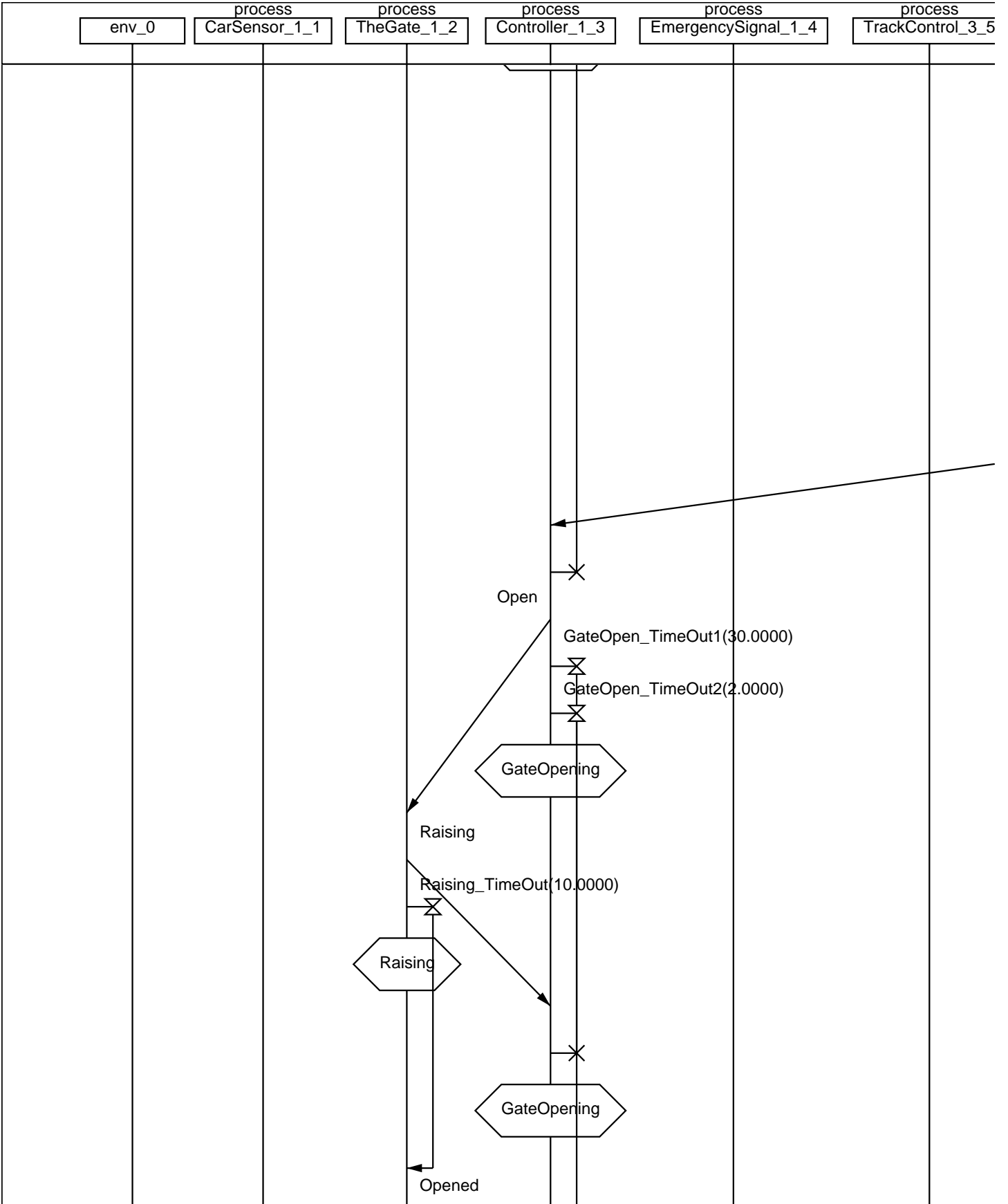


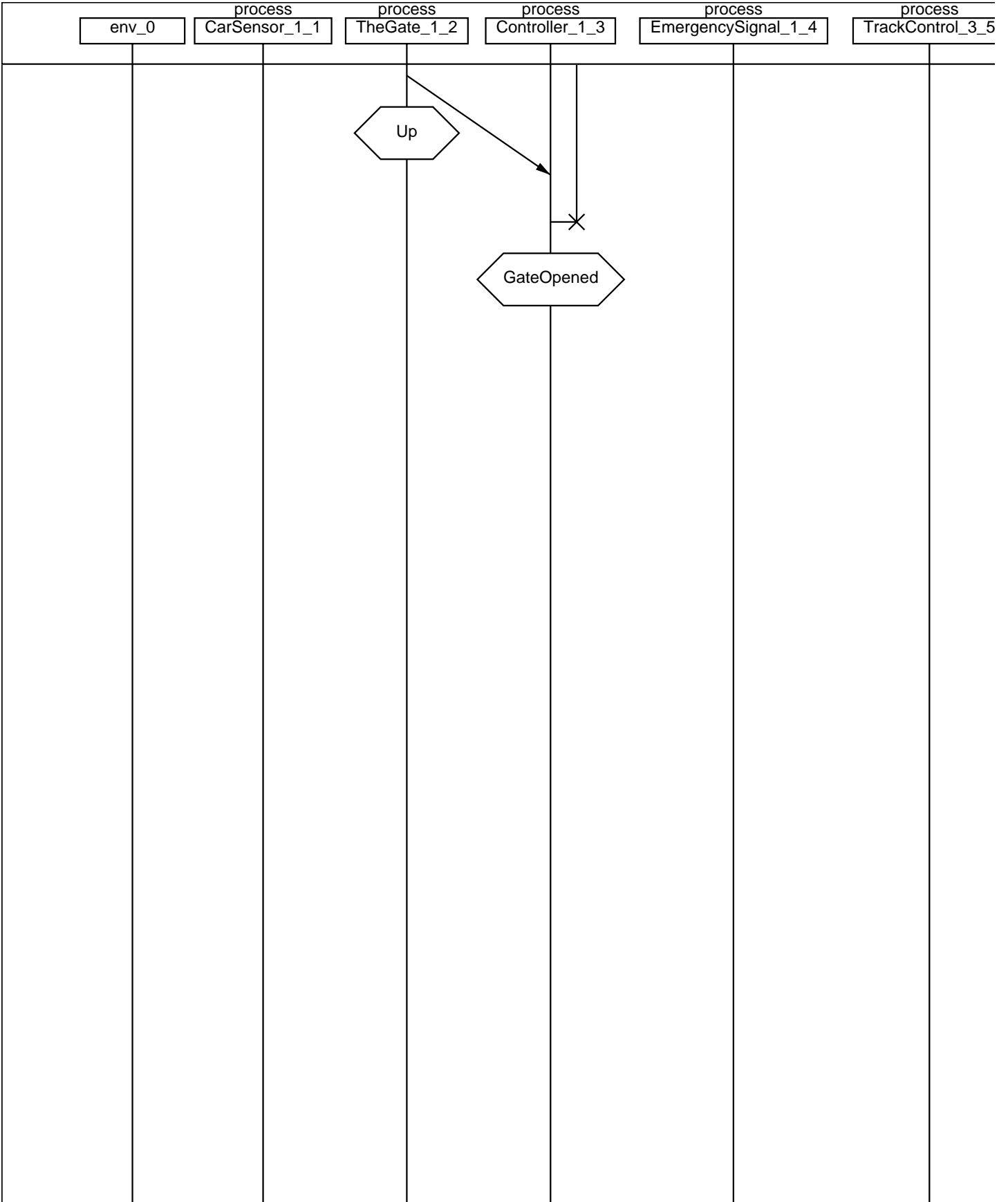


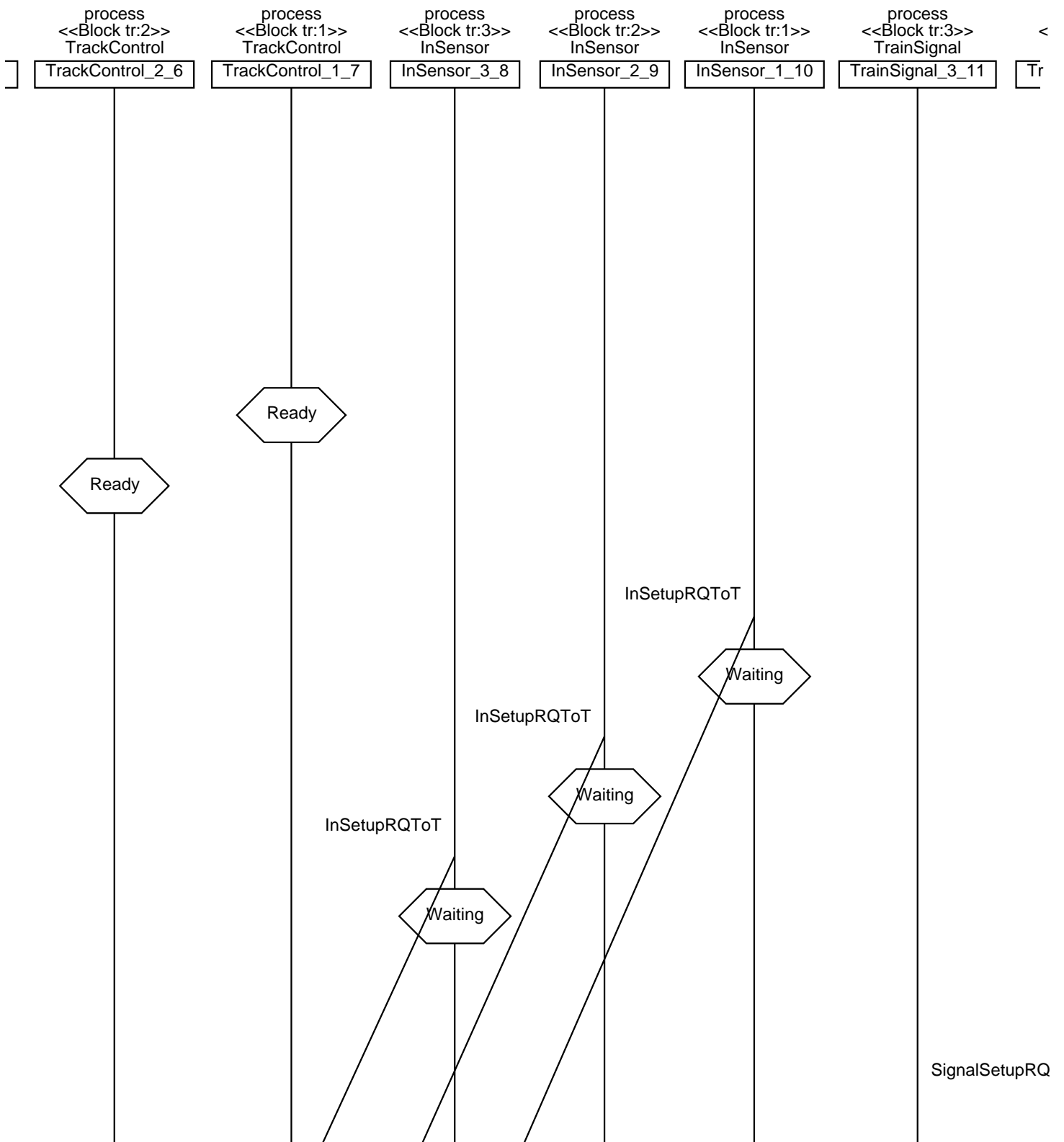


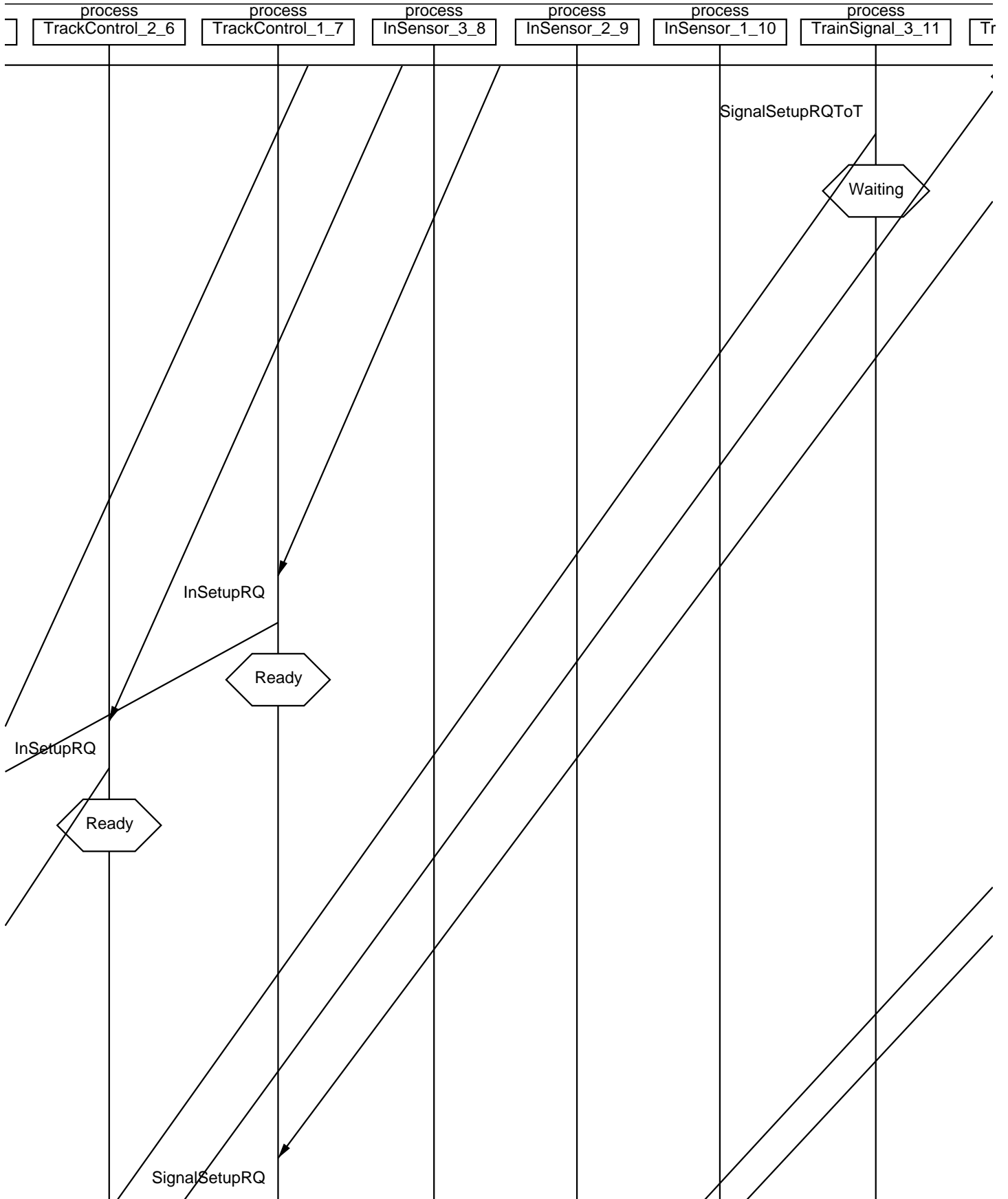


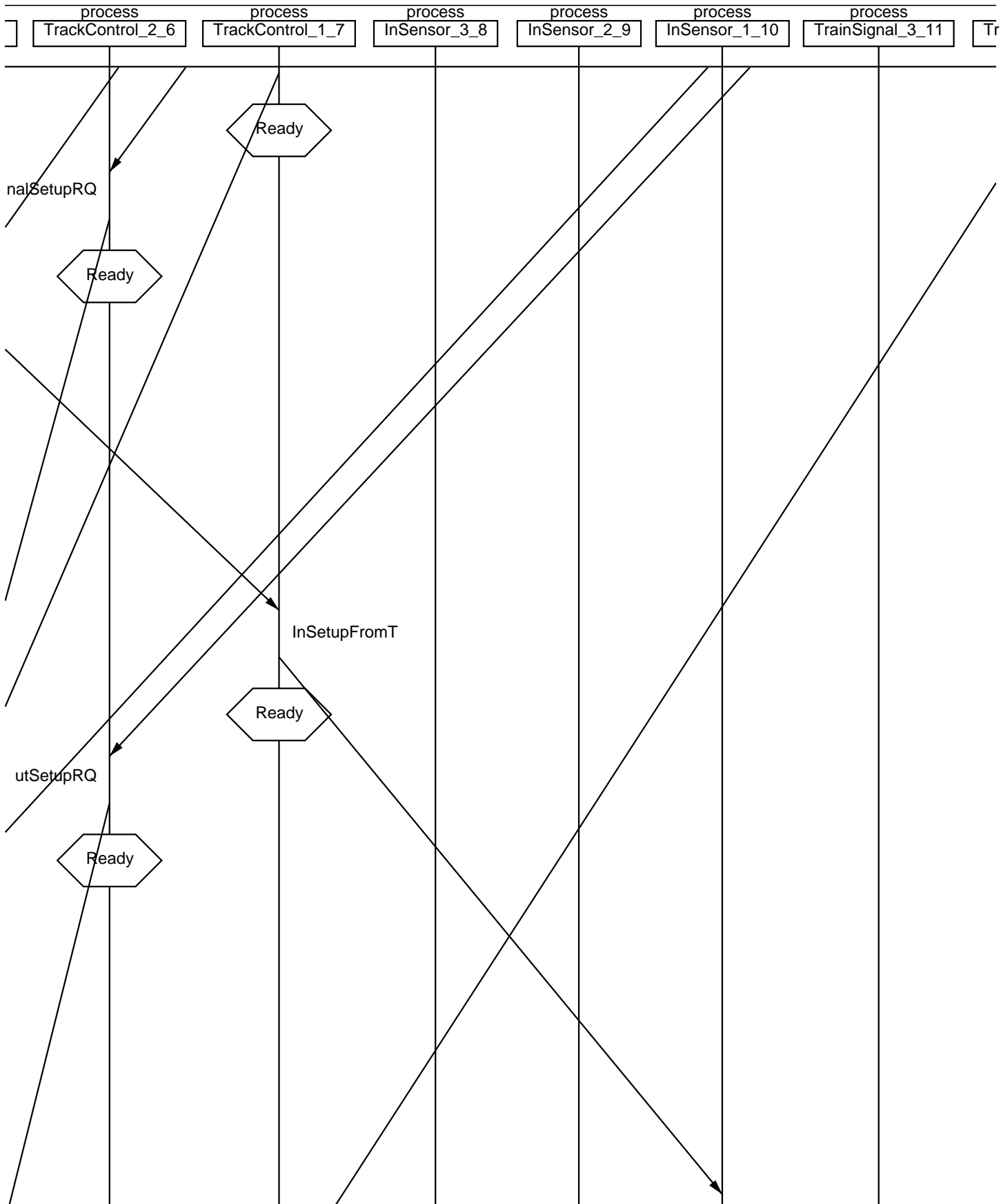


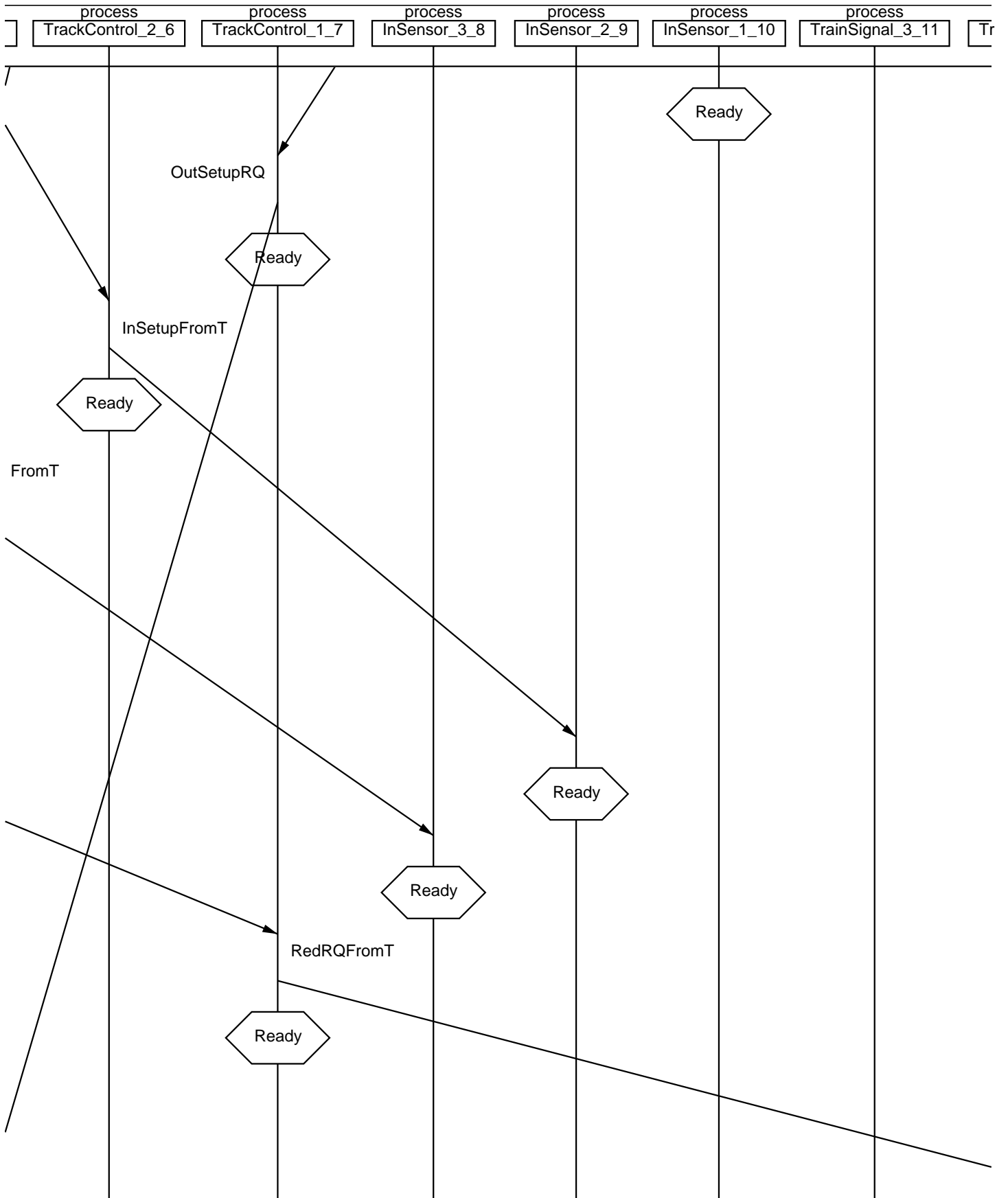


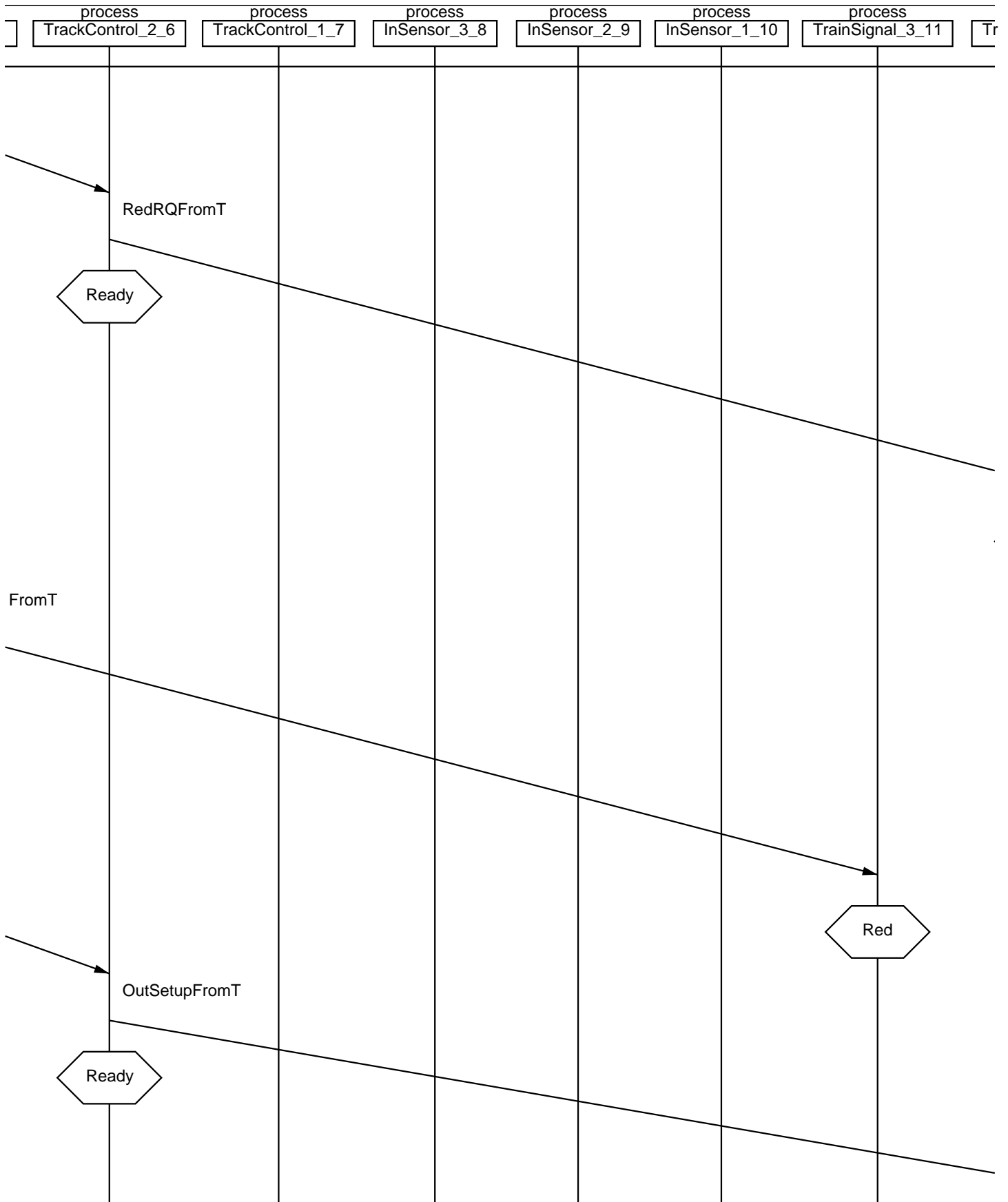


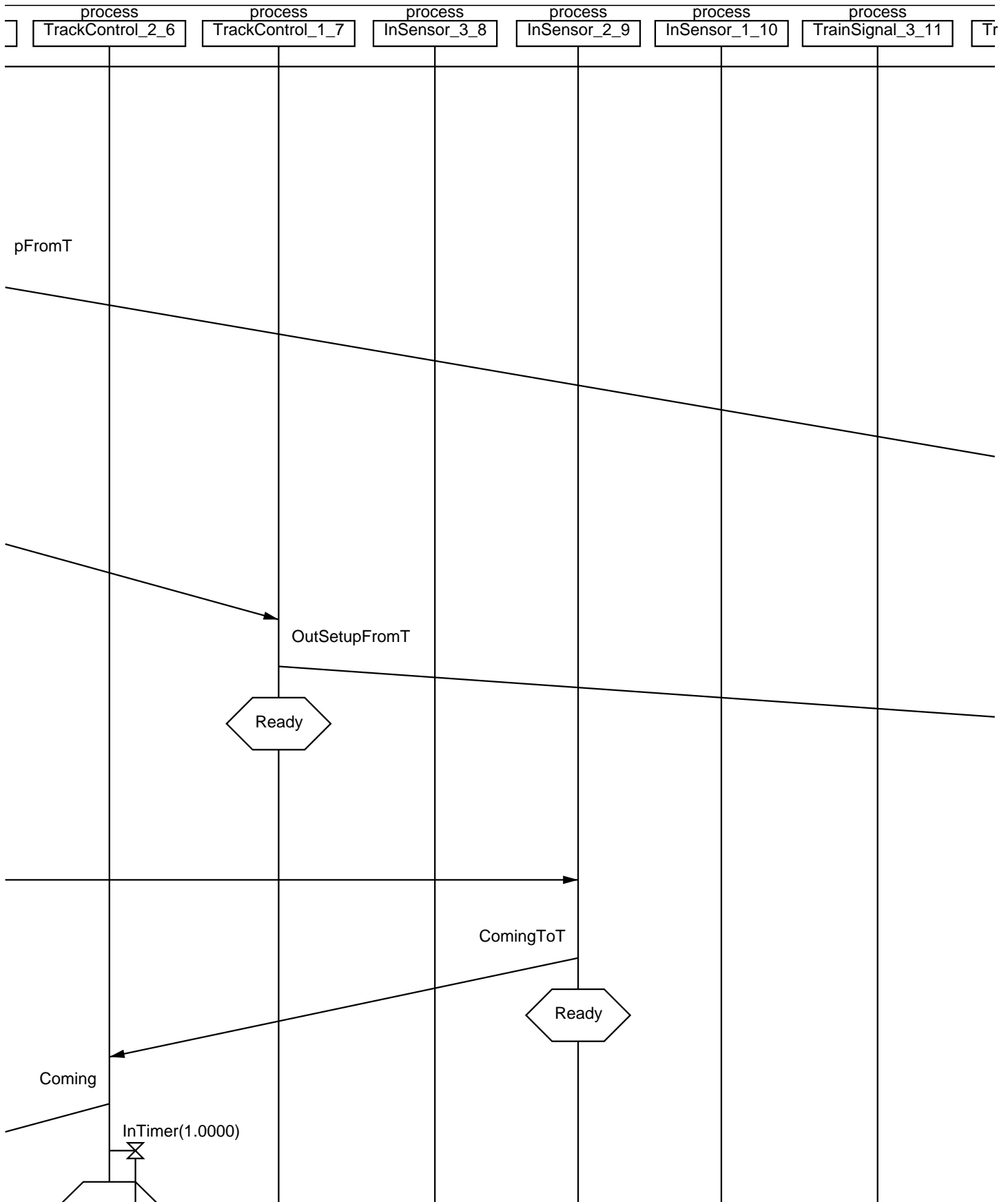


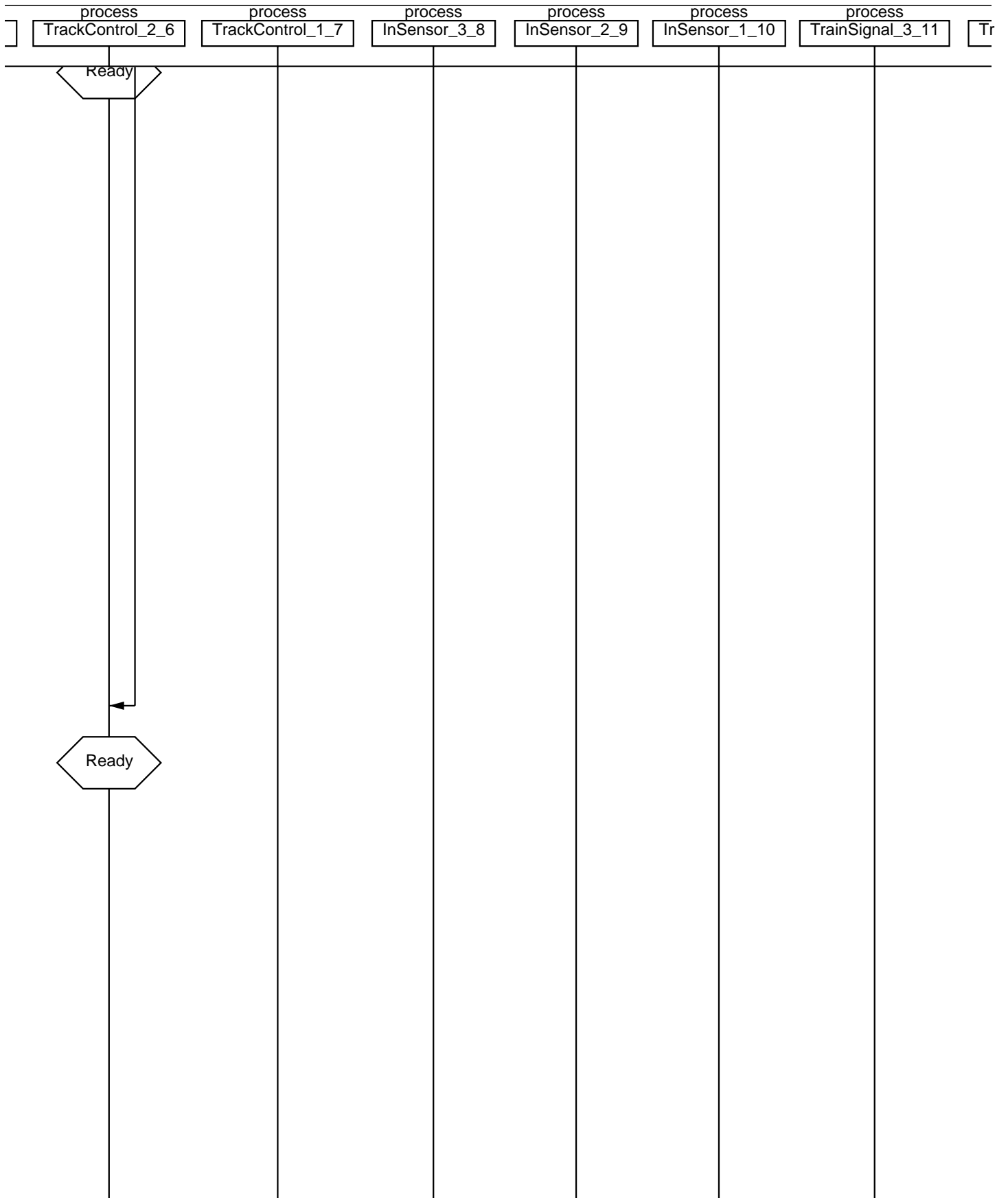


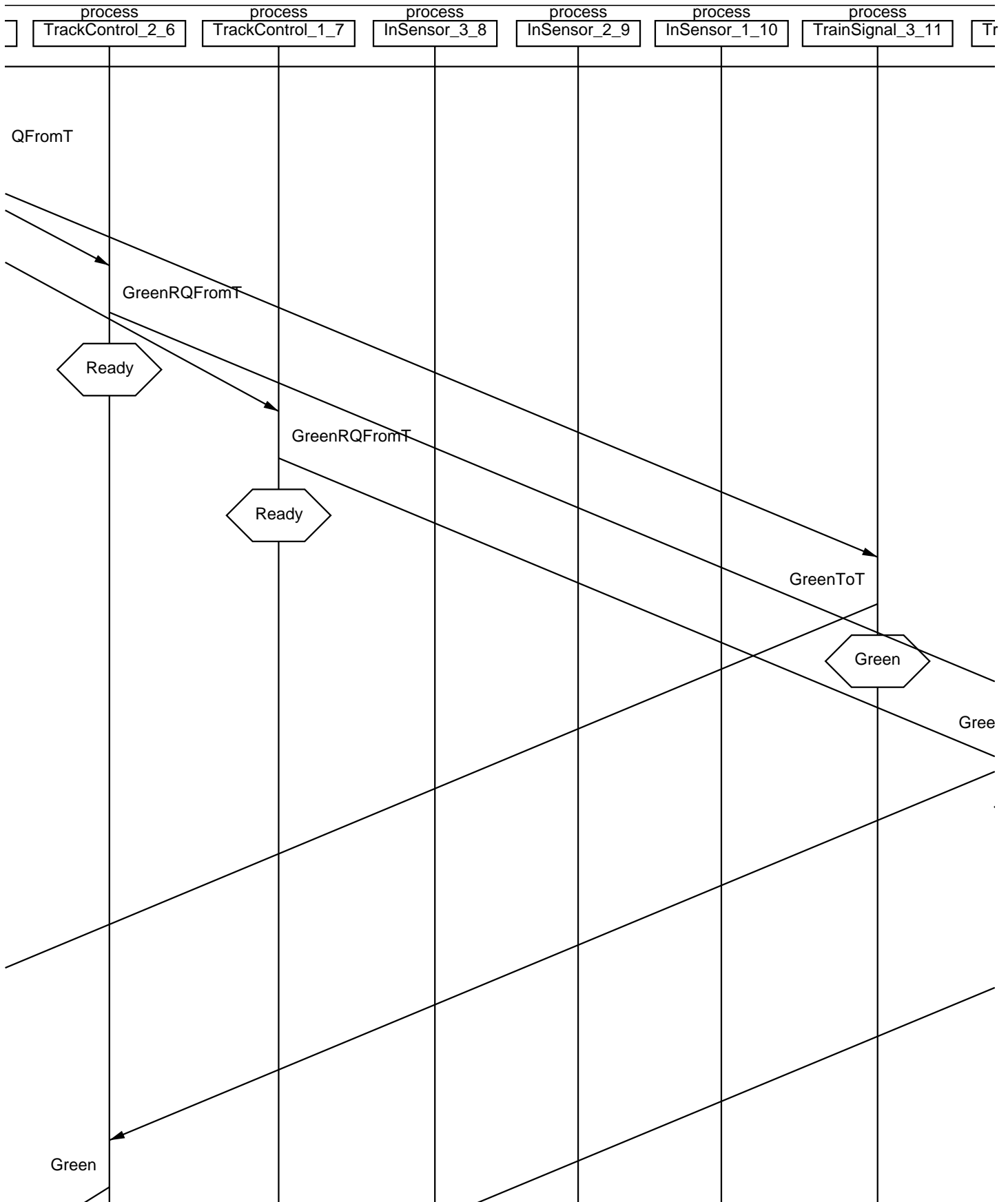


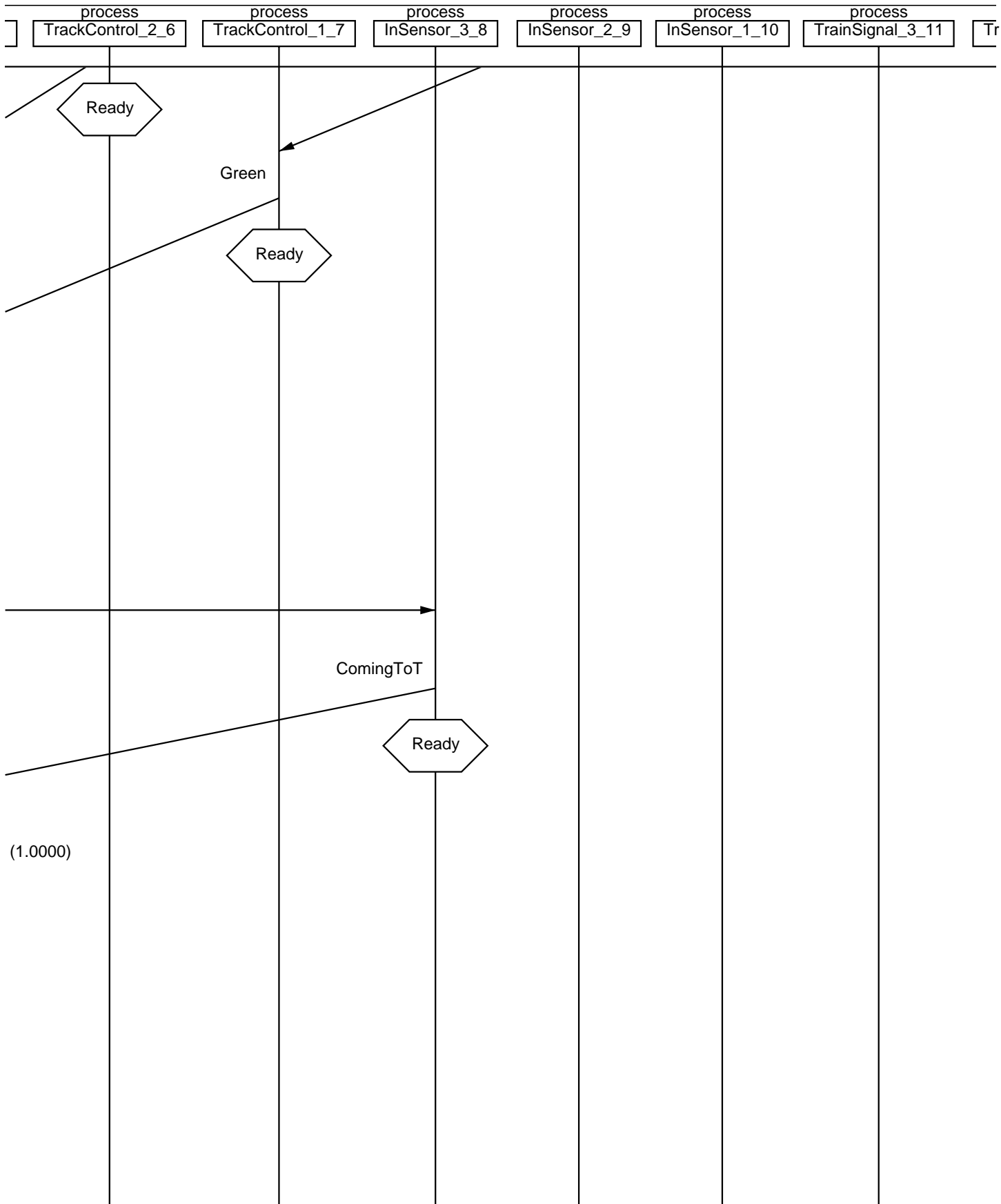


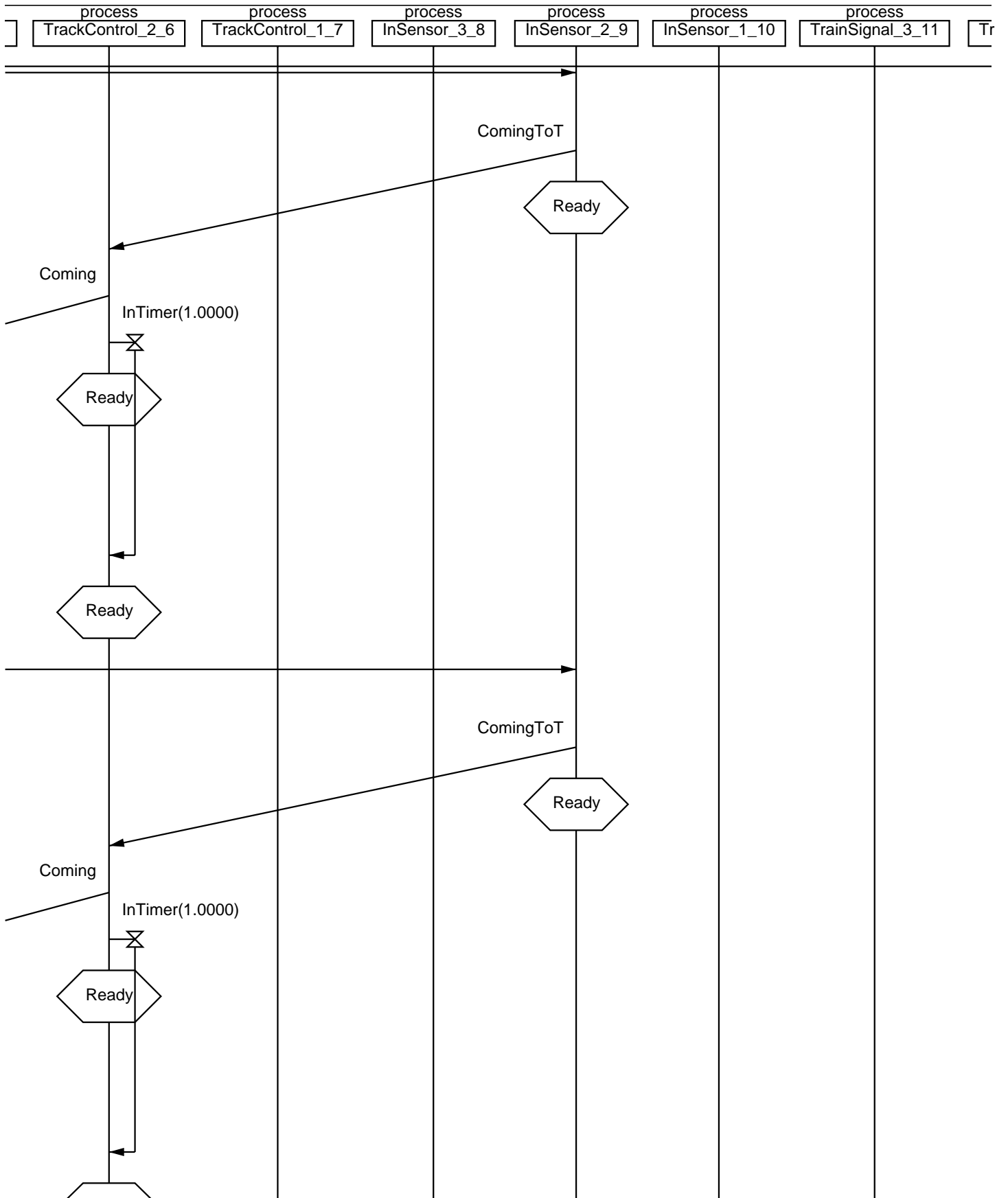


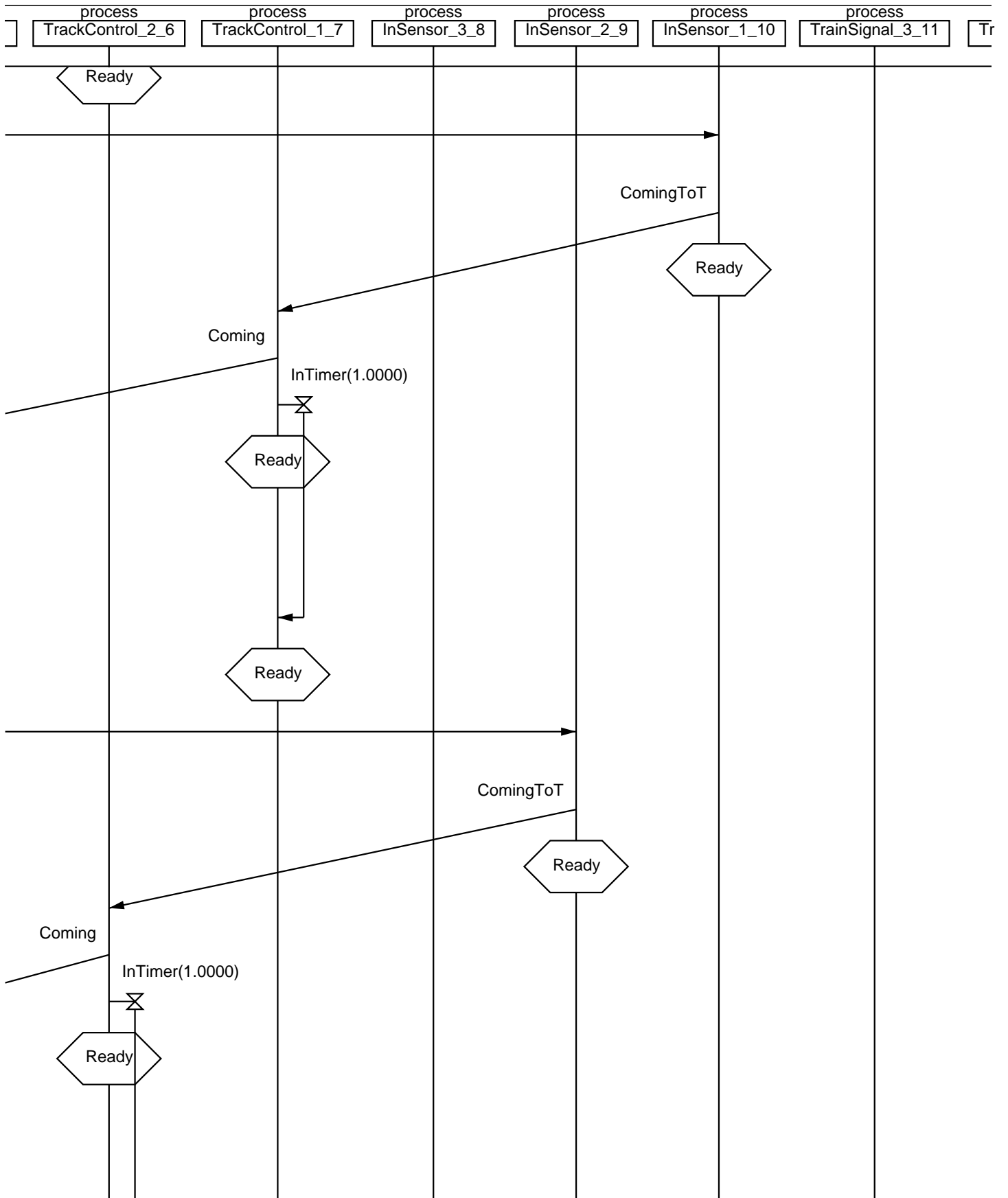


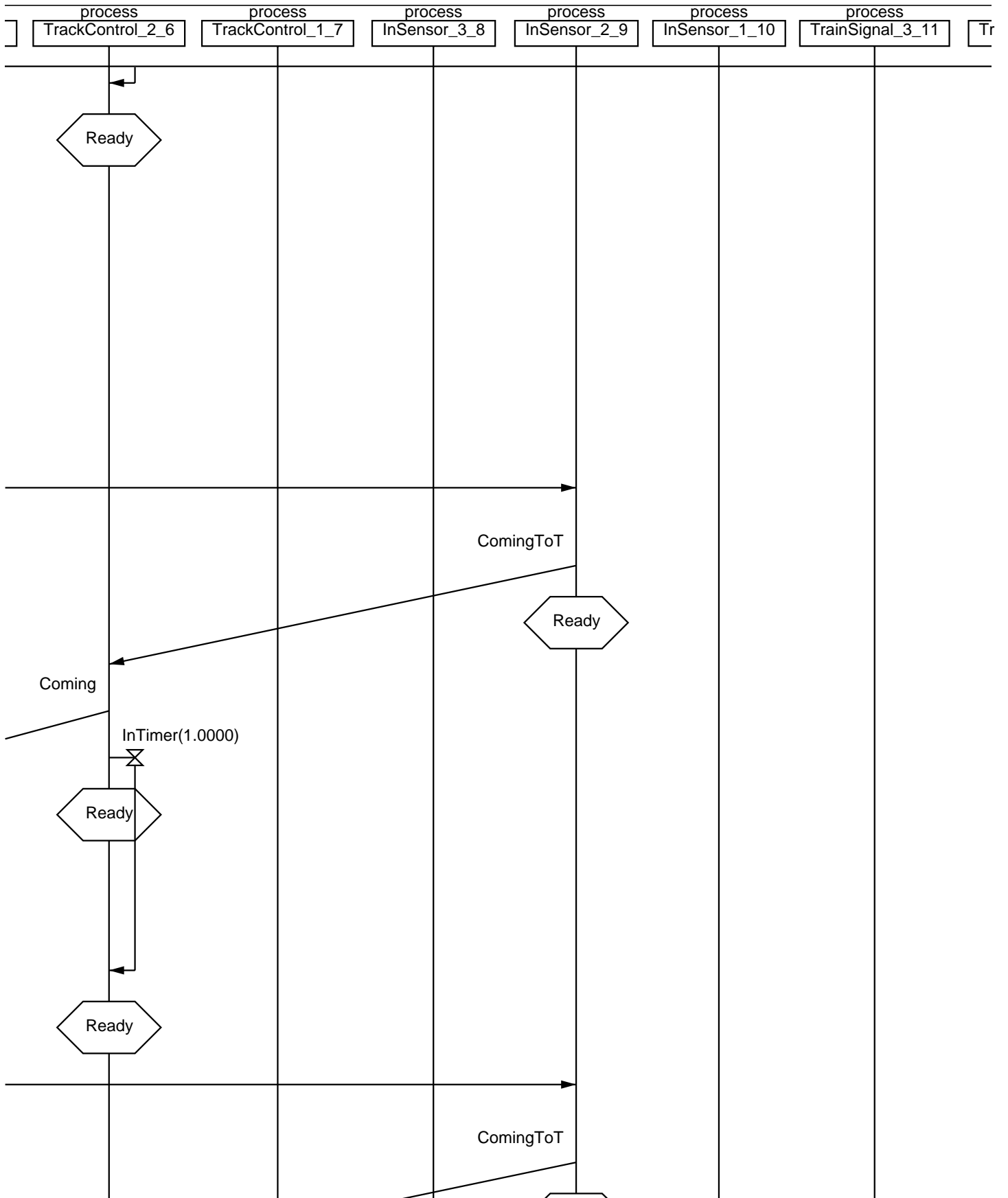


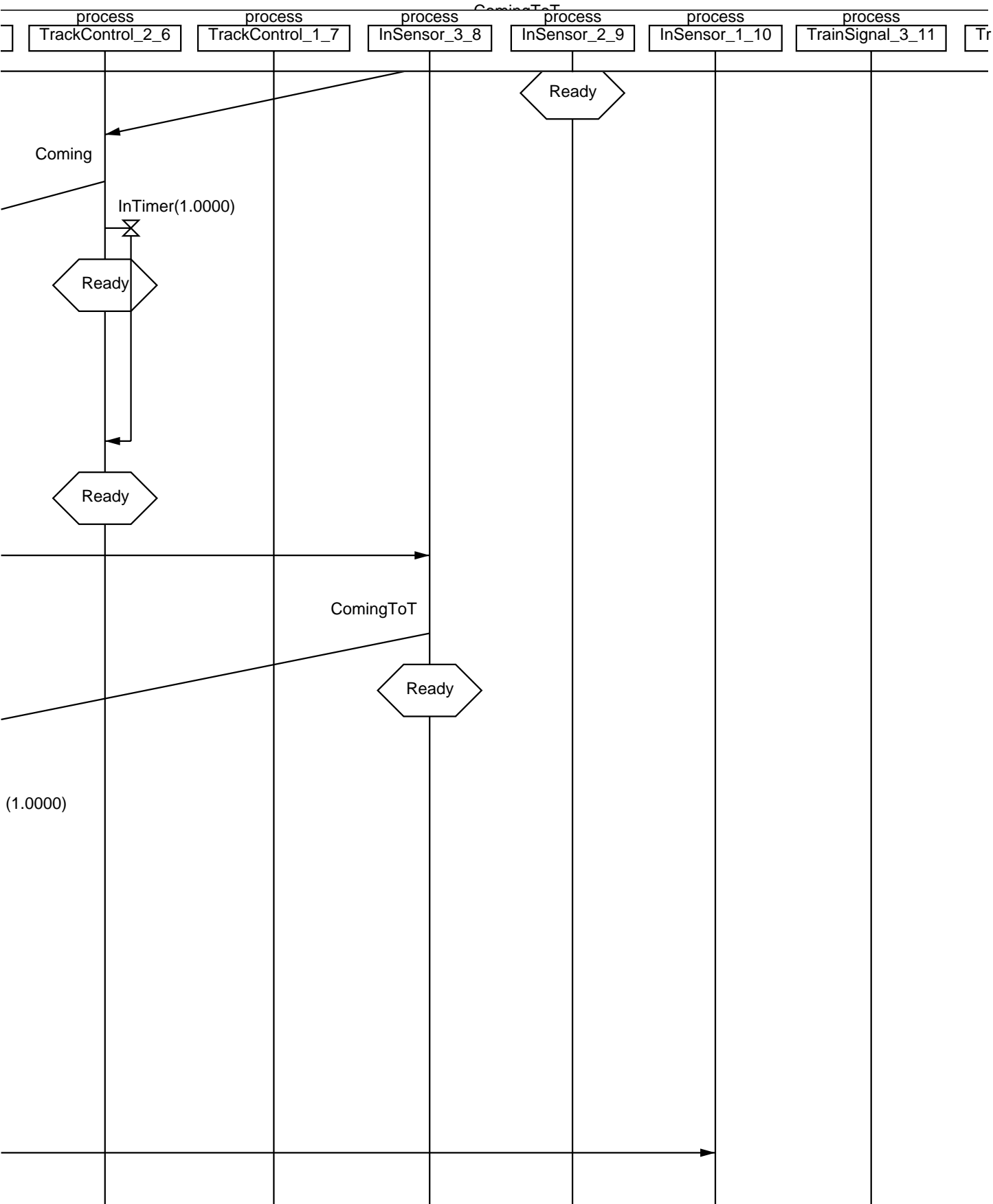


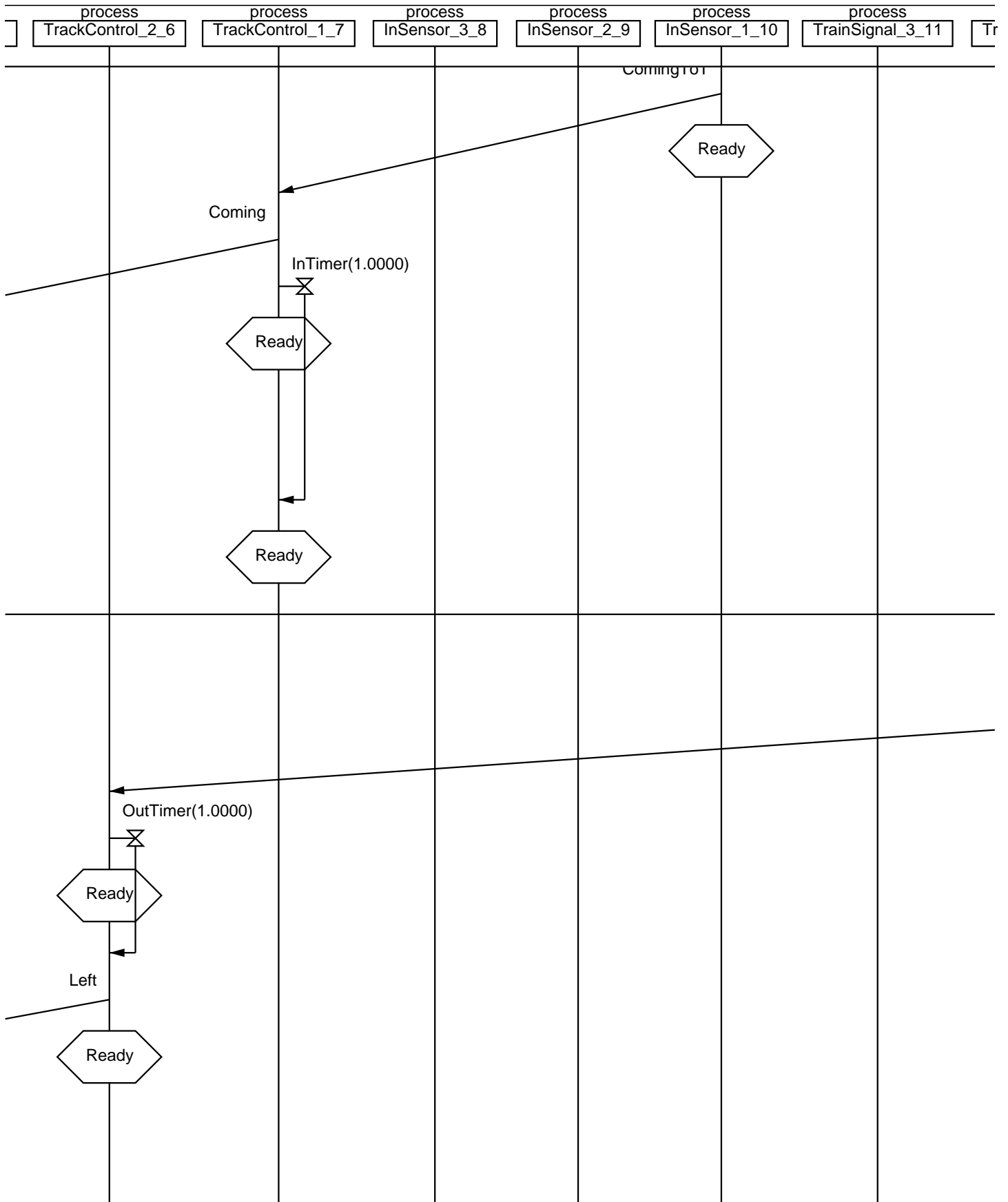


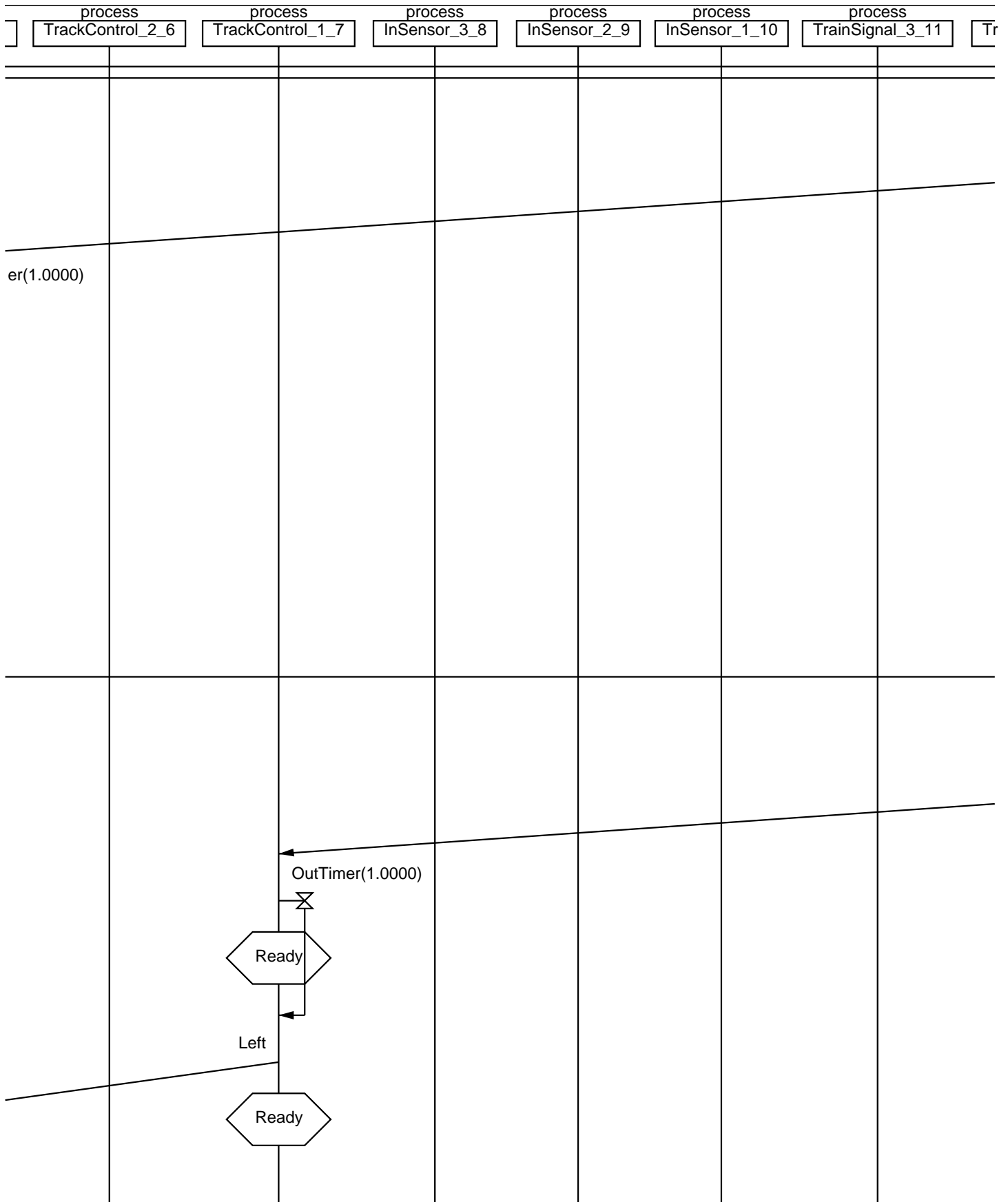


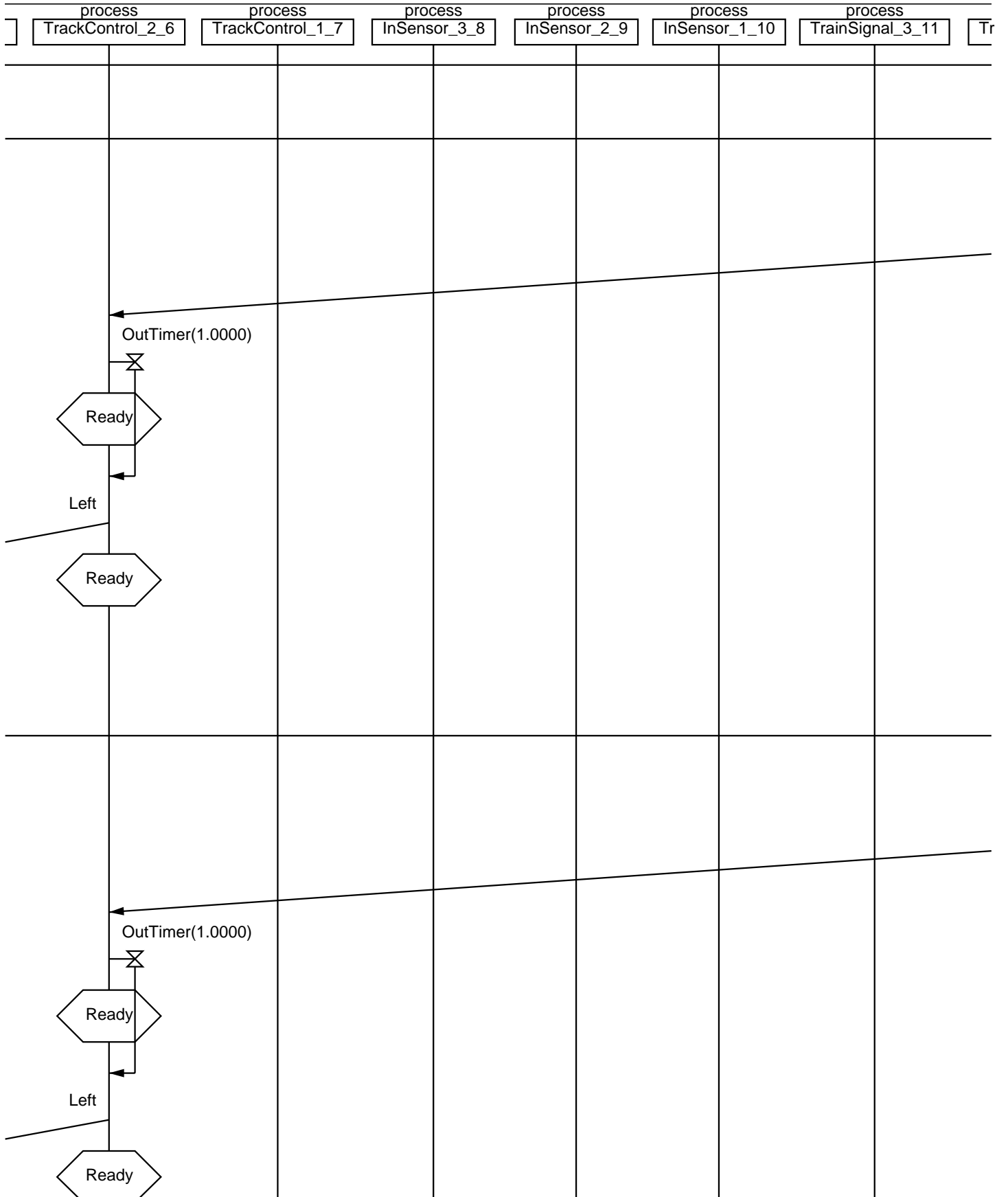


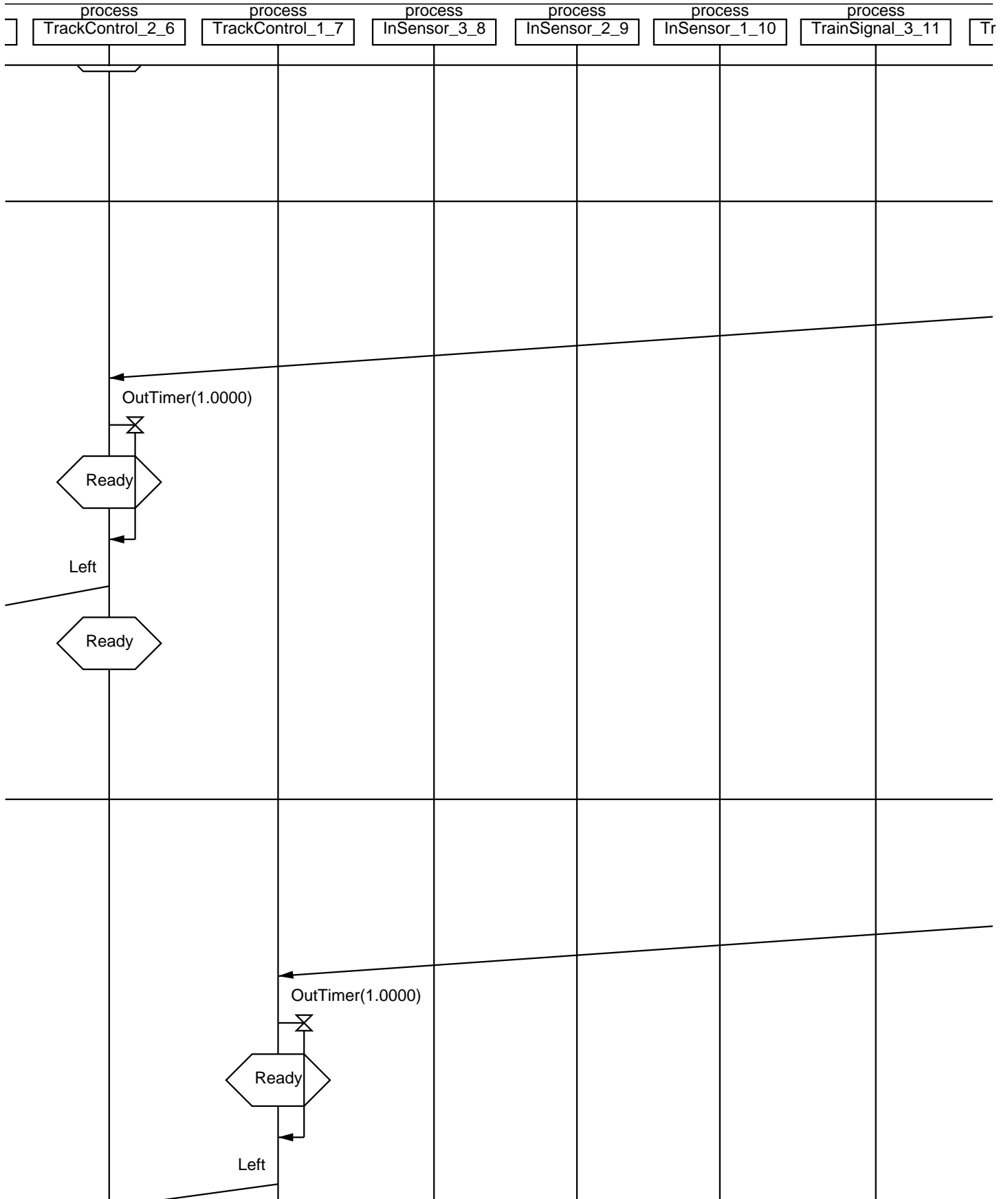


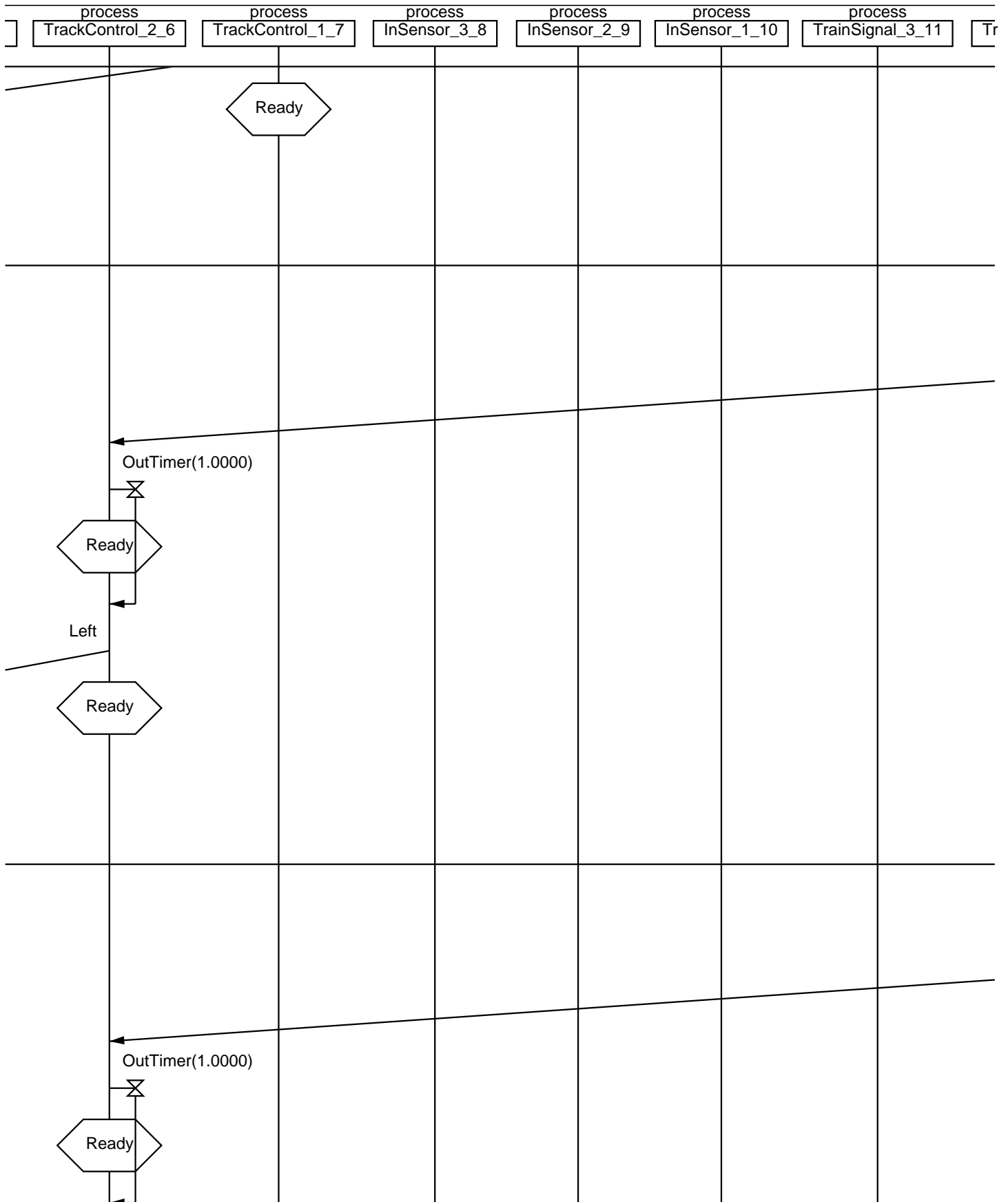


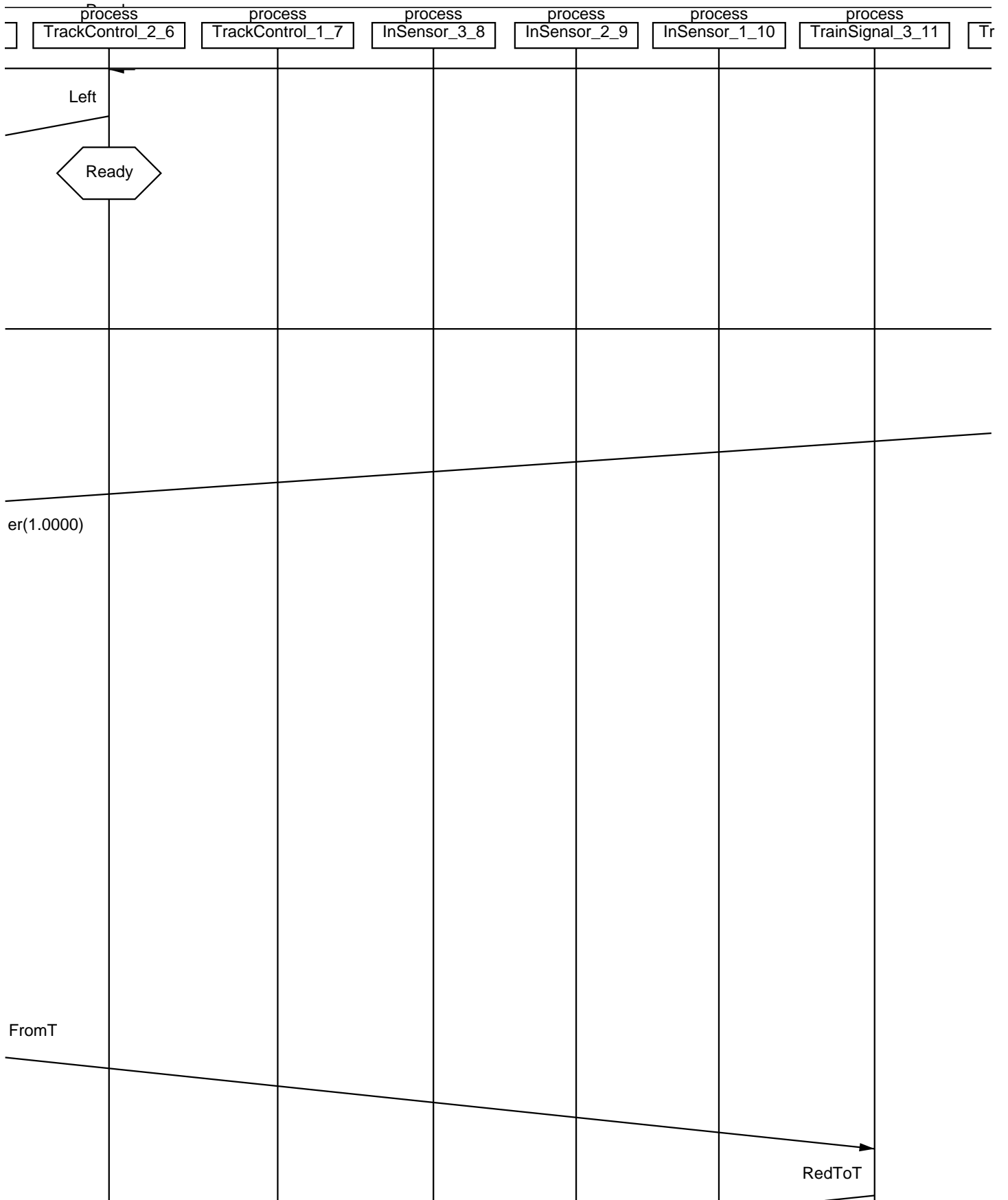


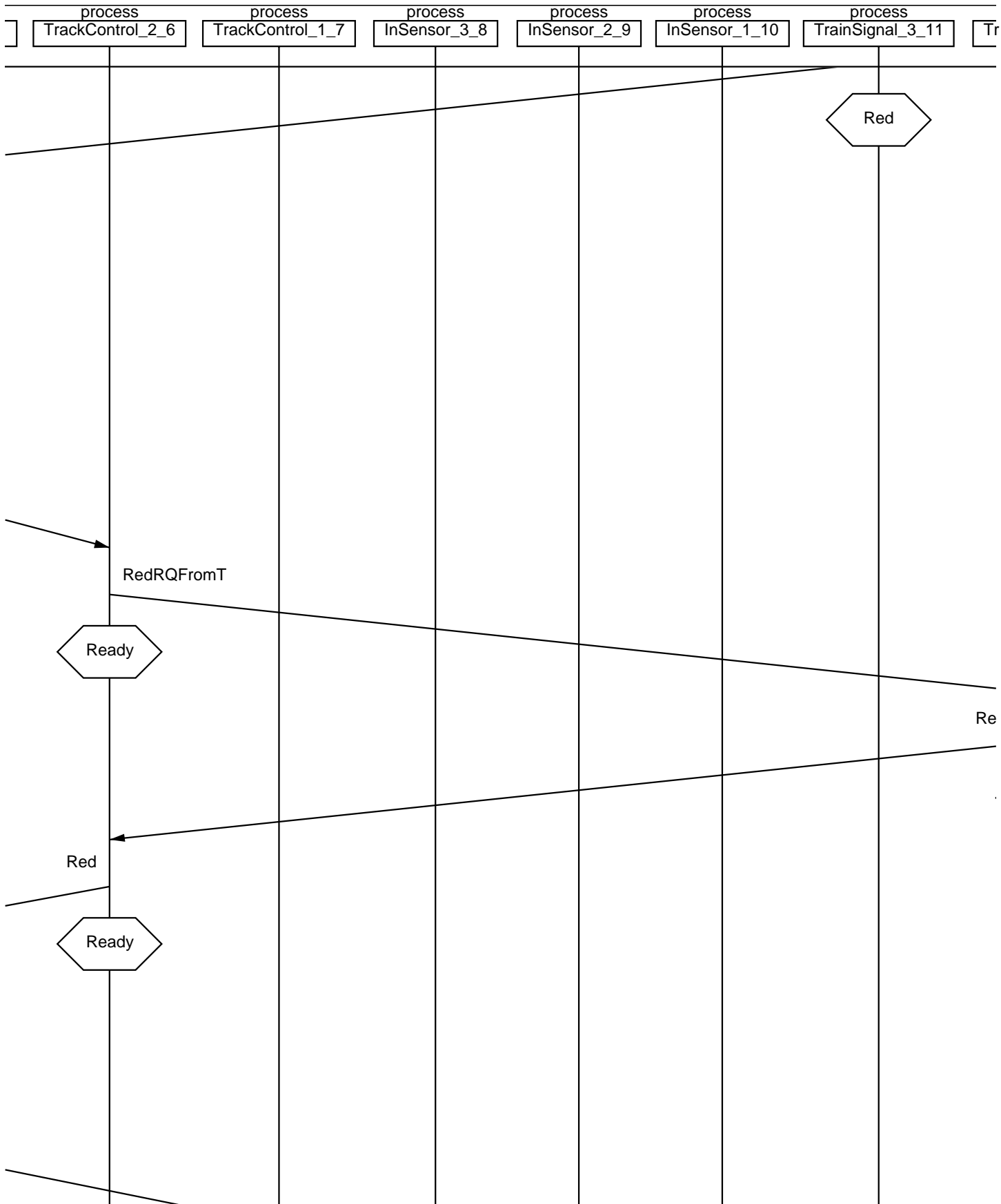


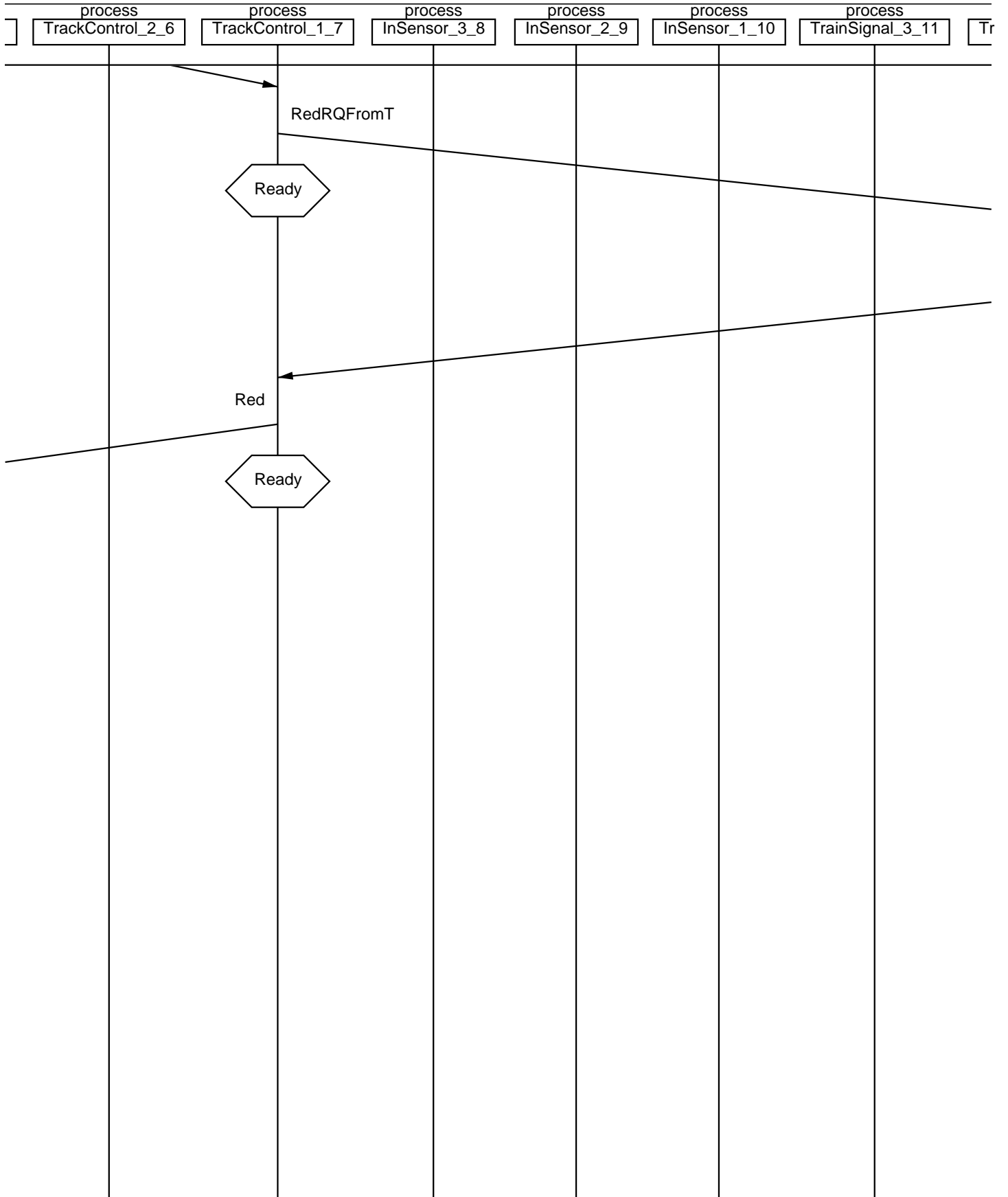




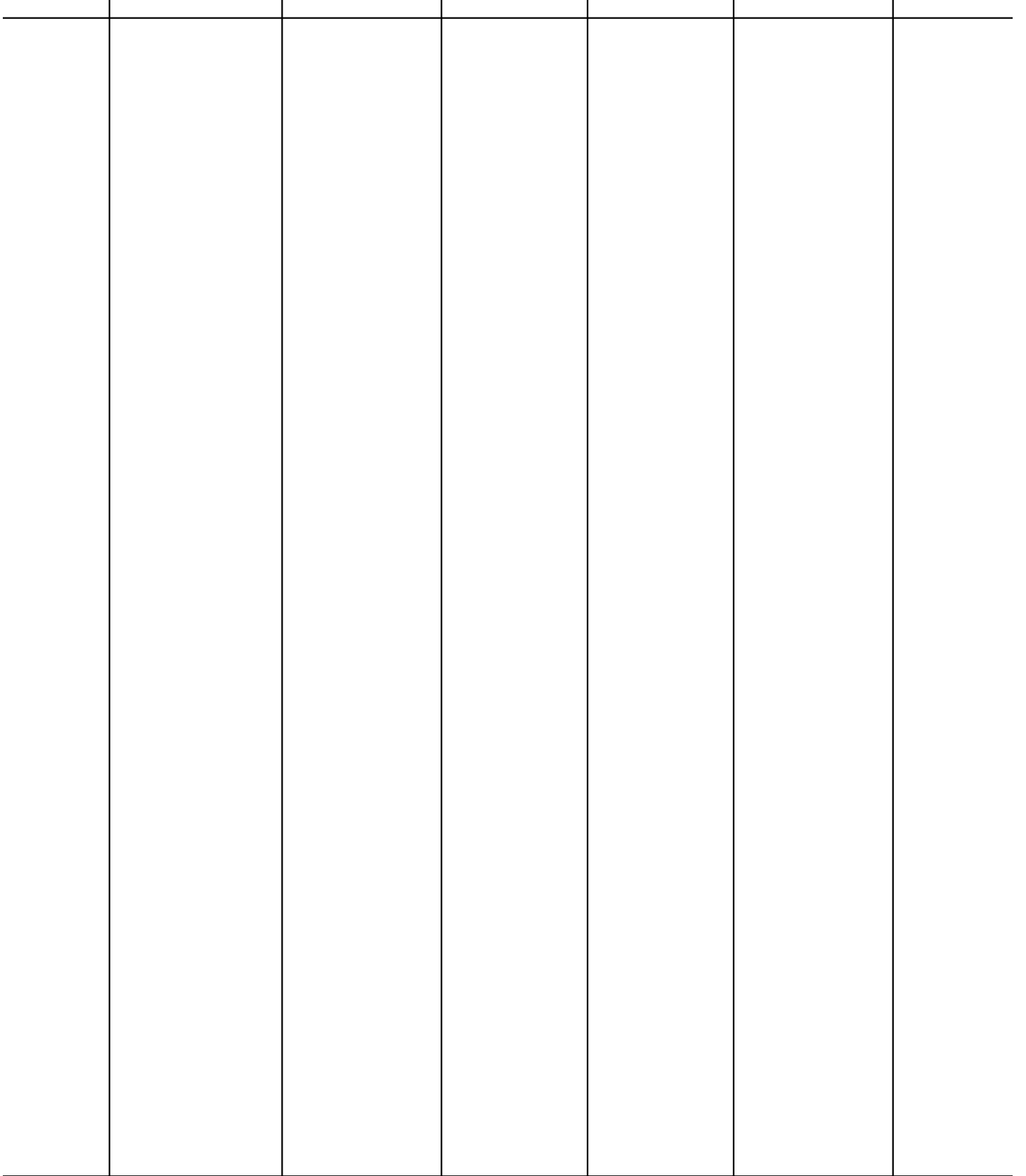


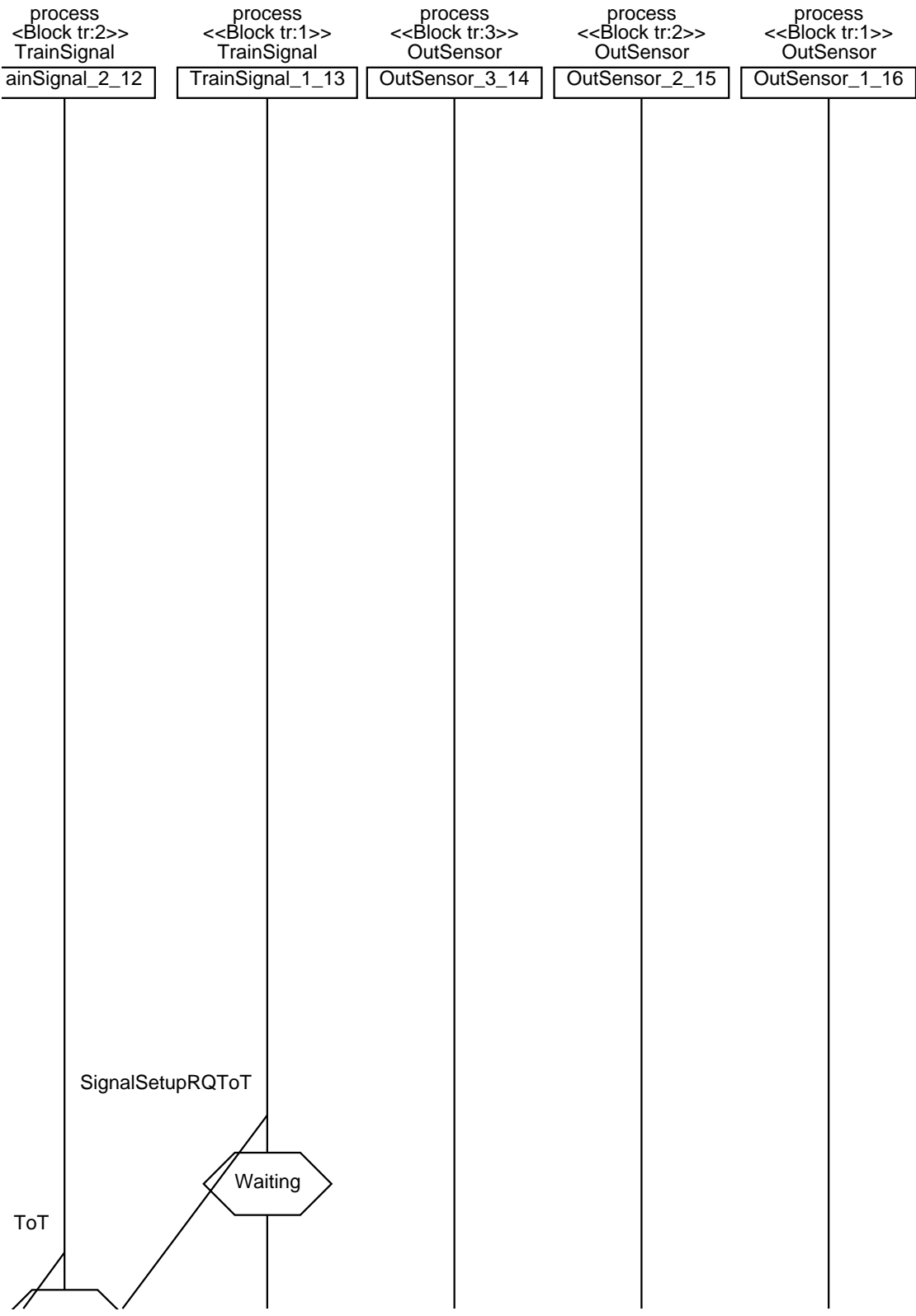


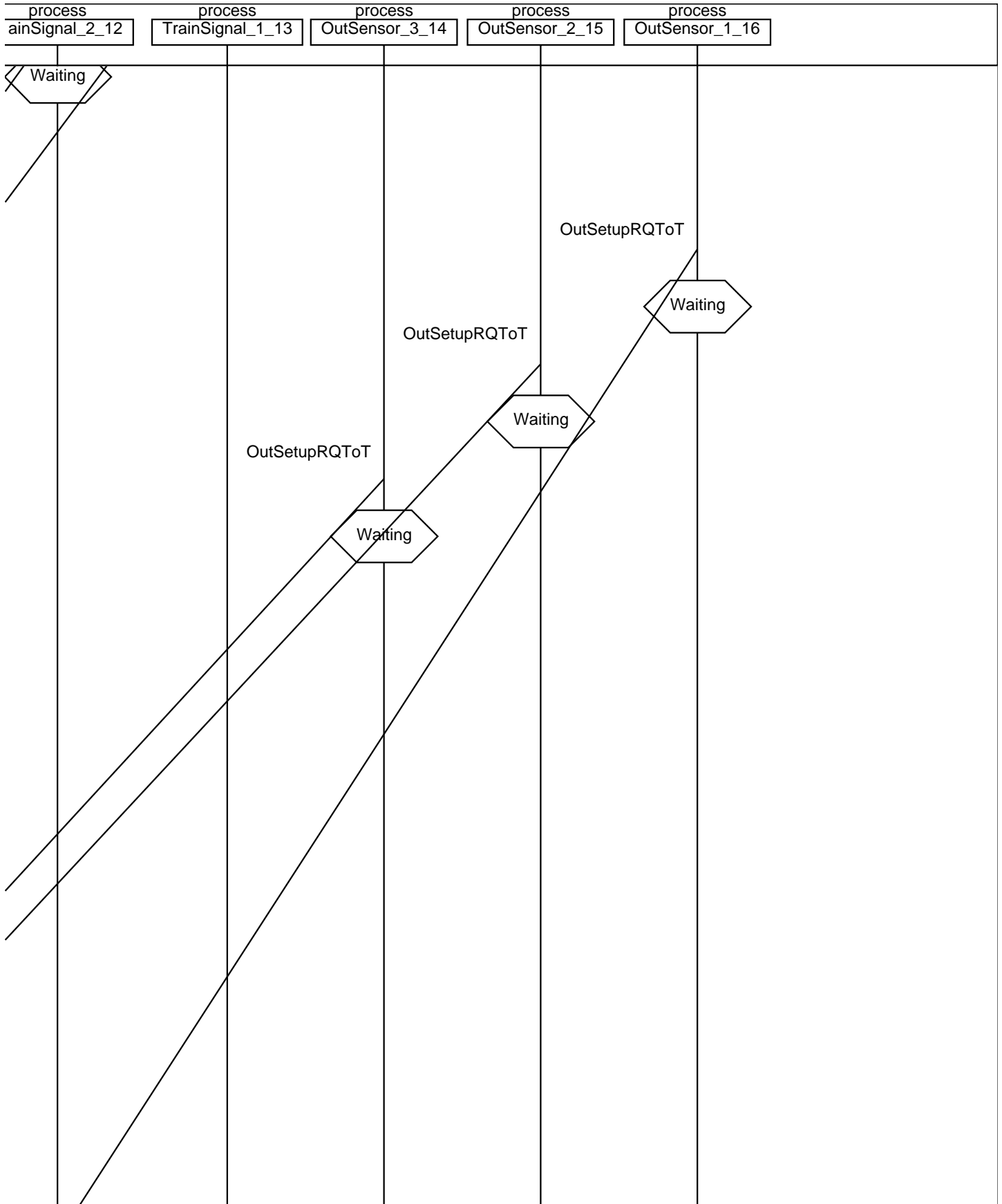




	process TrackControl_2_6	process TrackControl_1_7	process InSensor_3_8	process InSensor_2_9	process InSensor_1_10	process TrainSignal_3_11	Tr
--	-----------------------------	-----------------------------	-------------------------	-------------------------	--------------------------	-----------------------------	----







process	process	process	process	process
---------	---------	---------	---------	---------

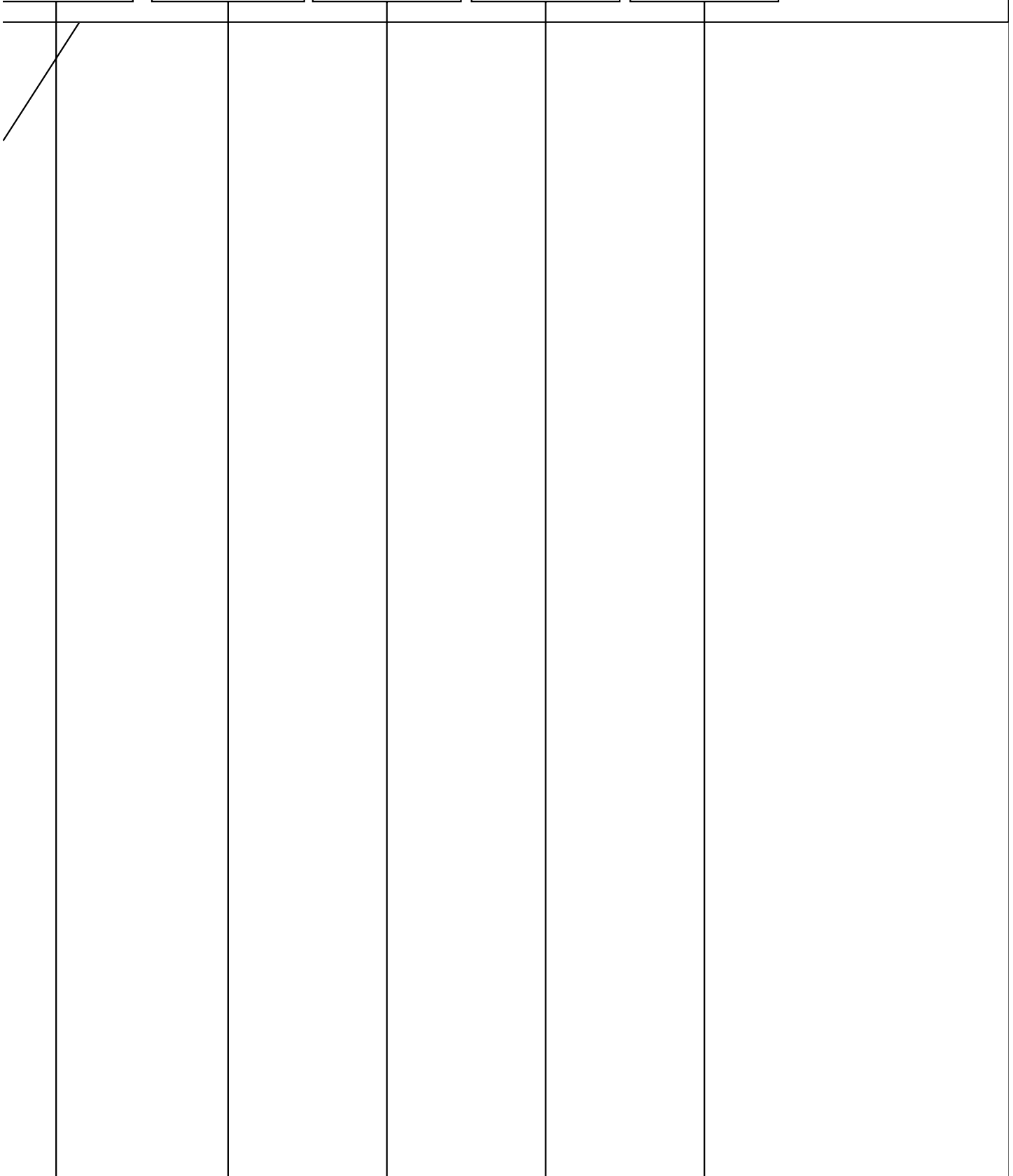
ainSignal_2_12

TrainSignal_1_13

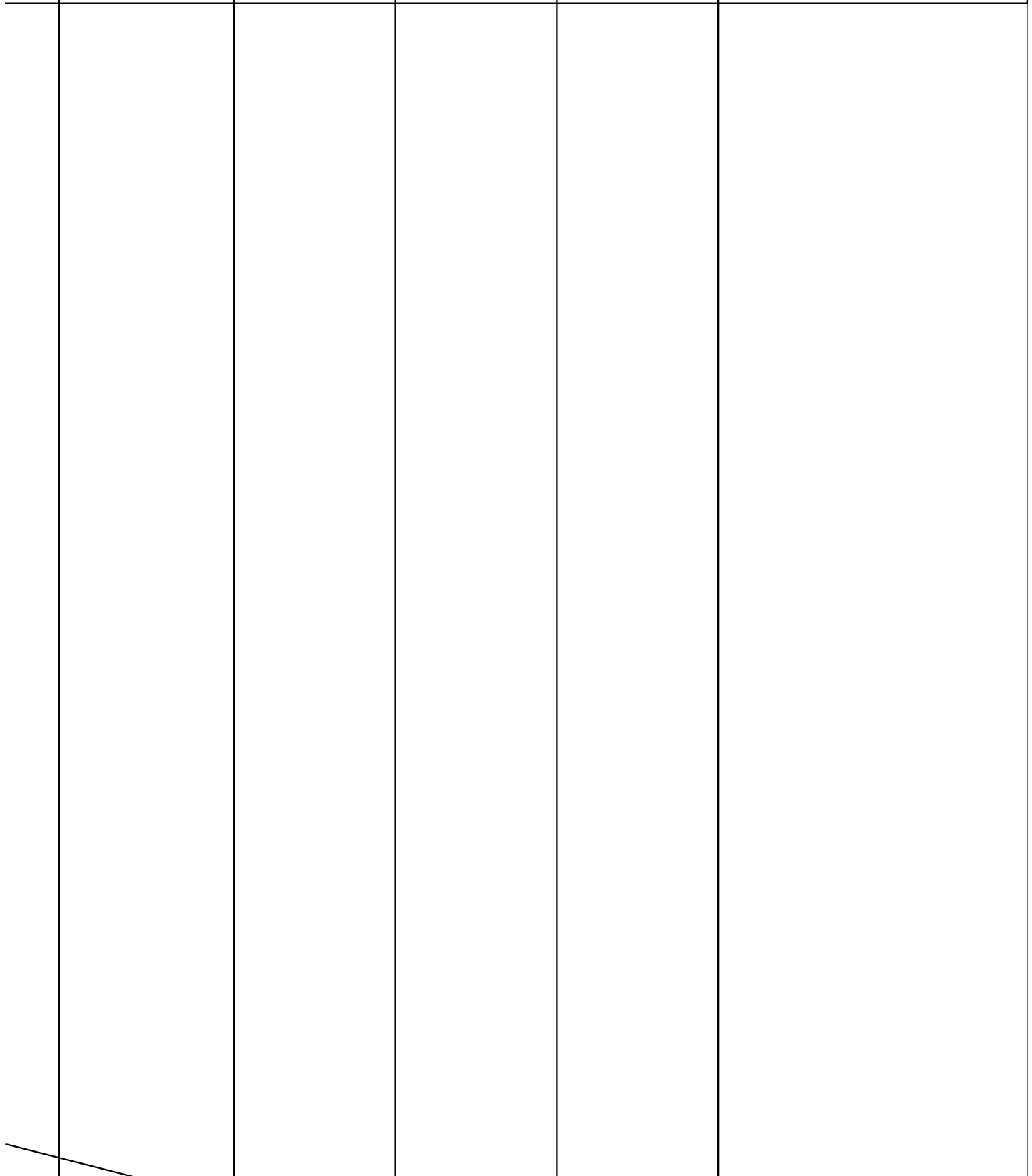
OutSensor_3_14

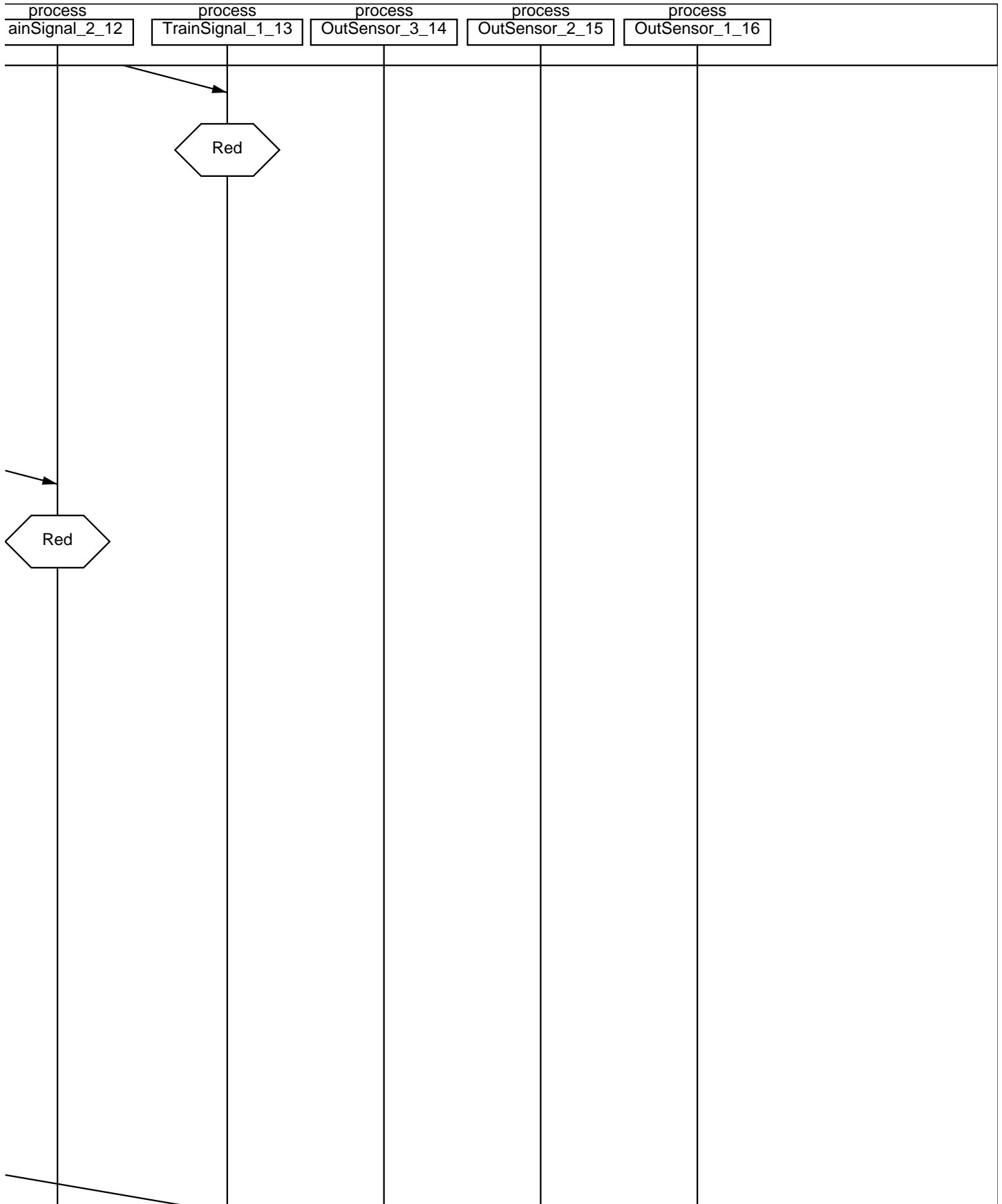
OutSensor_2_15

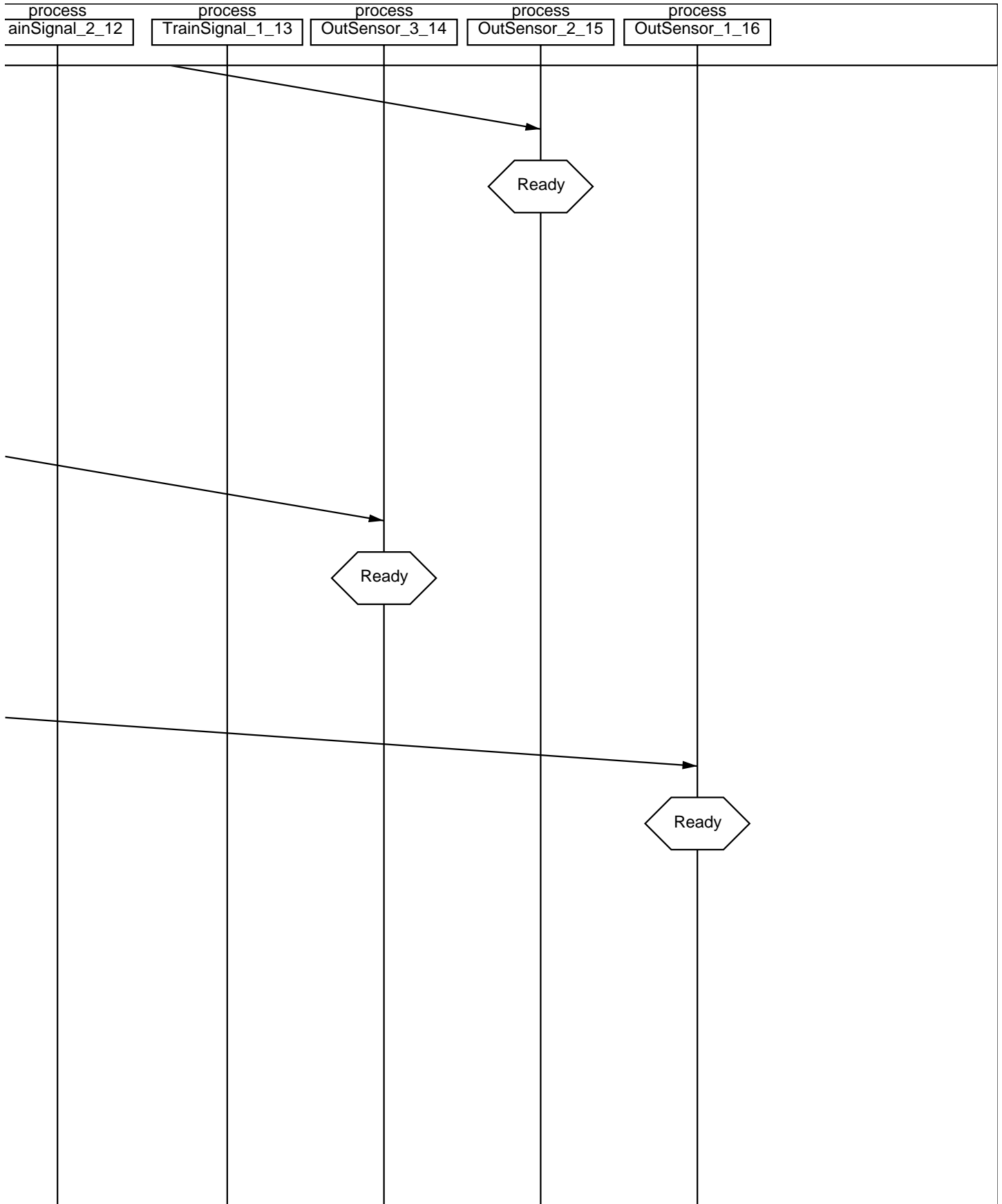
OutSensor_1_16



process	process	process	process	process
ainSignal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

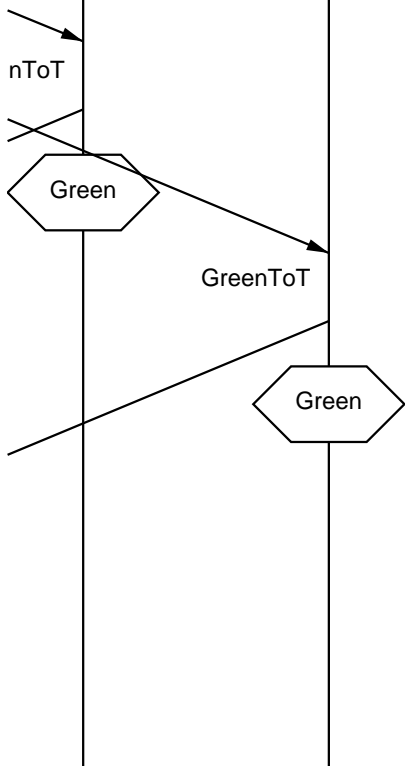
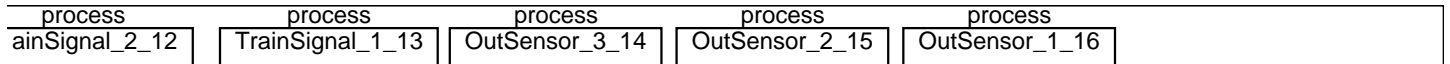






process ainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
---------------------------	-----------------------------	---------------------------	---------------------------	---------------------------

--	--	--	--	--	--



process	process	process	process	process
---------	---------	---------	---------	---------

ainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16

--	--	--	--	--	--

process	process	process	process	process
---------	---------	---------	---------	---------

ainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16

--	--	--	--	--	--

process ainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
---------------------------	-----------------------------	---------------------------	---------------------------	---------------------------

--	--	--	--	--	--

process	process	process	process	process
---------	---------	---------	---------	---------

ainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16

--	--	--	--	--	--

process	process	process	process	process
---------	---------	---------	---------	---------

ainSignal_2_12

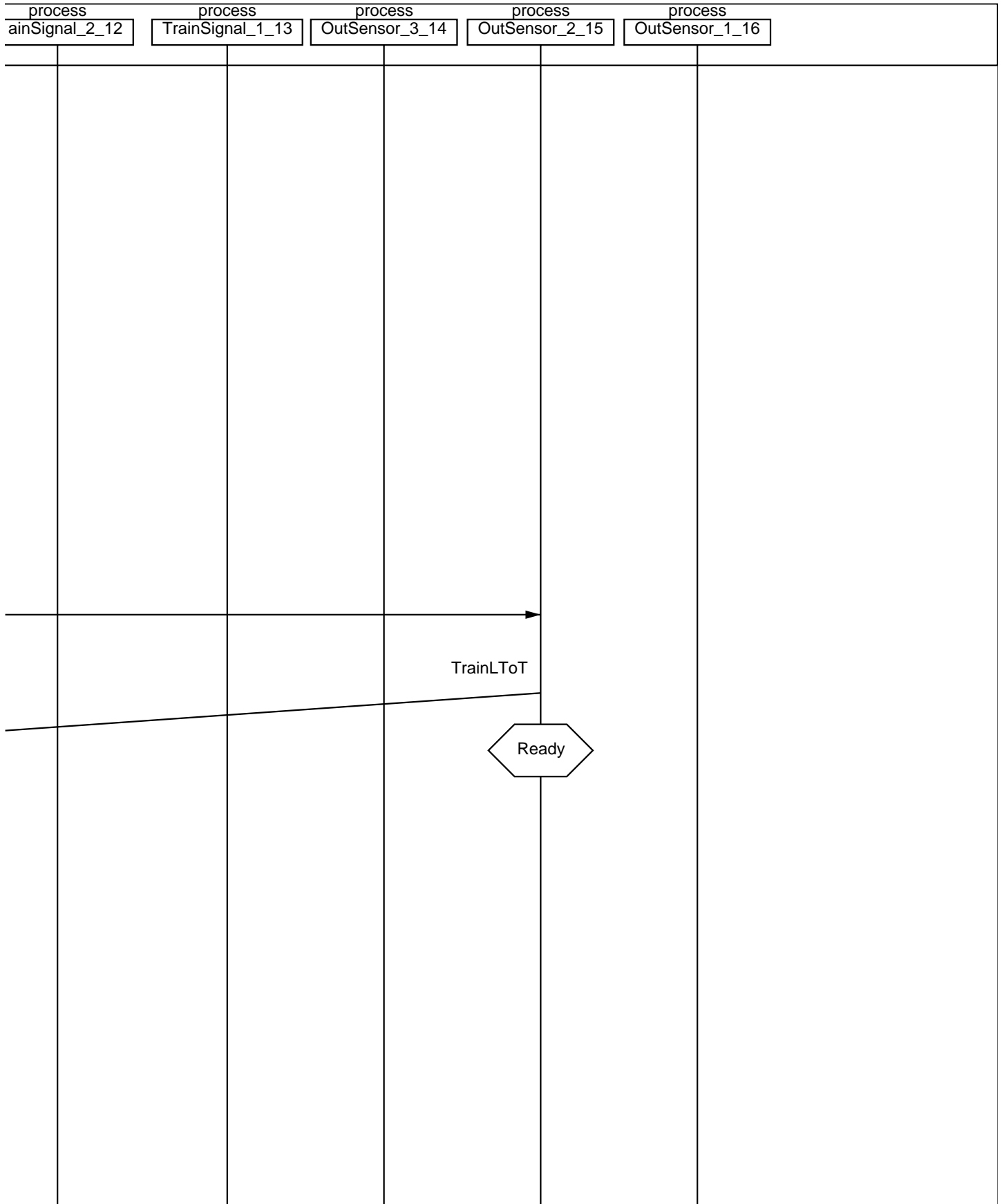
TrainSignal_1_13

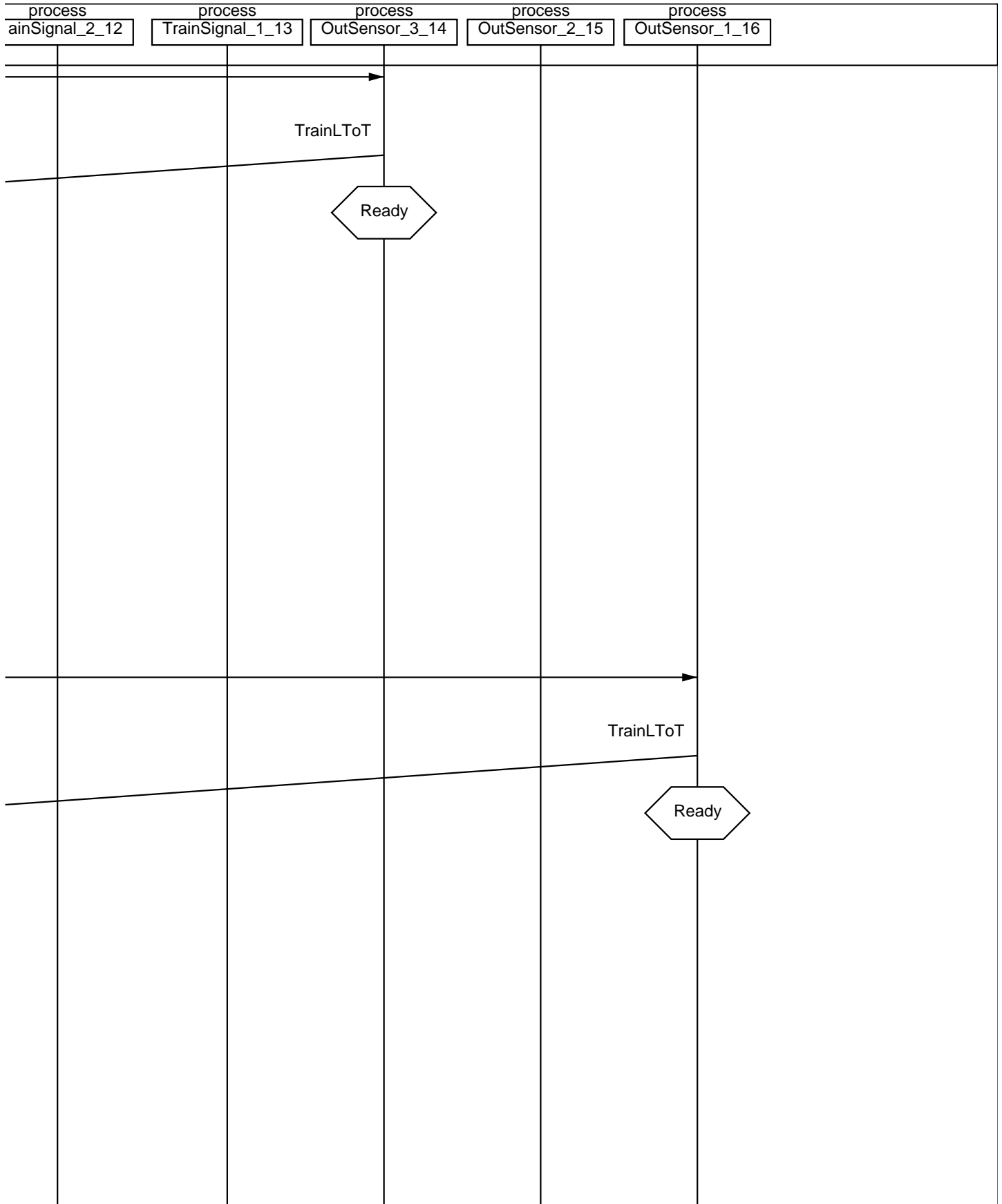
OutSensor_3_14

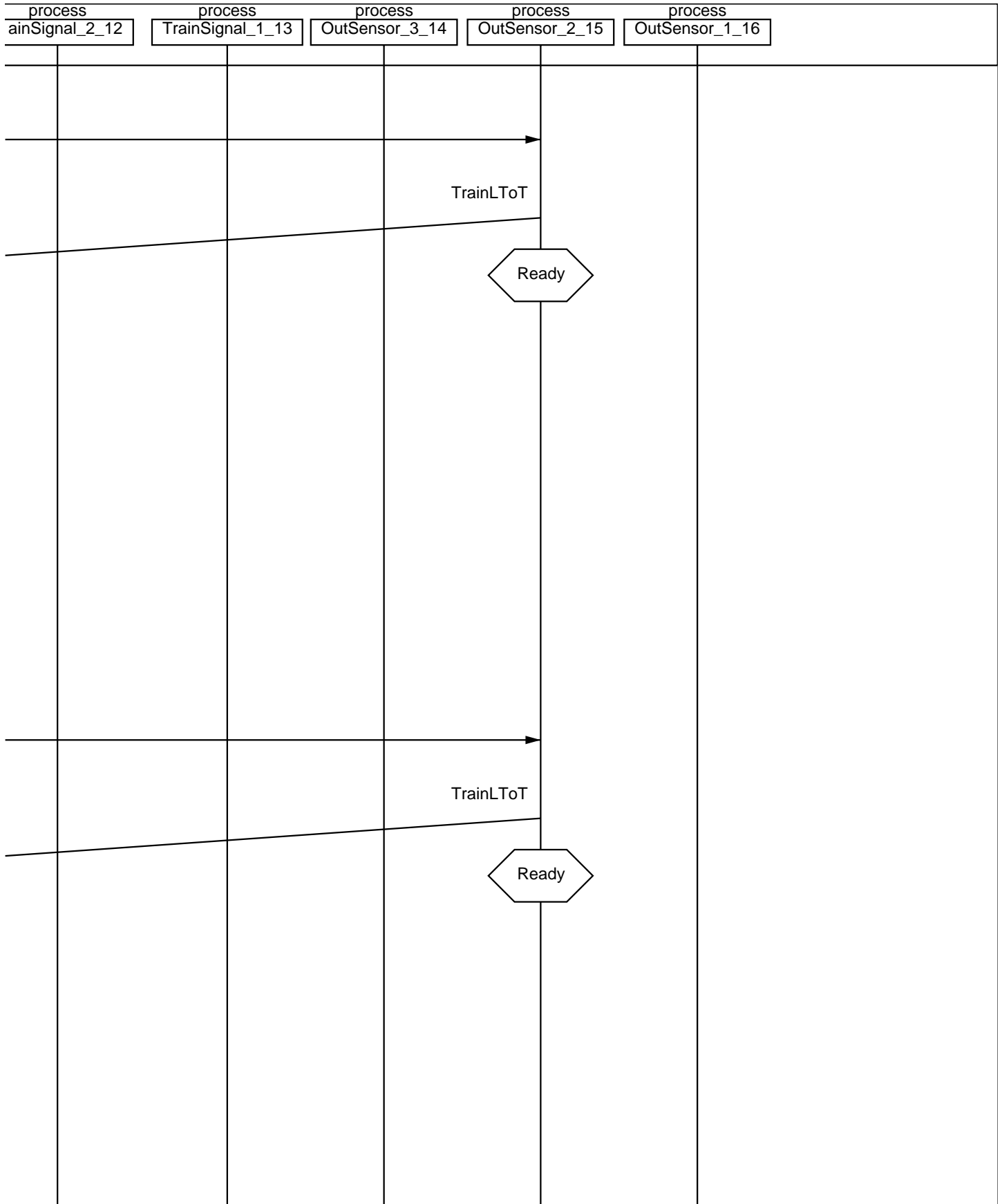
OutSensor_2_15

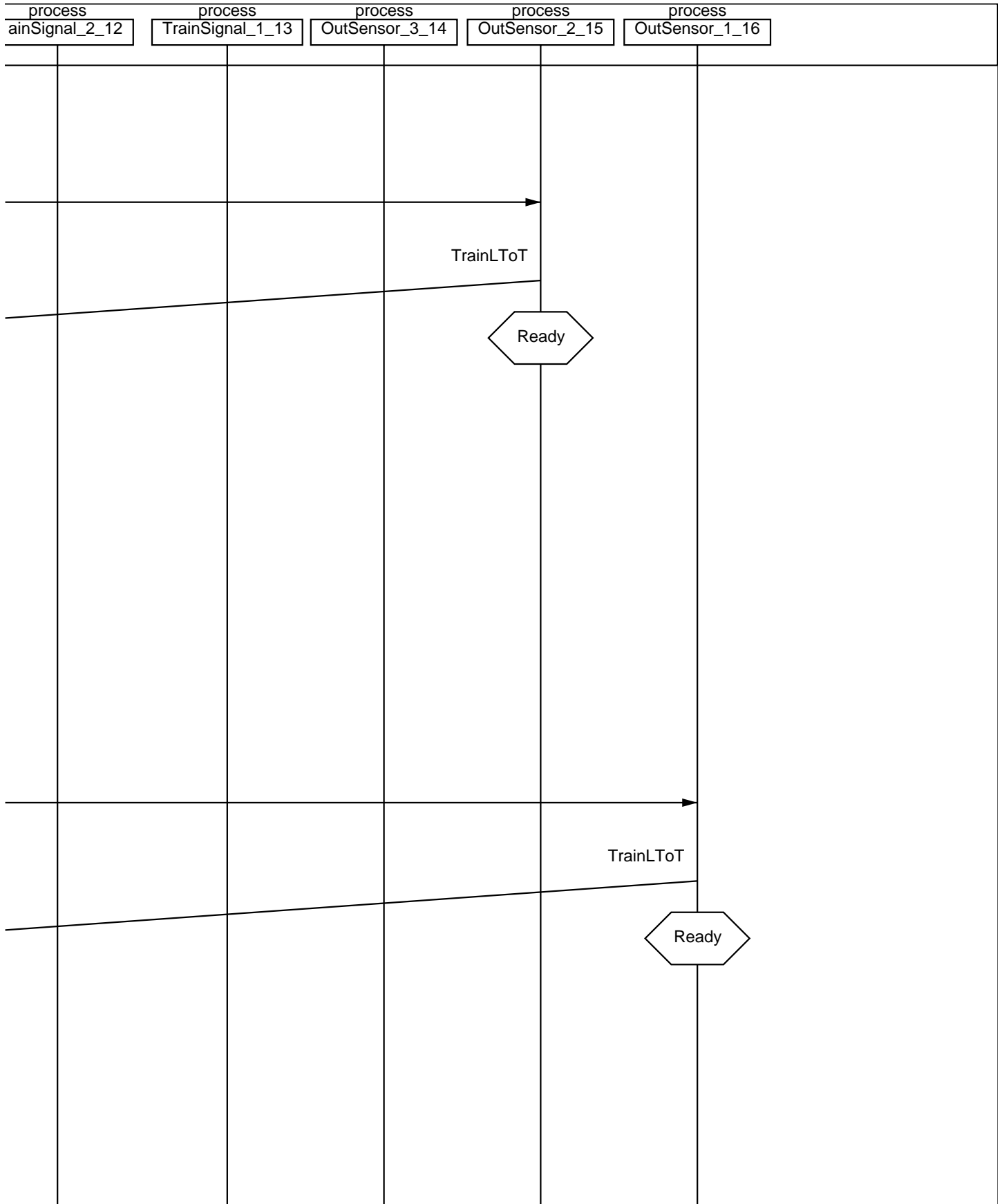
OutSensor_1_16

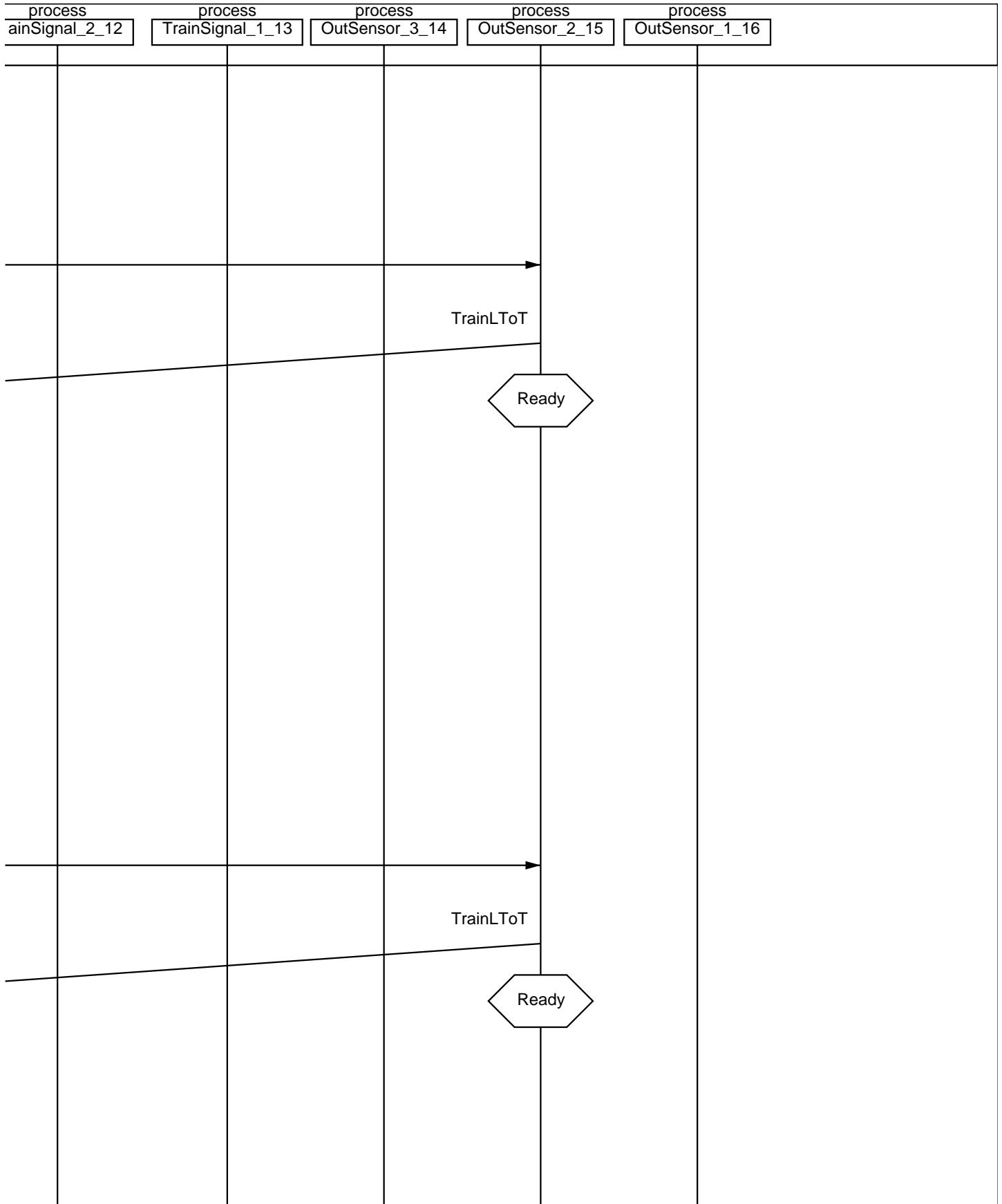
--	--	--	--	--	--

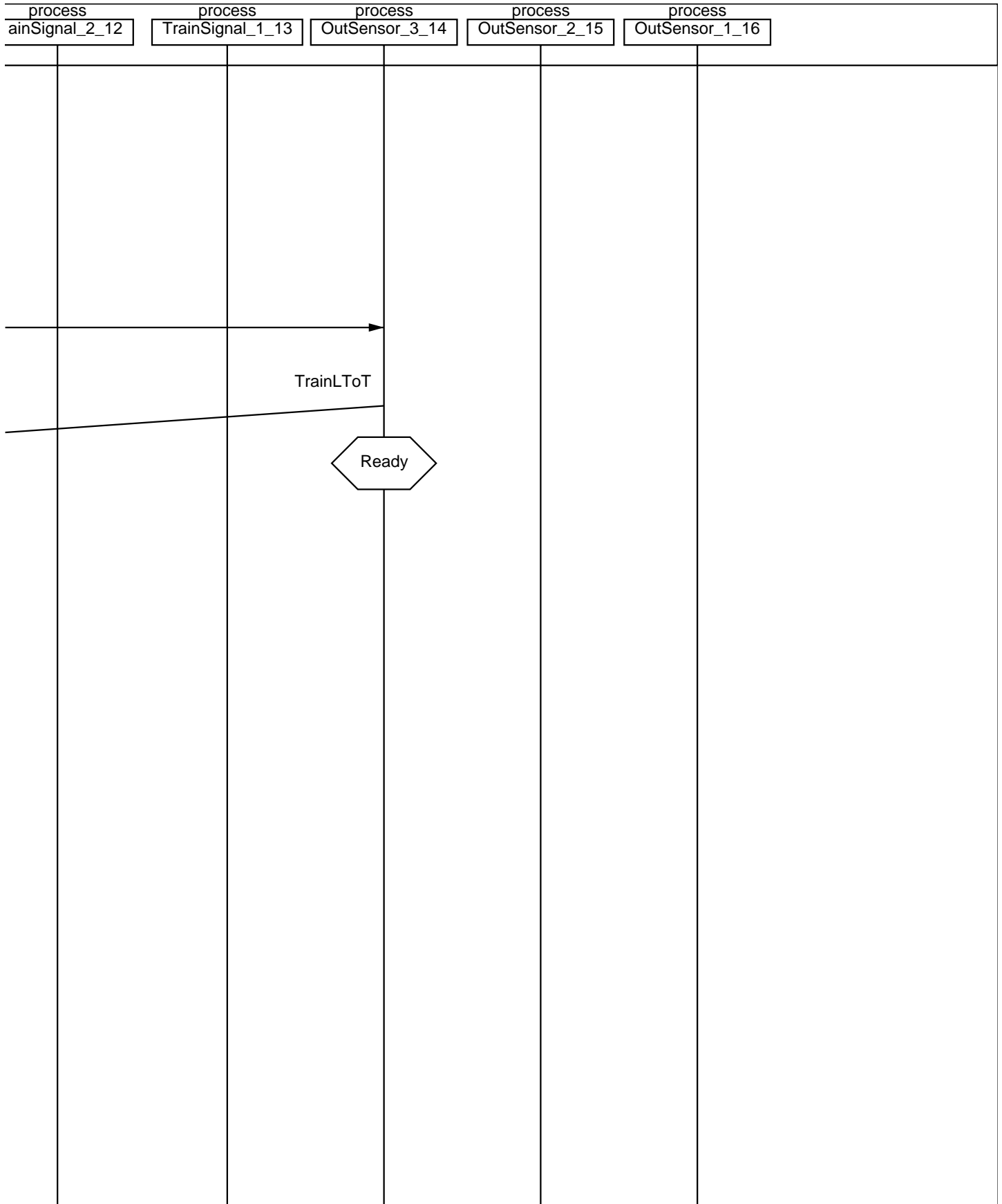


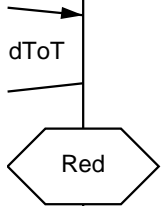
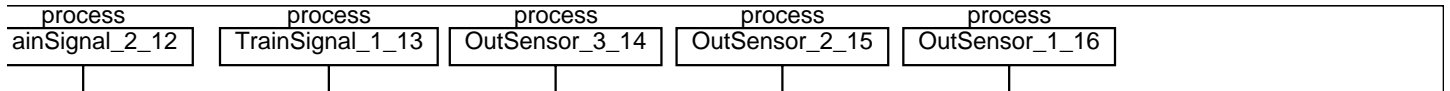


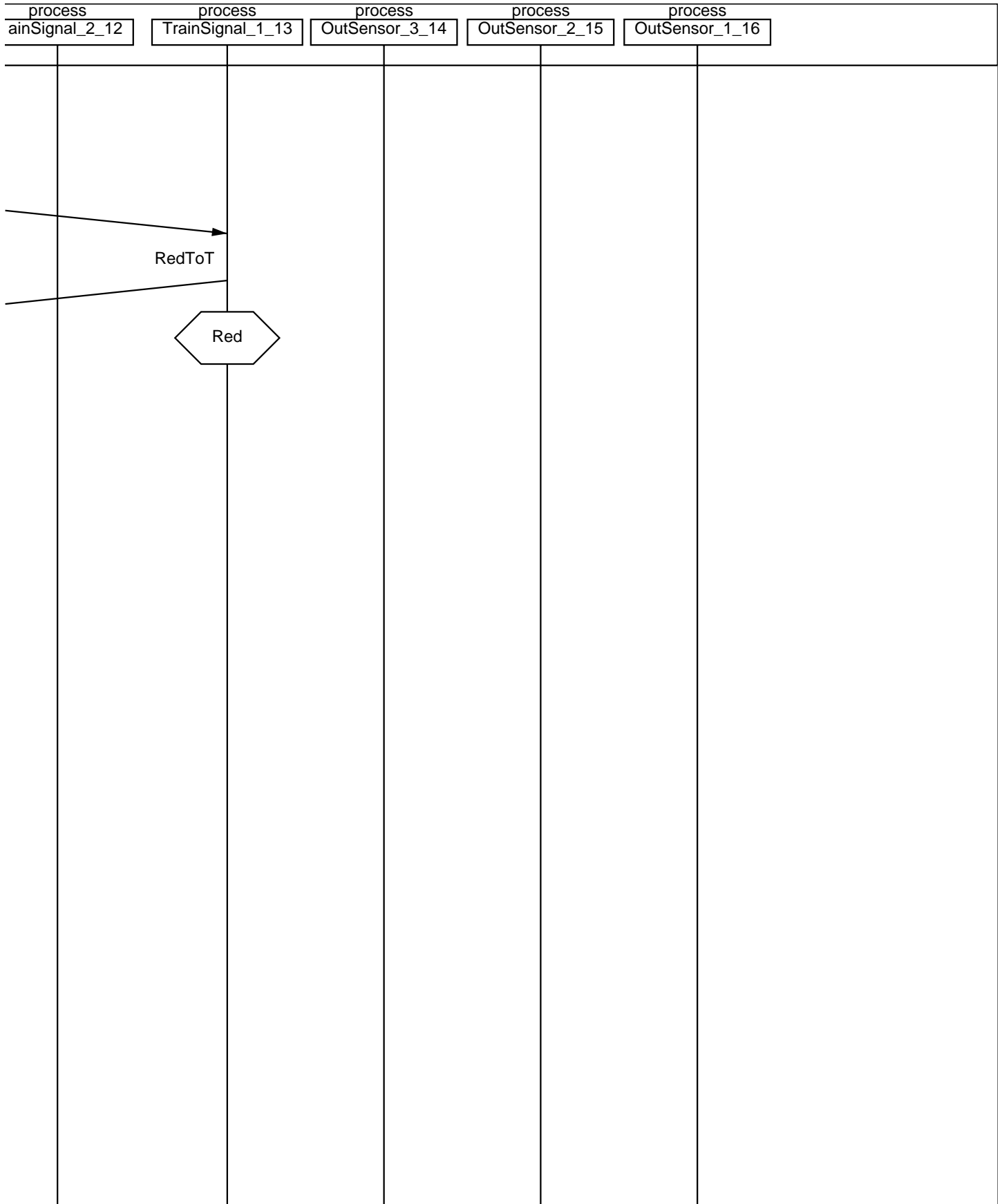








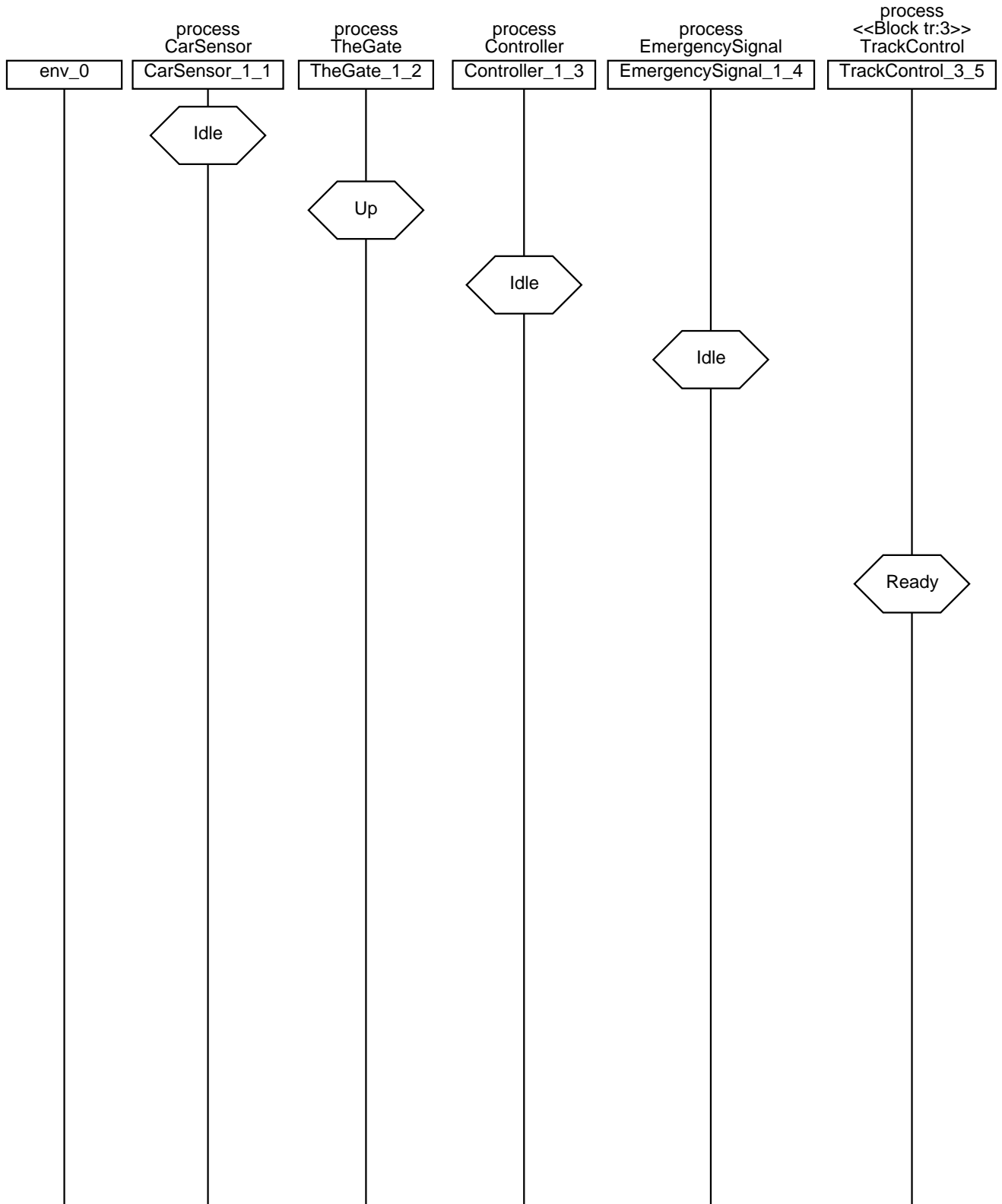


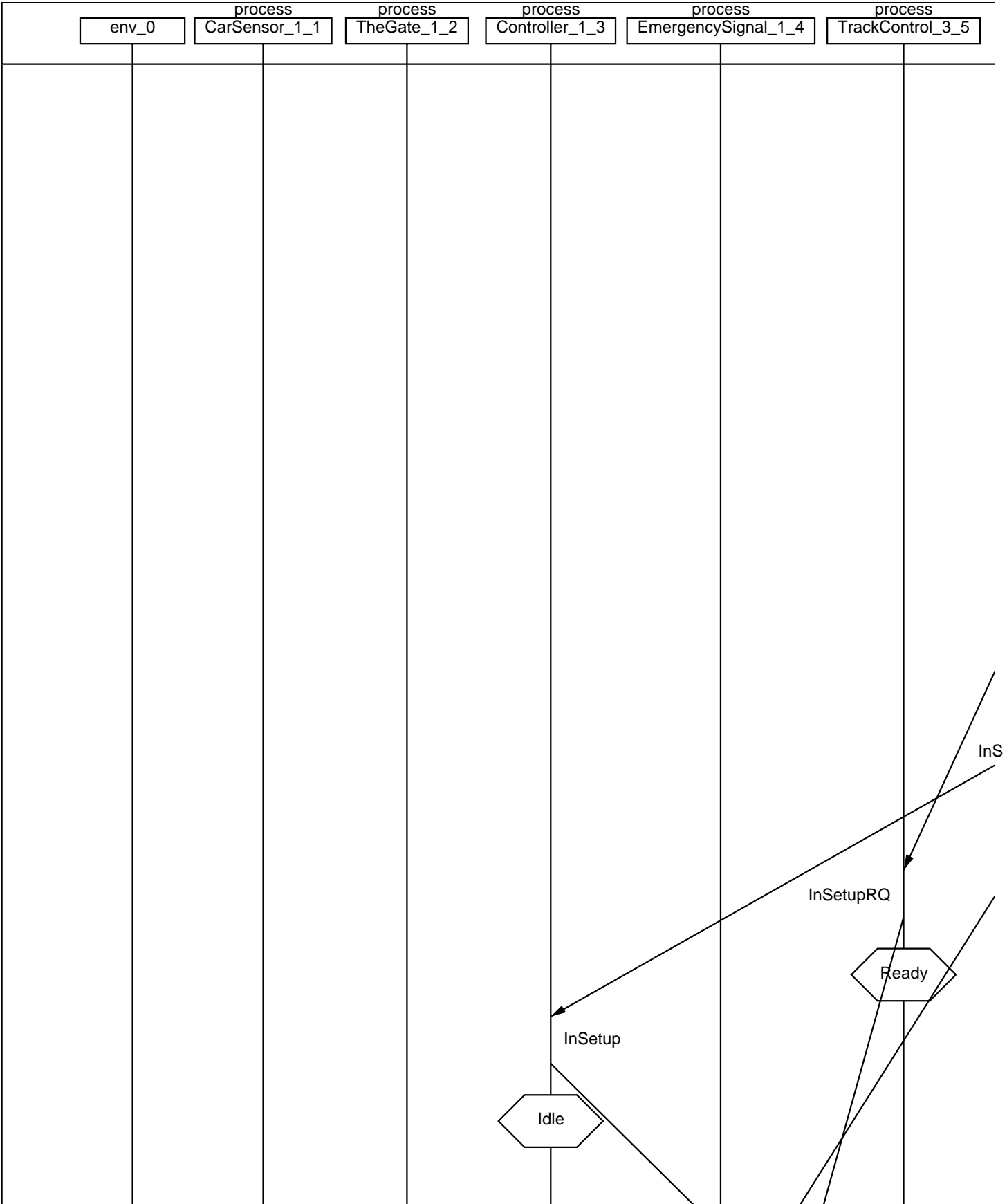


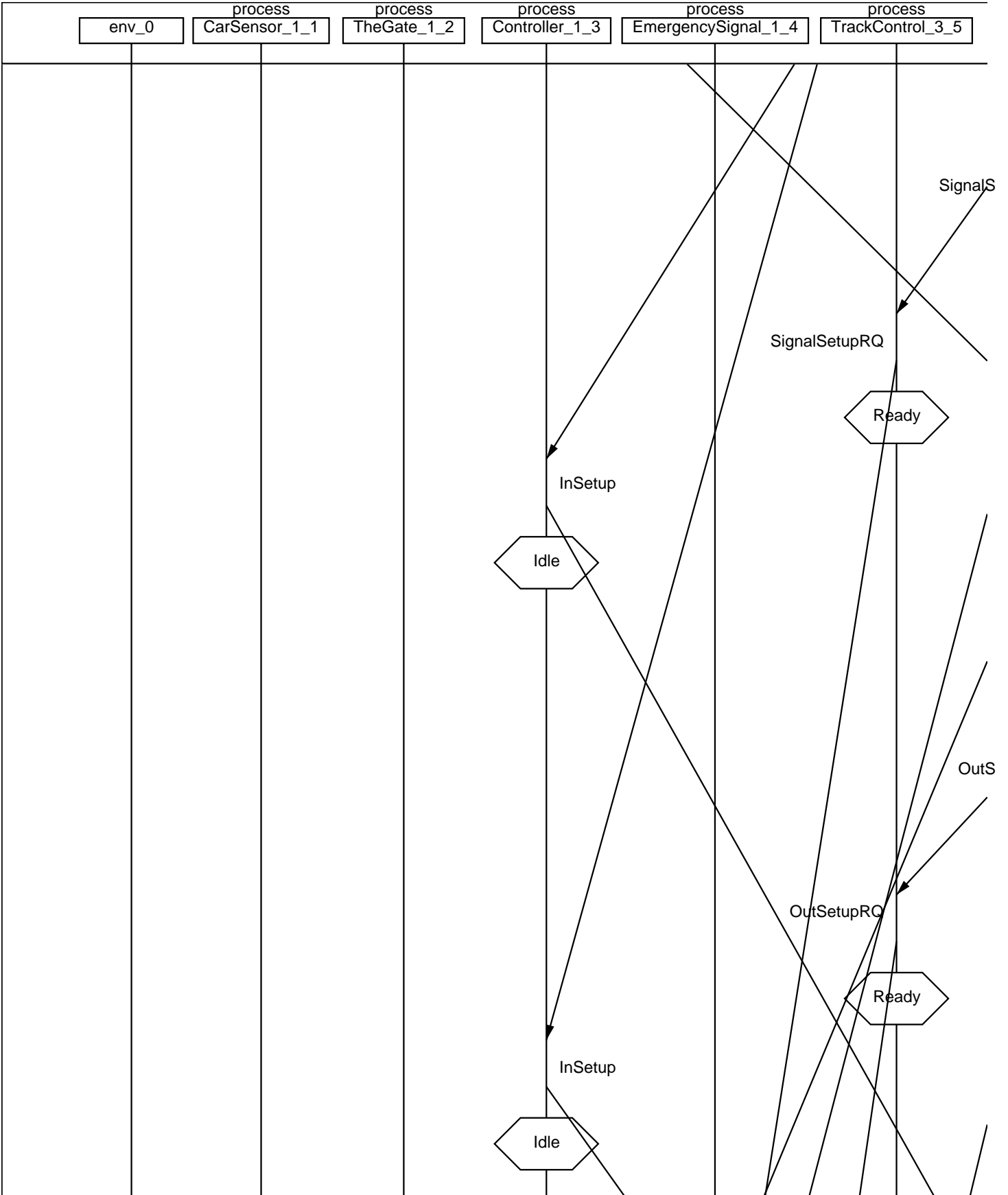
process ainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16

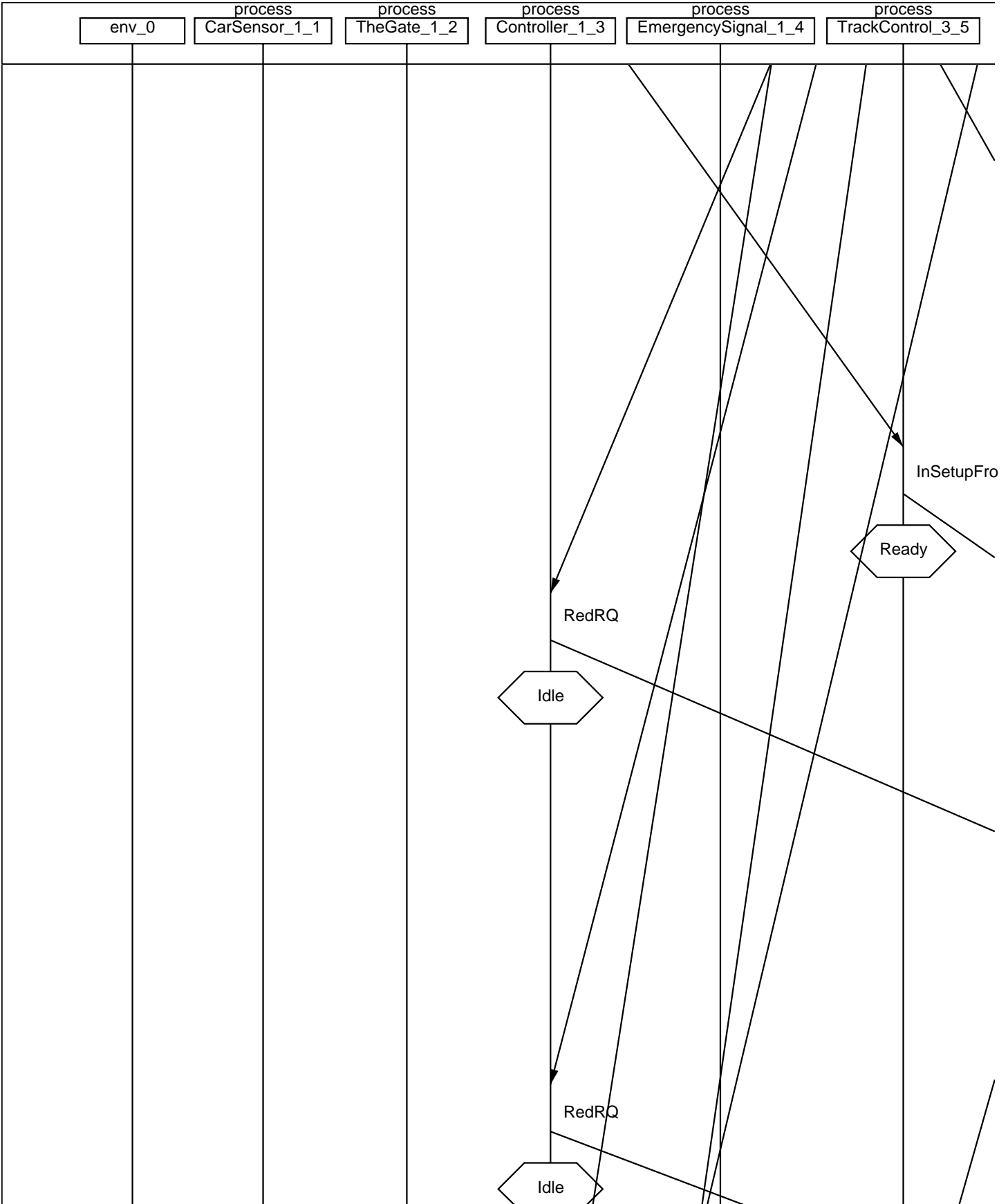
MSC CompleteMSC_TestCaseD_Strategy4

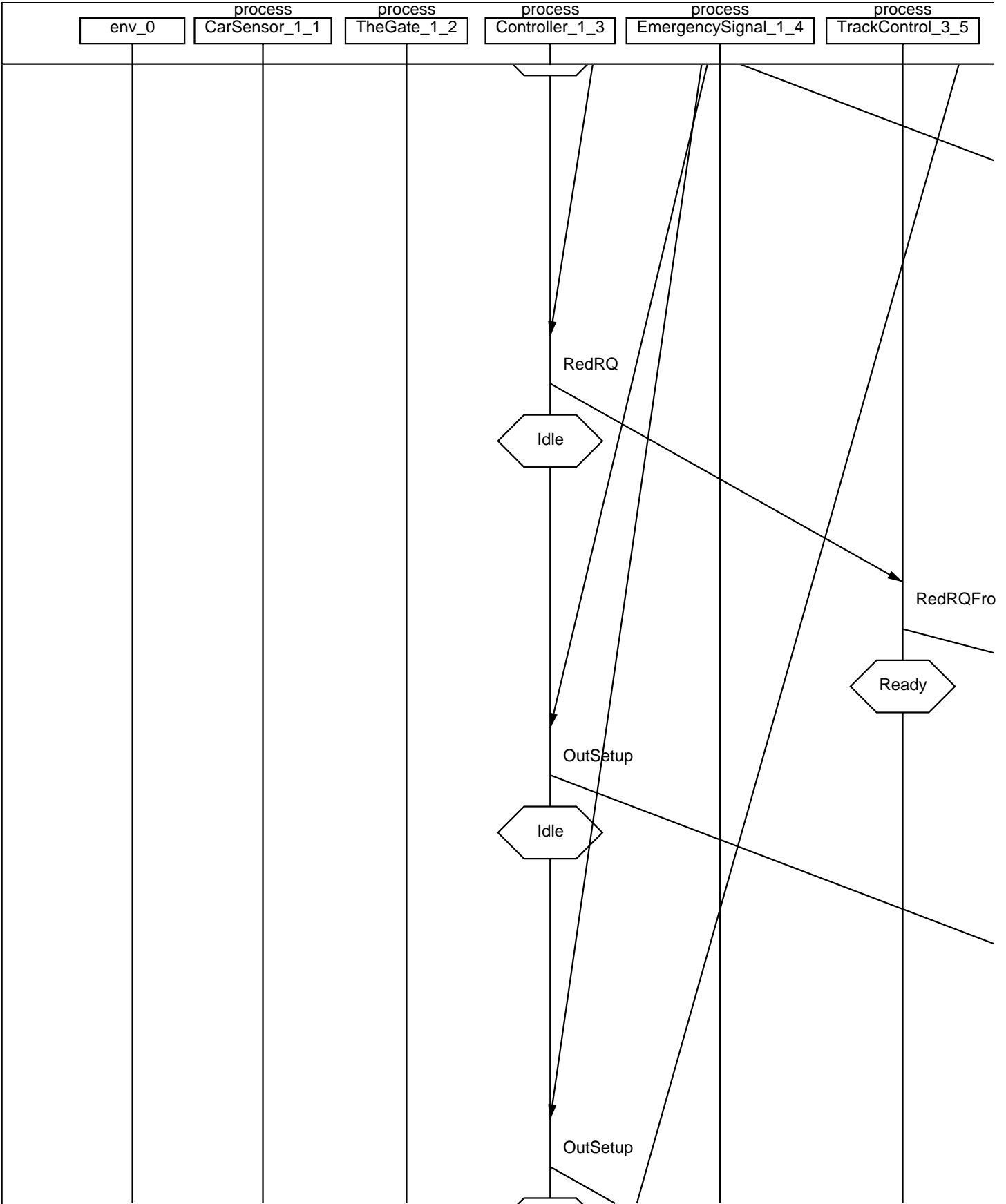
Simulation trace
generated by
SDL Simulator 4.3

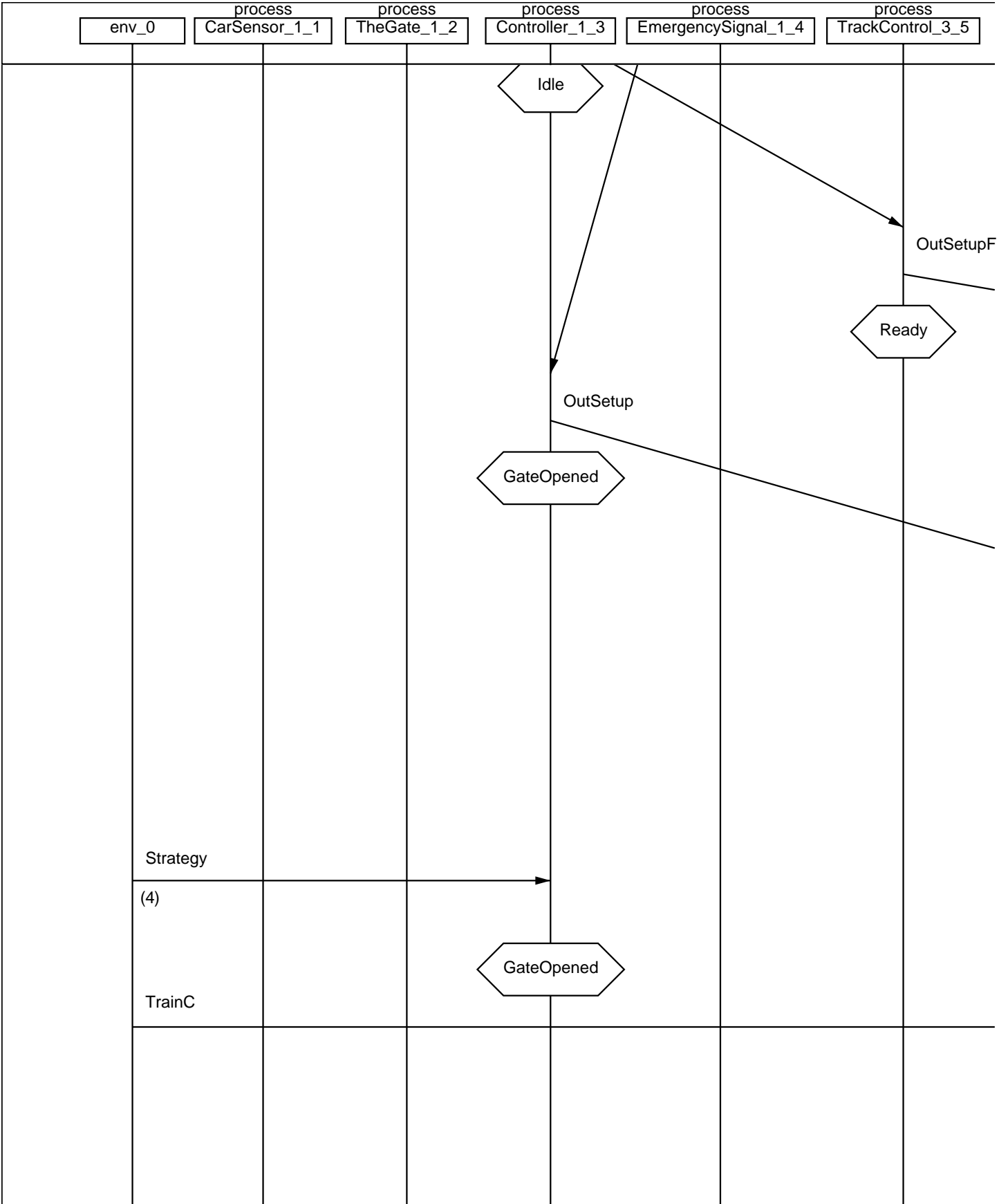


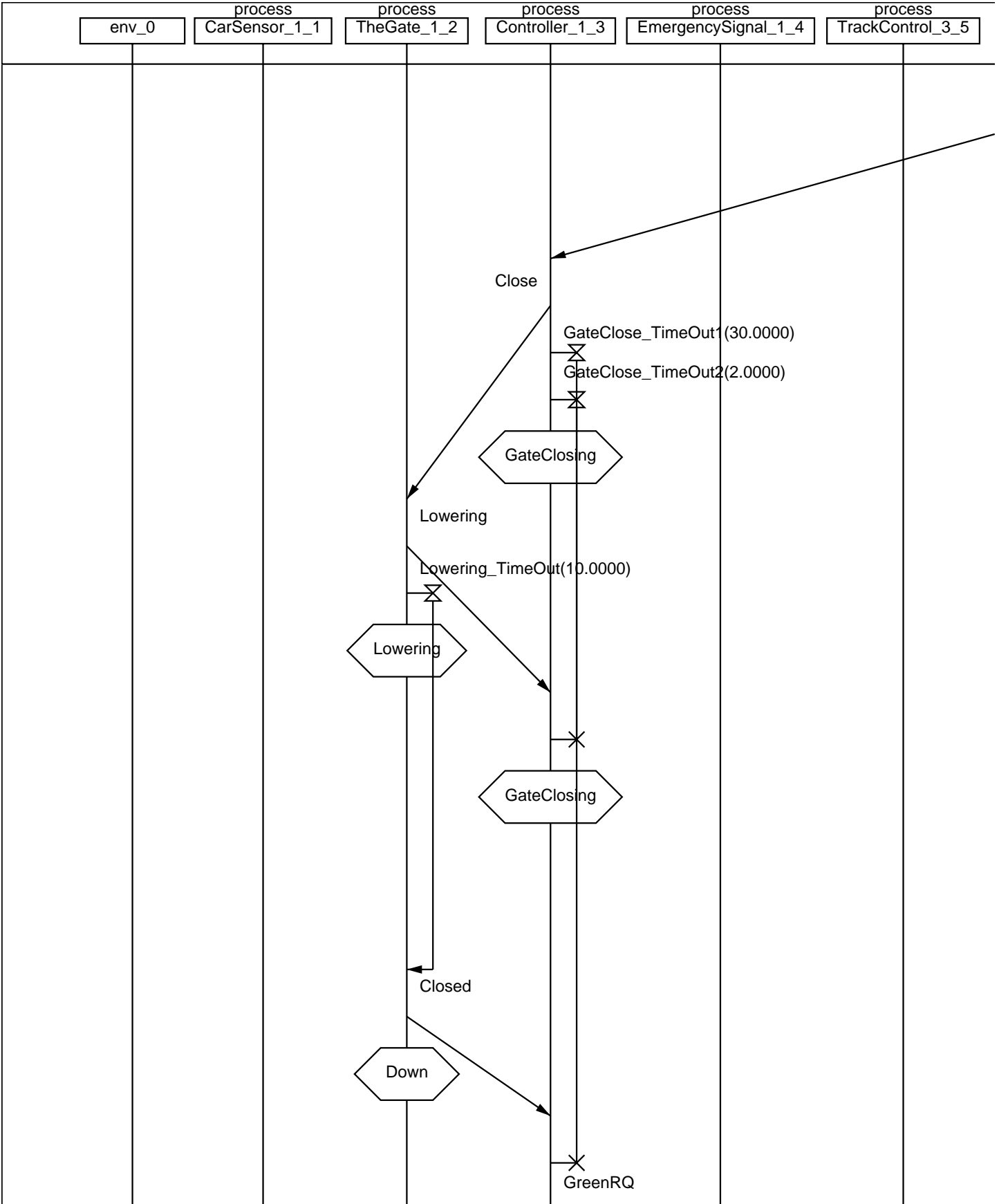


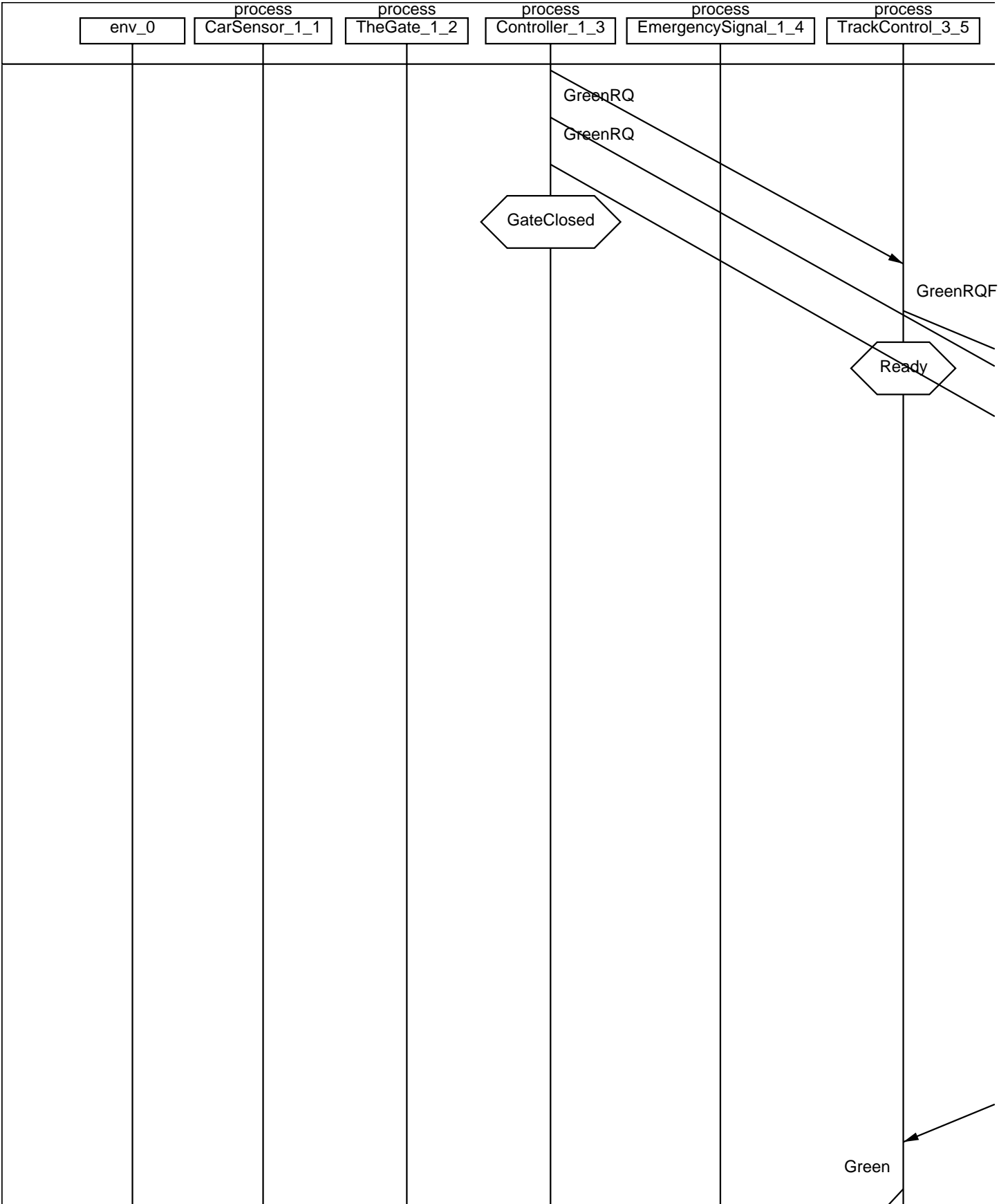


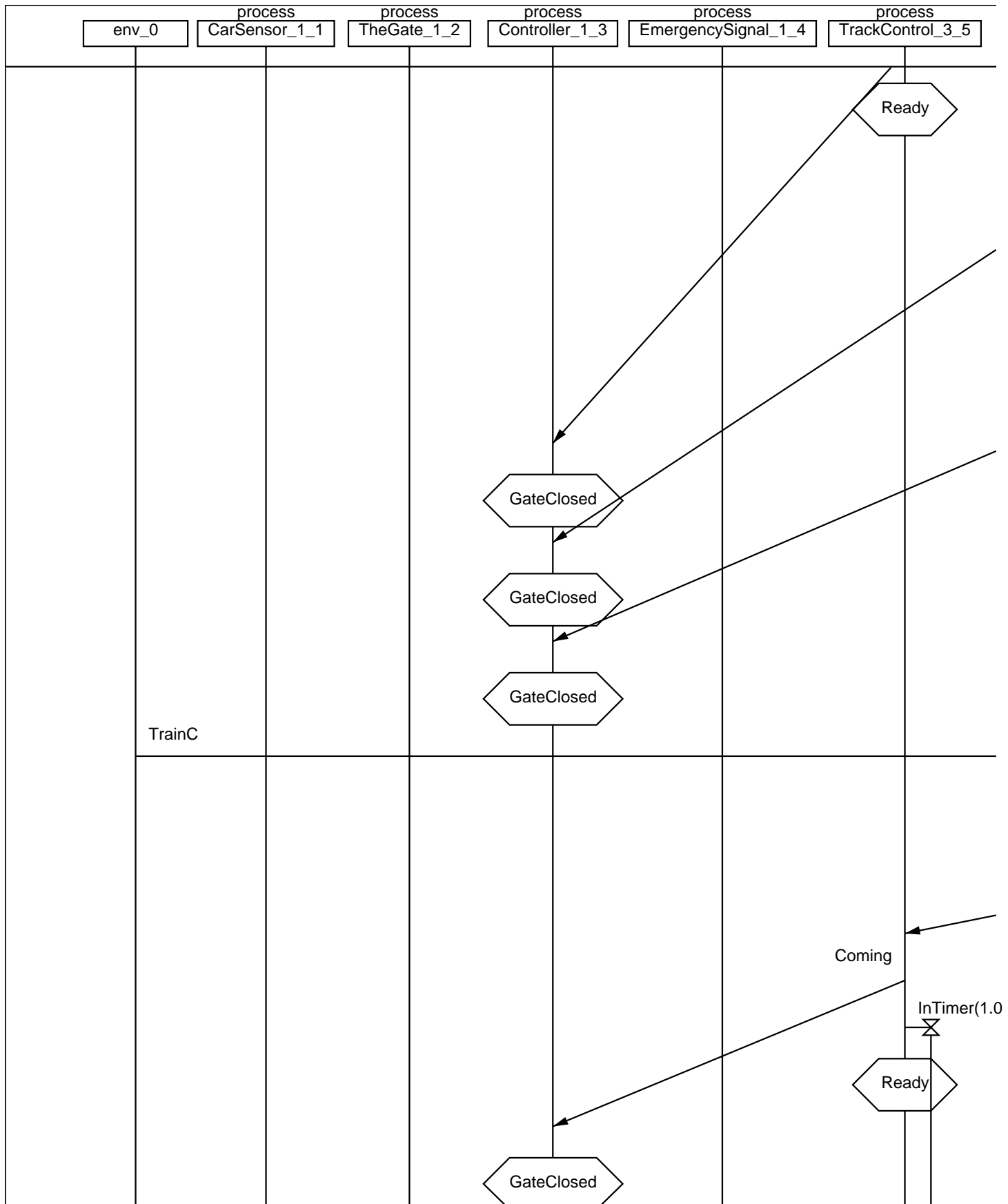


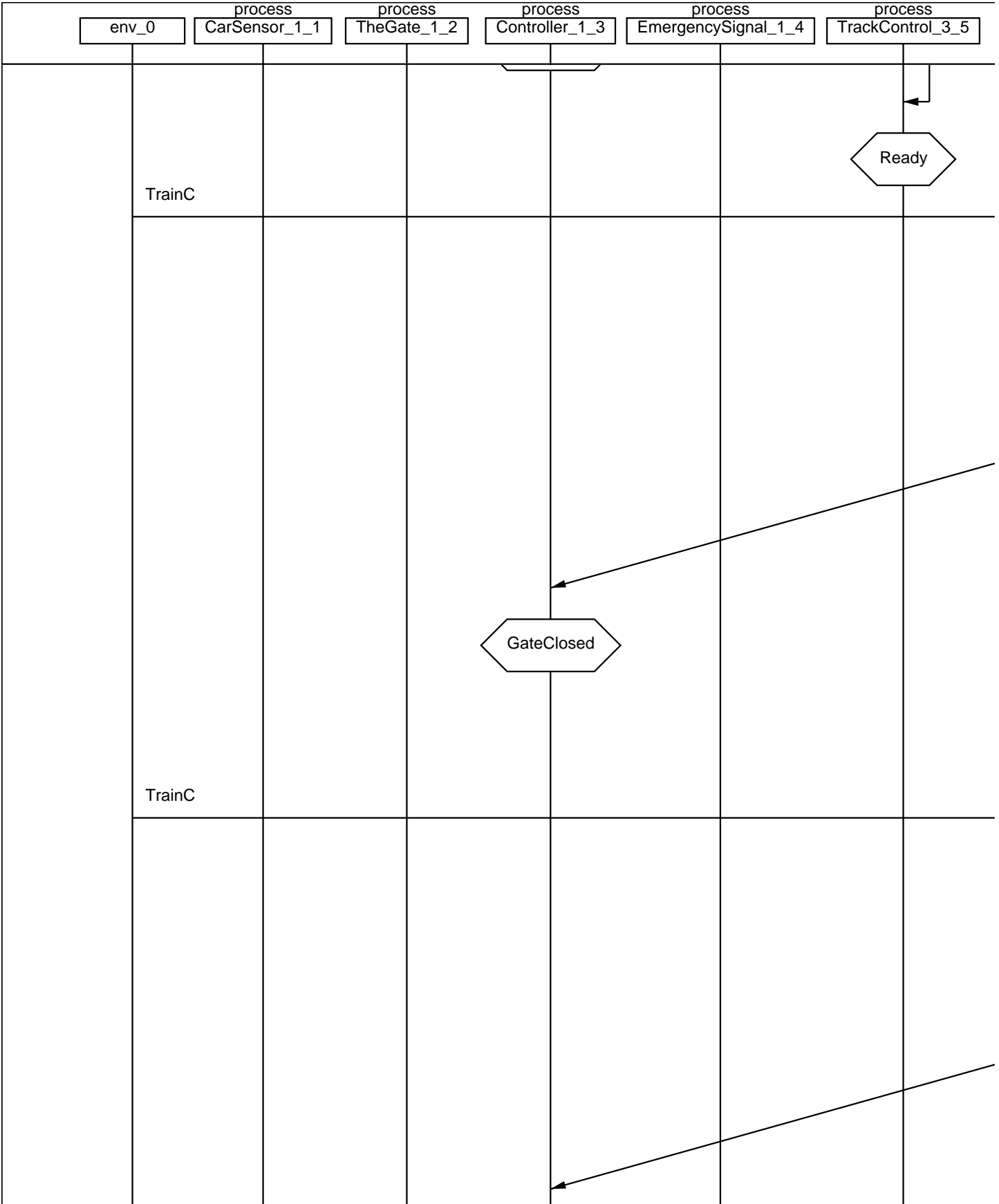


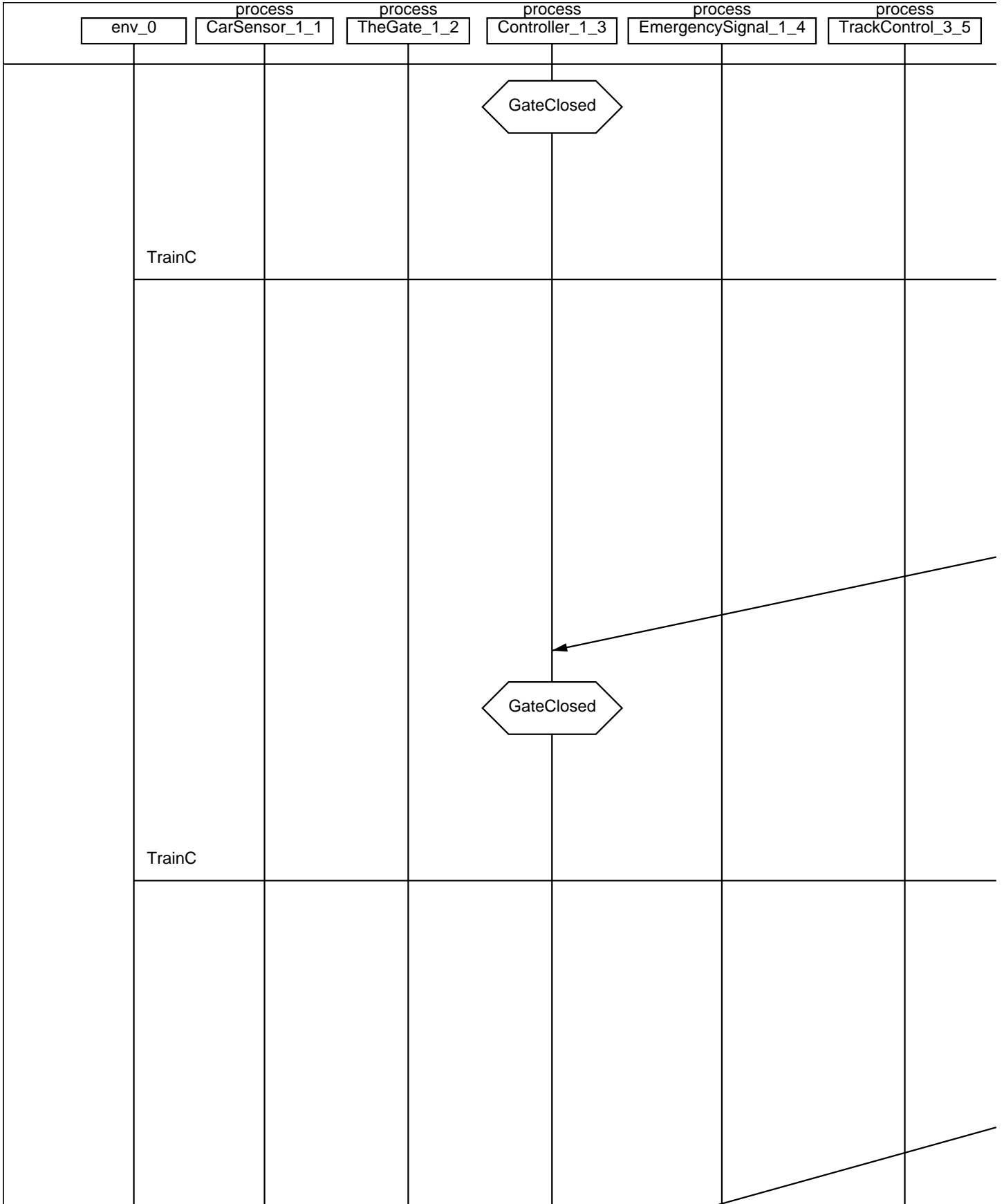


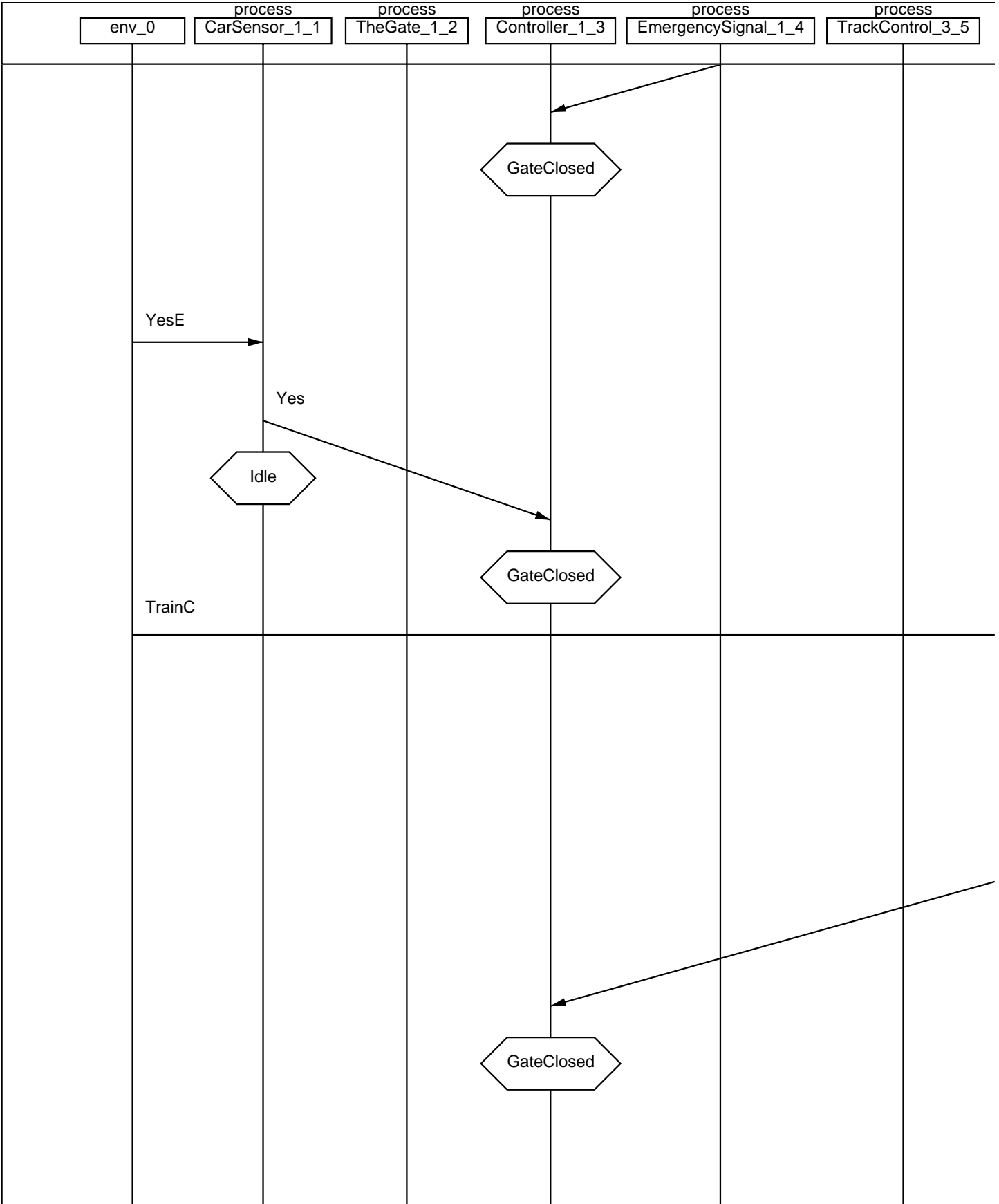


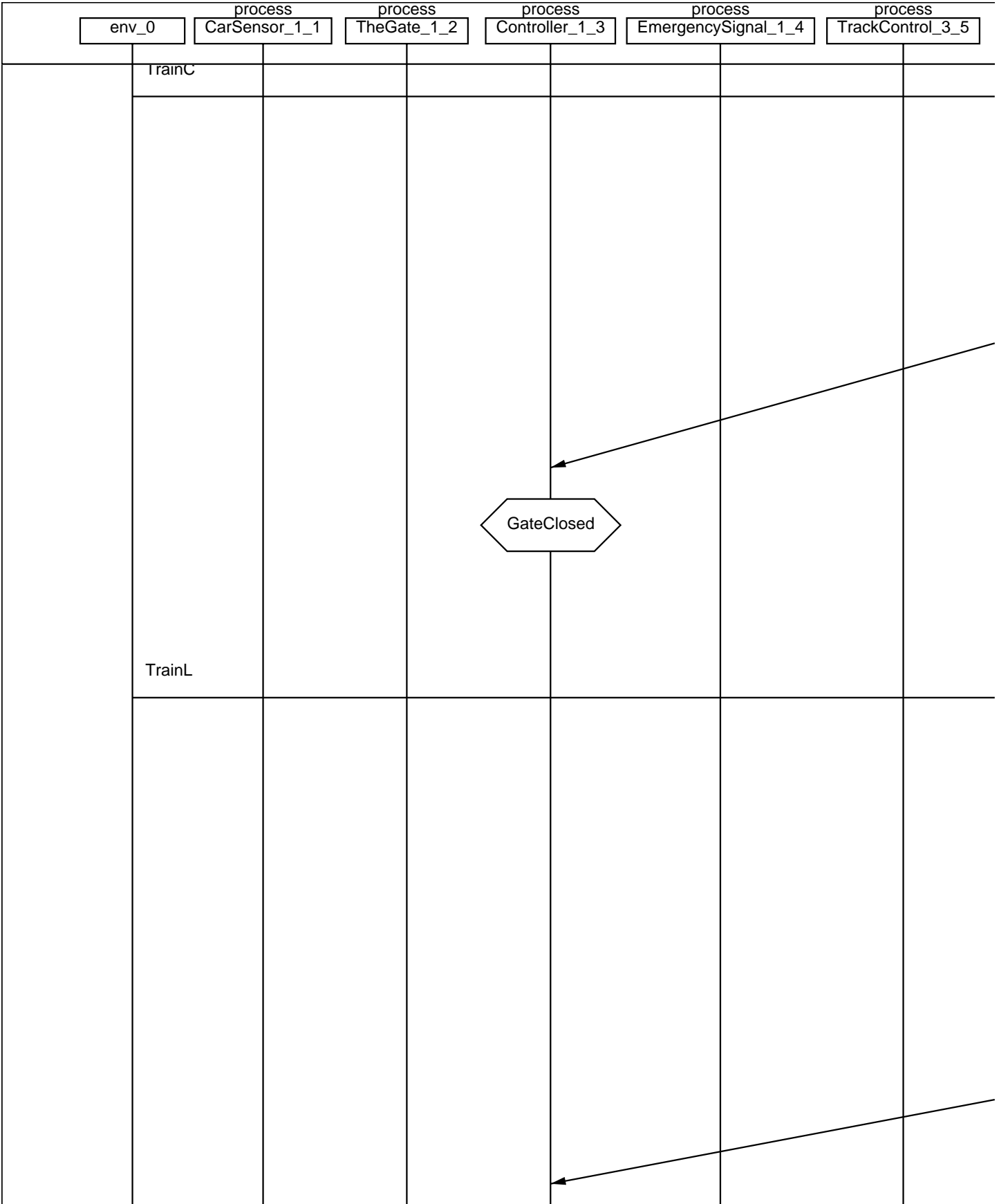


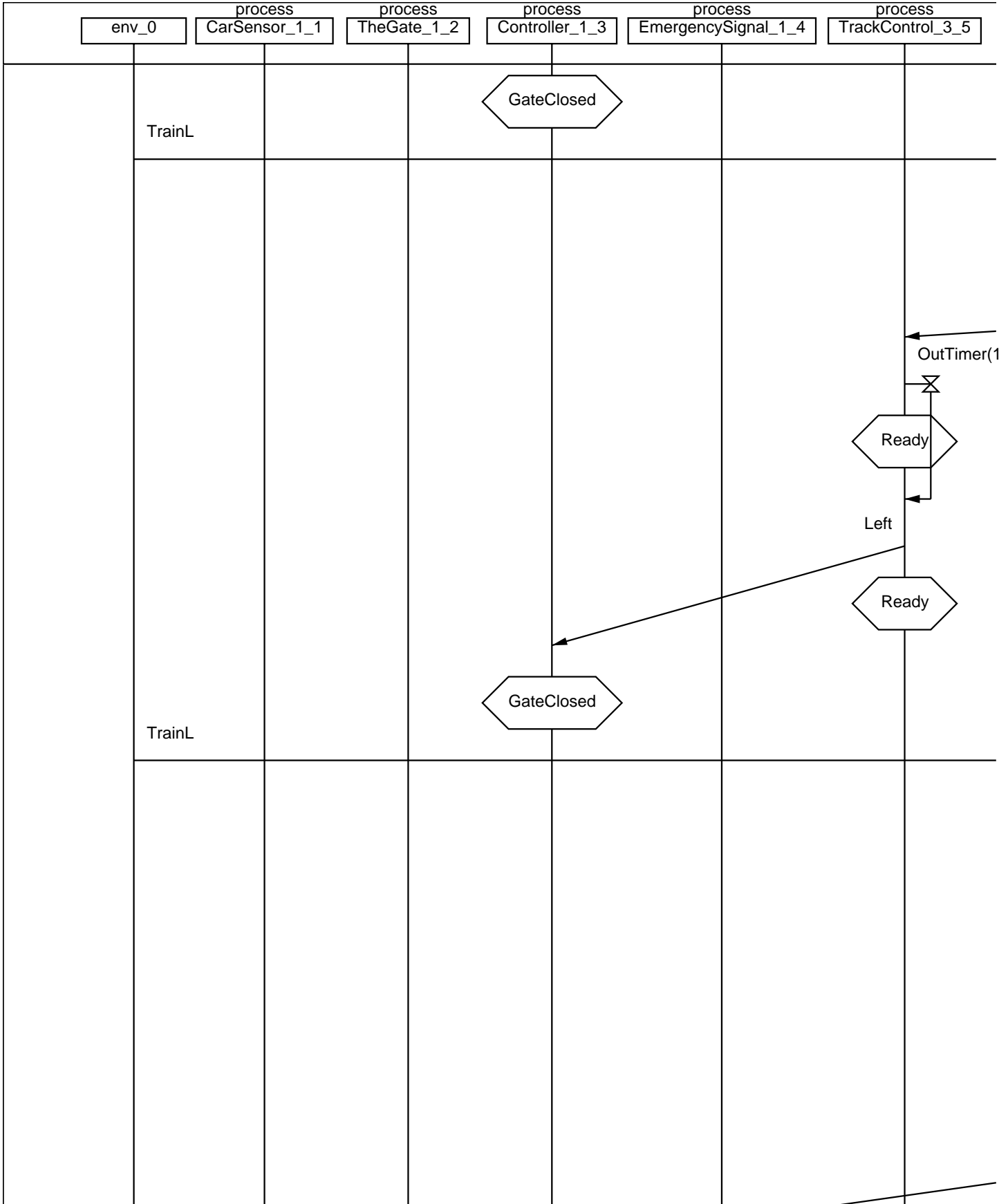


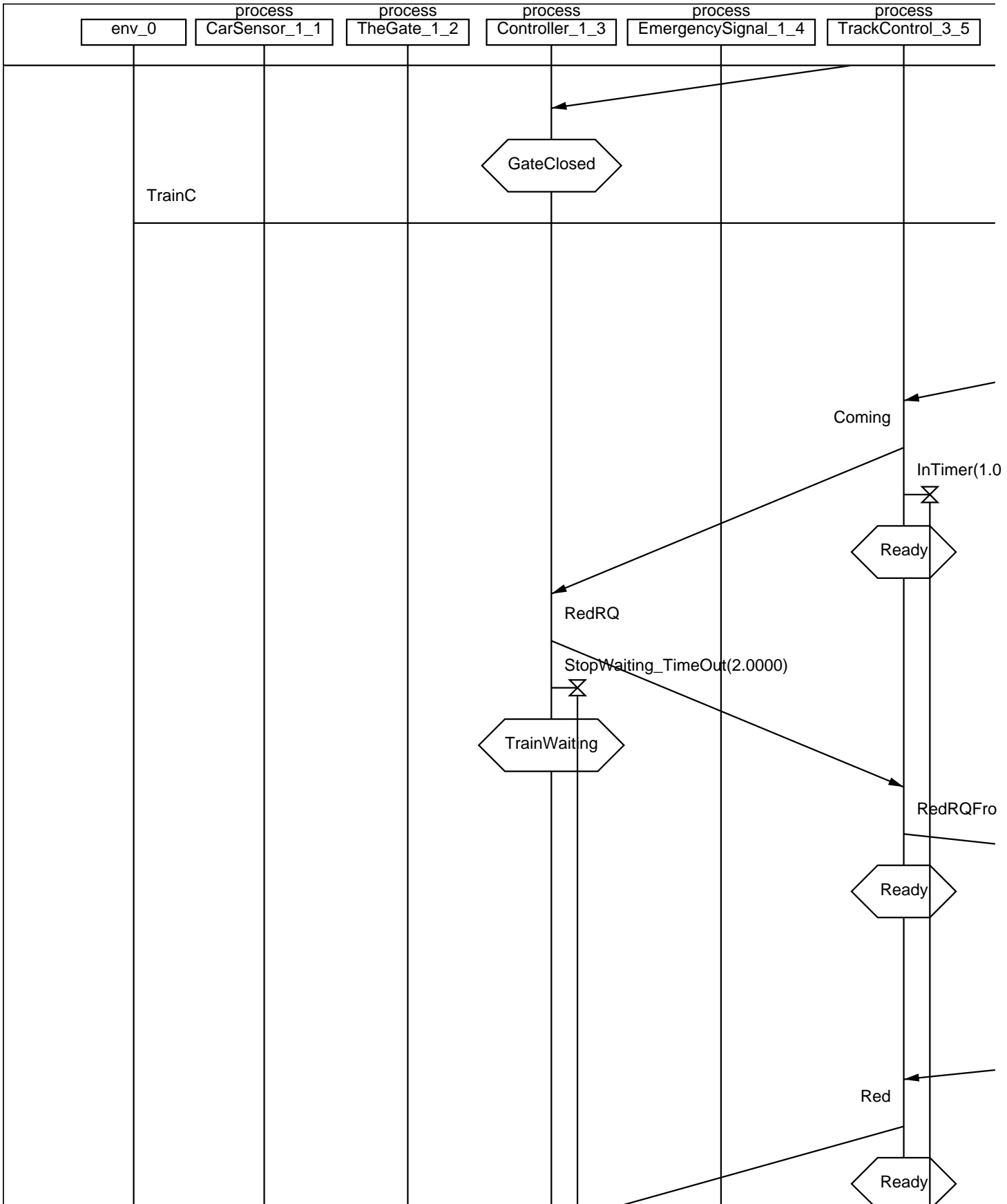


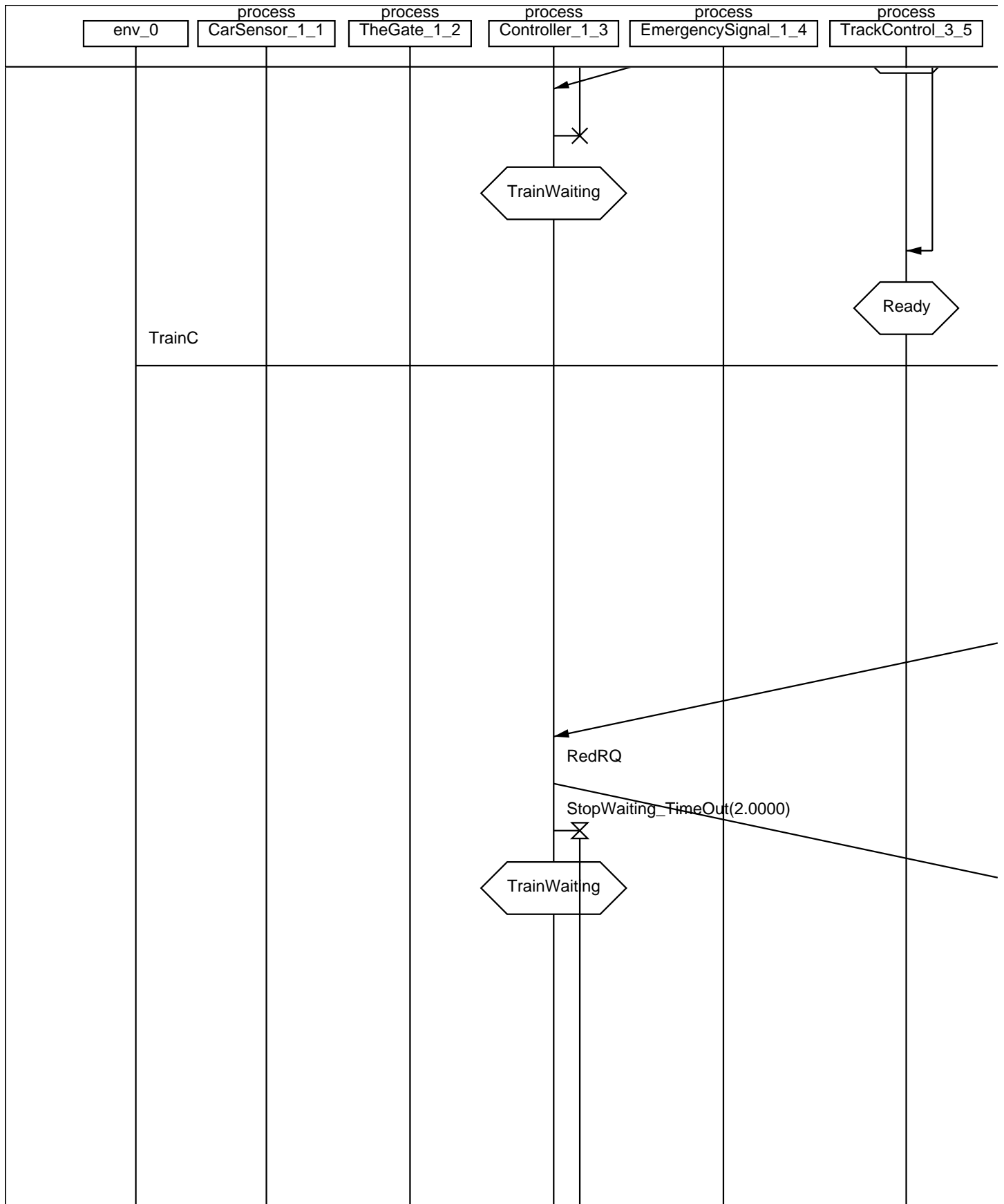


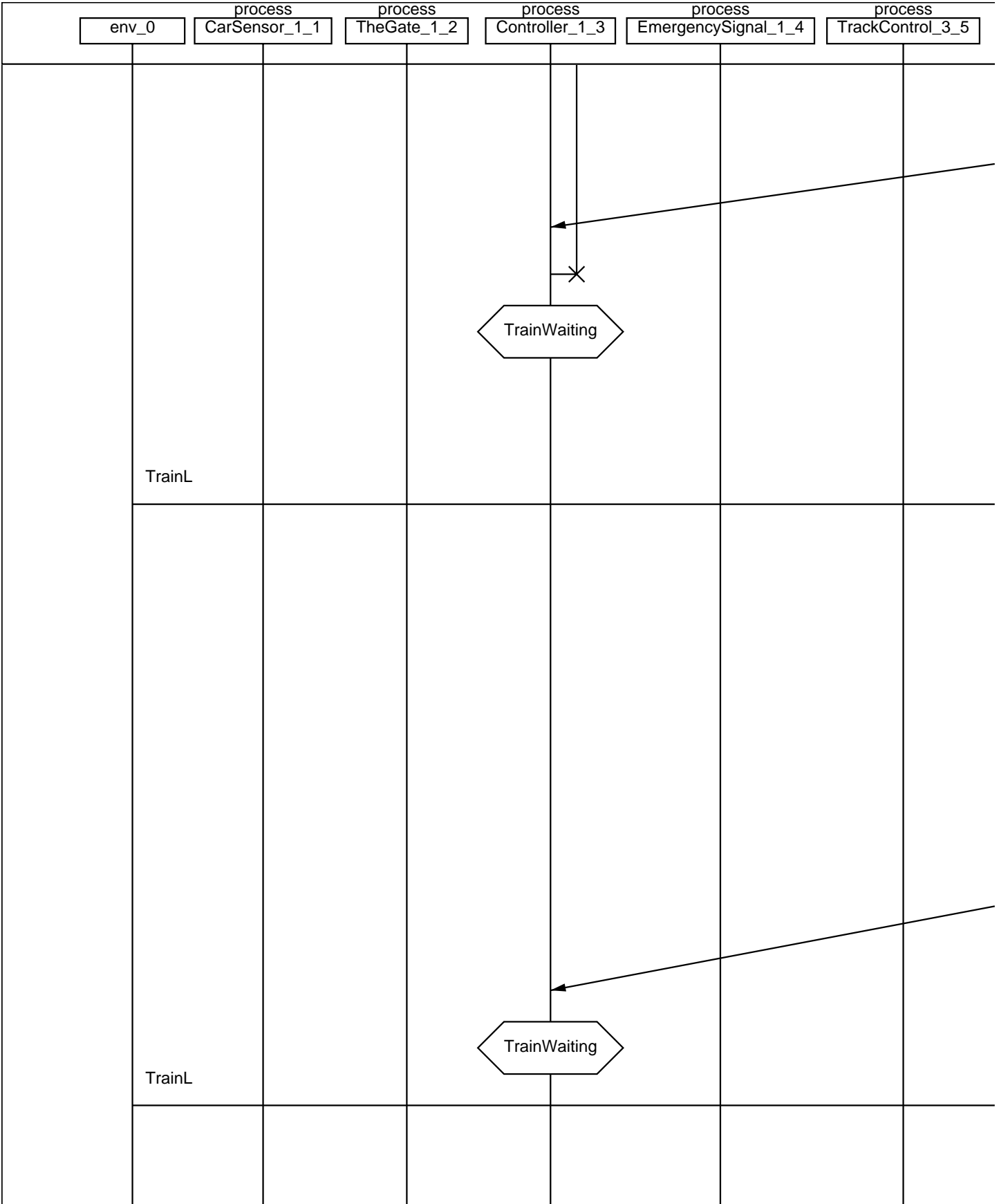


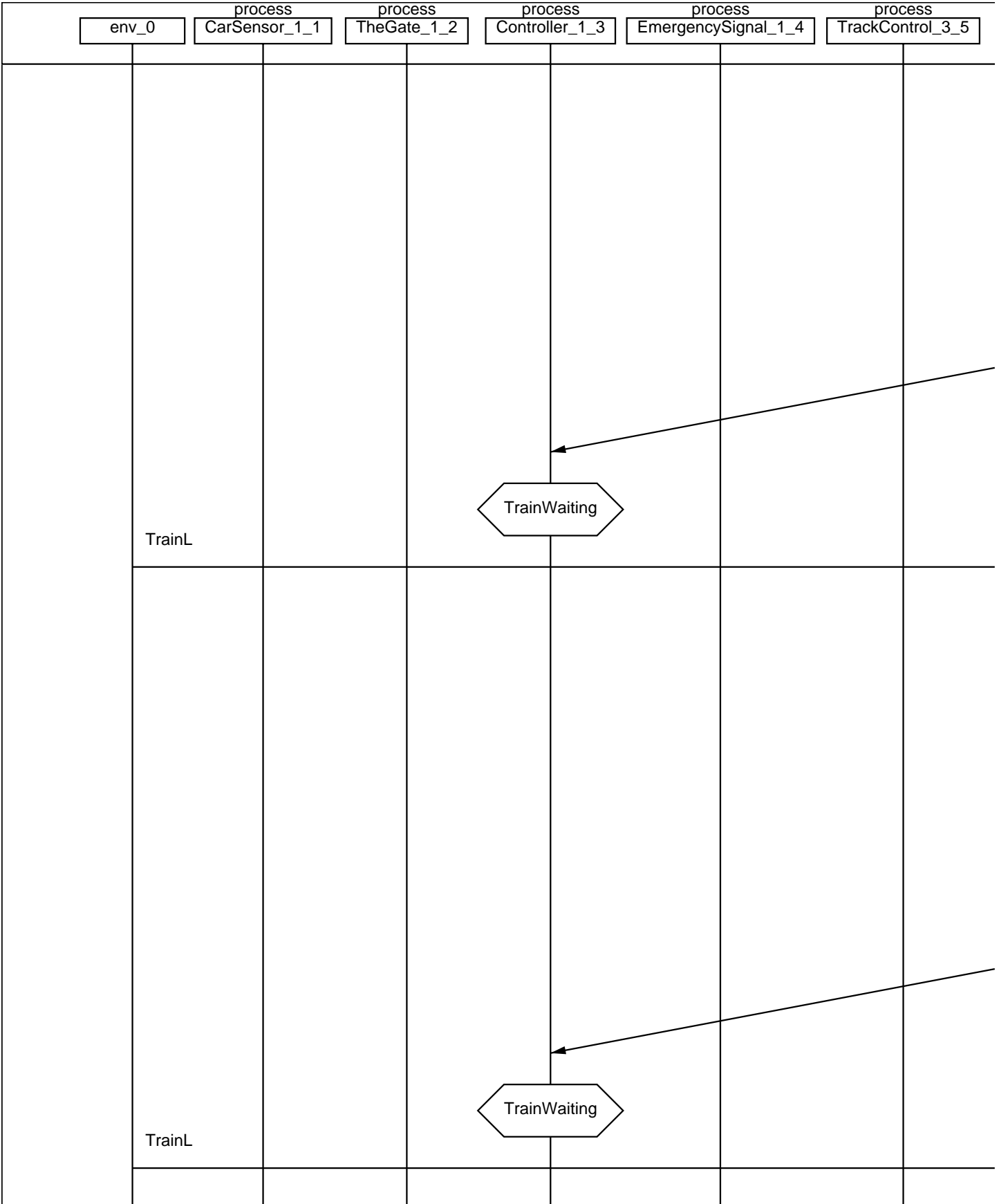


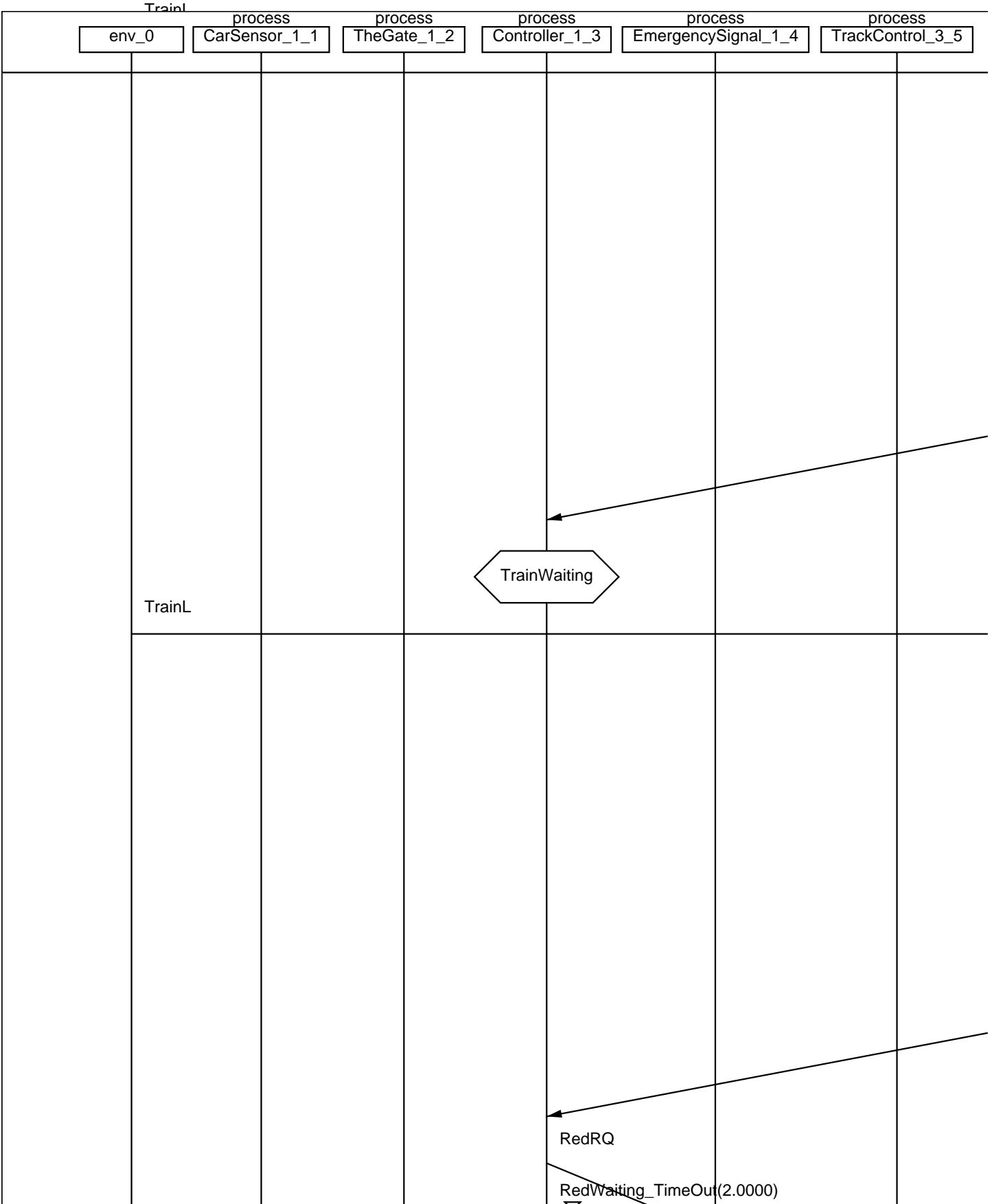


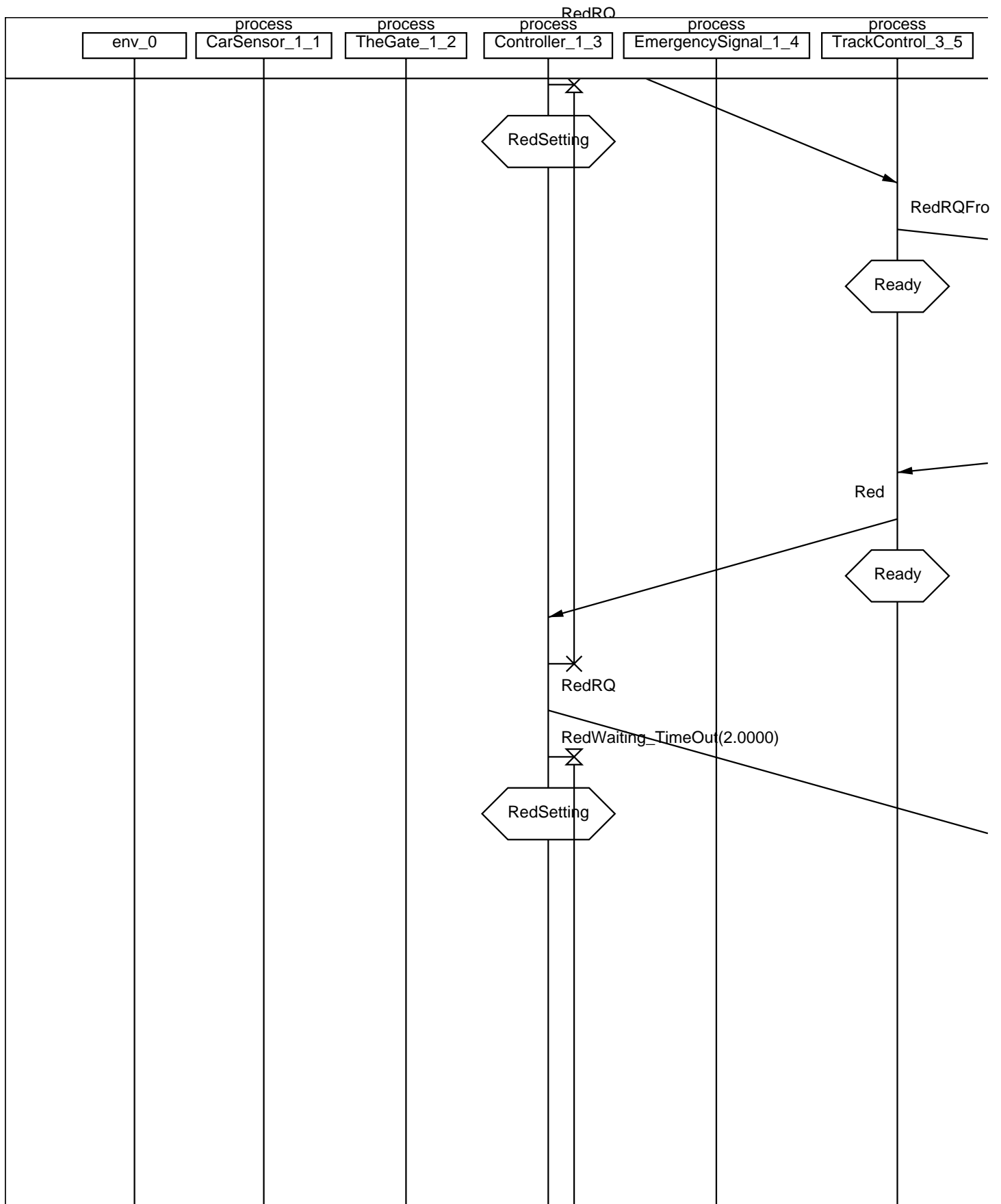


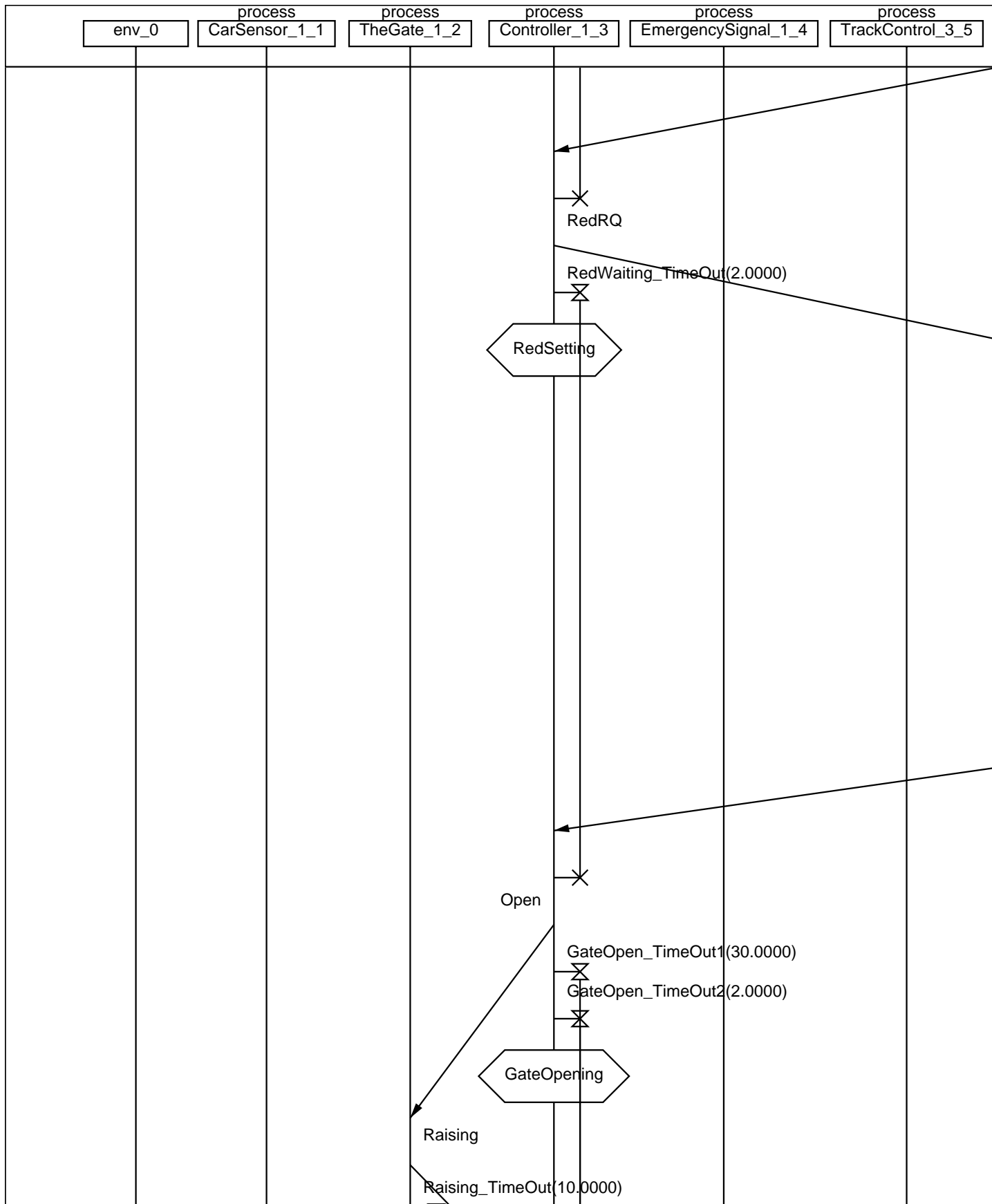


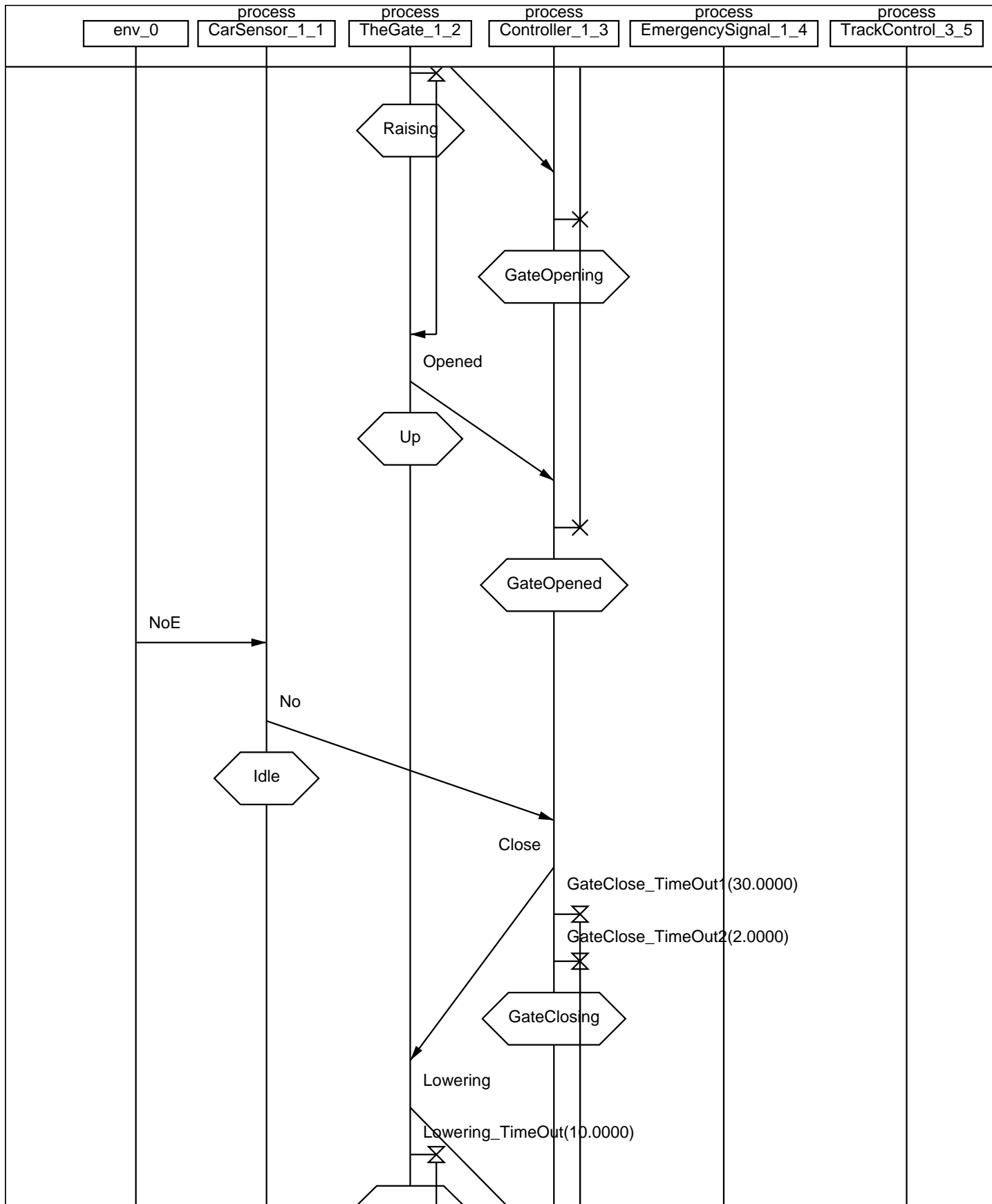


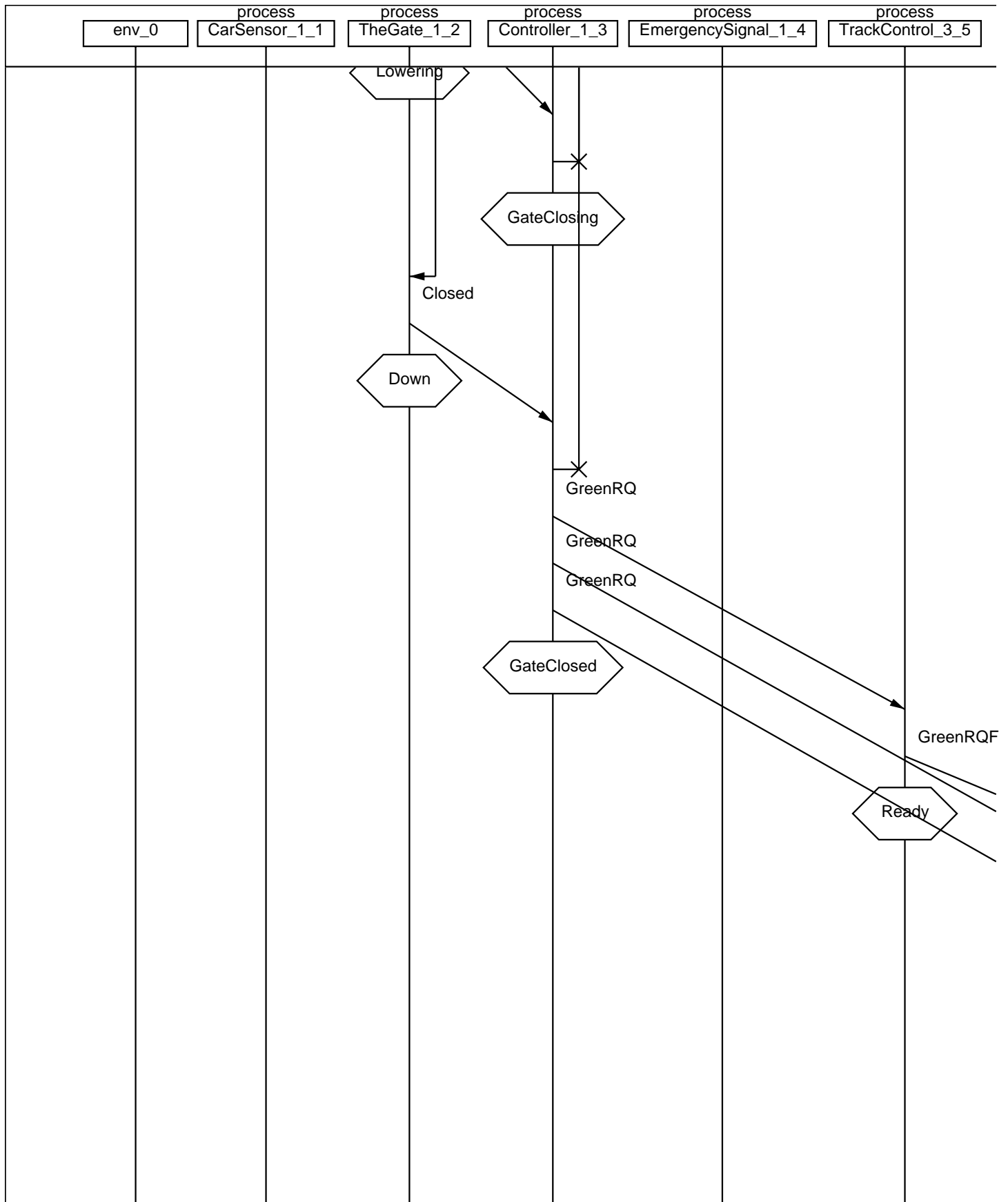


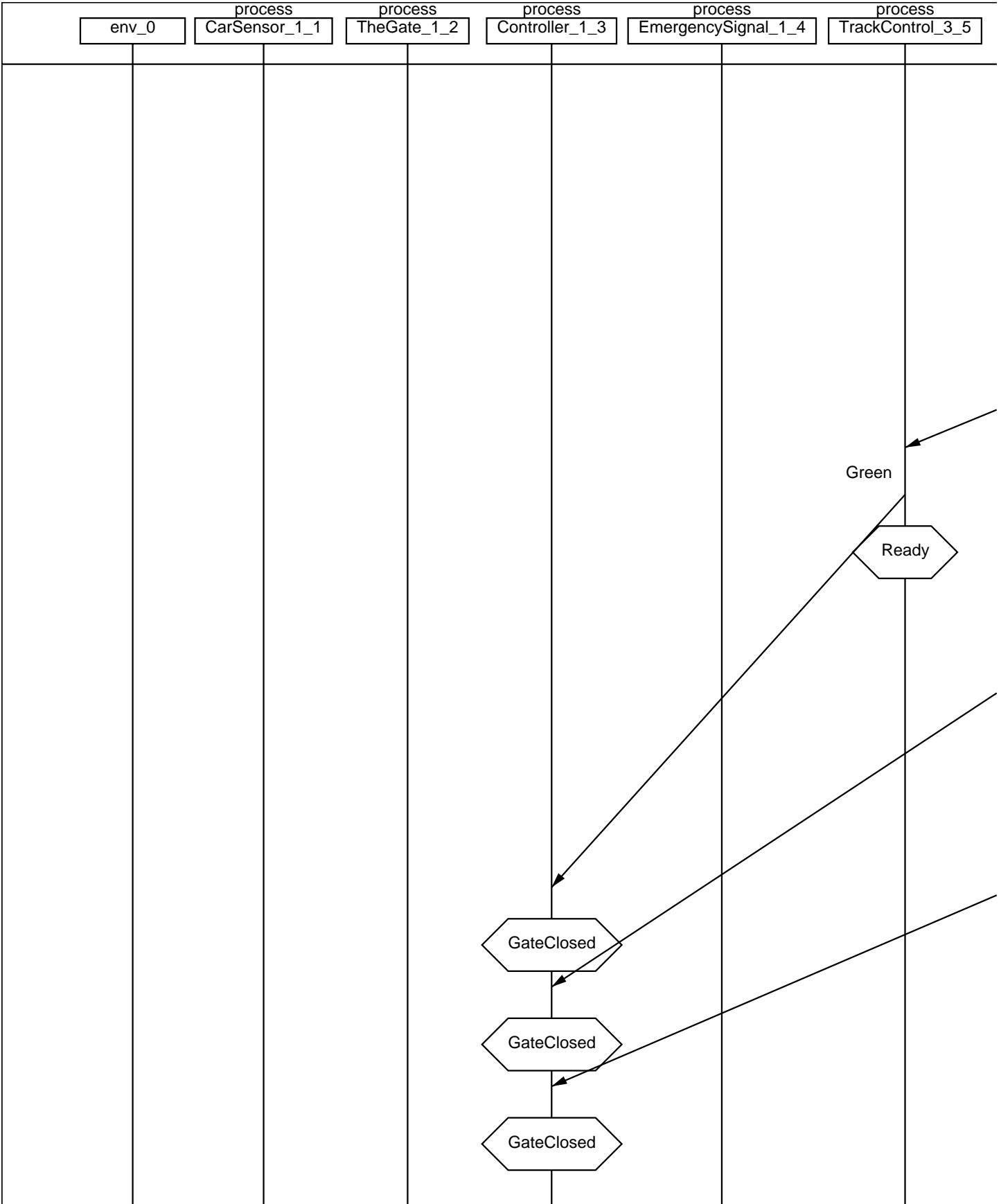


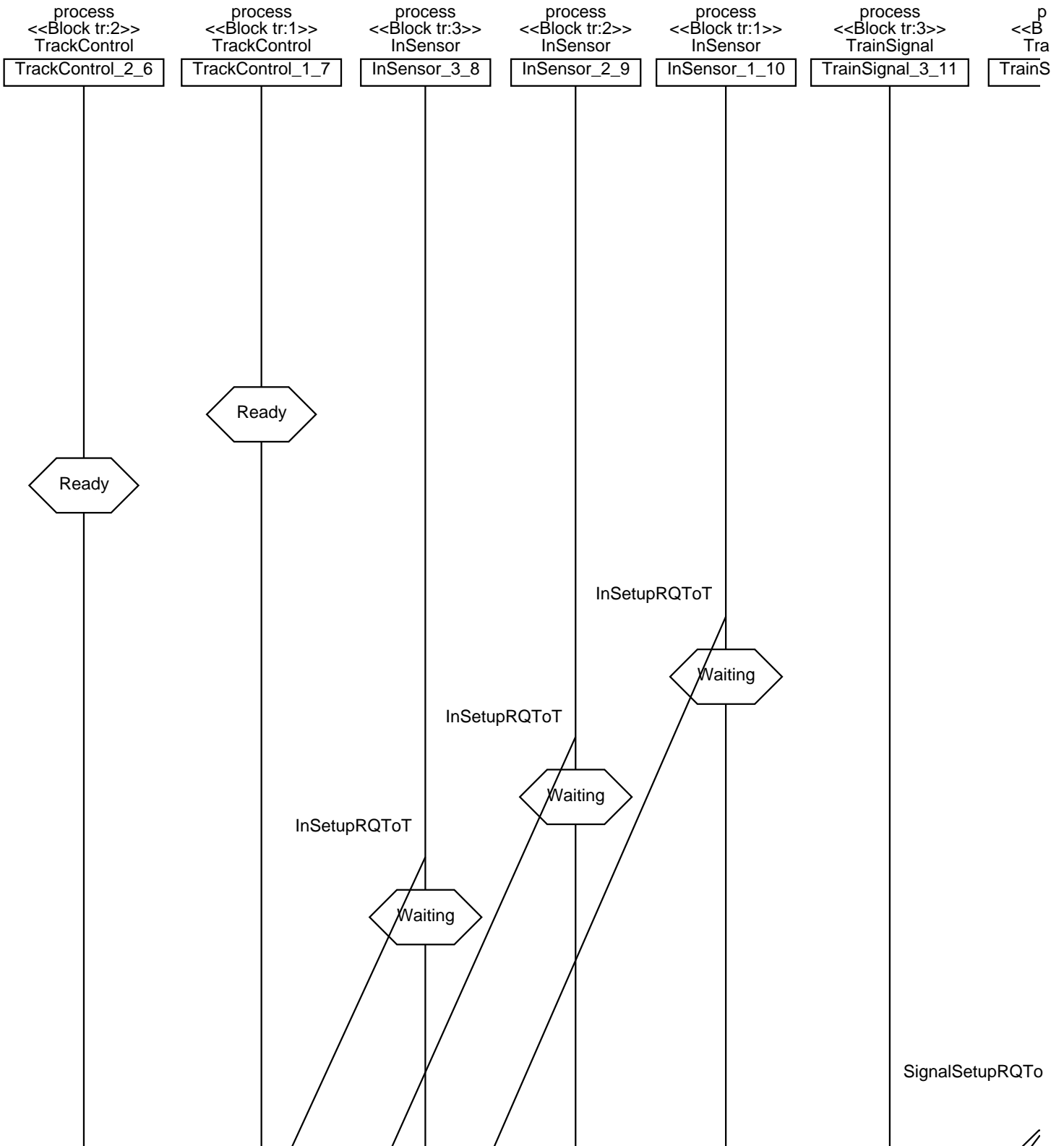


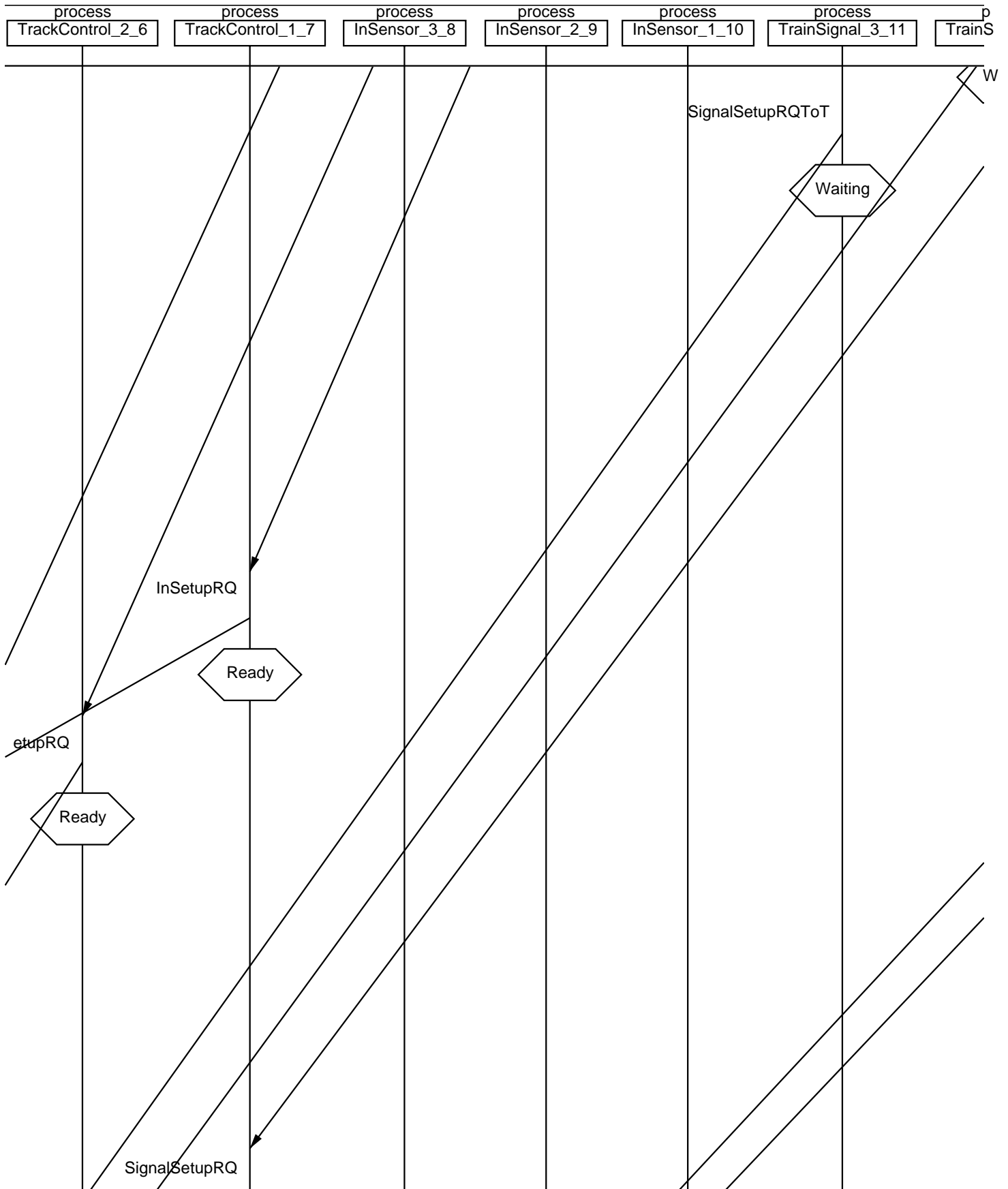


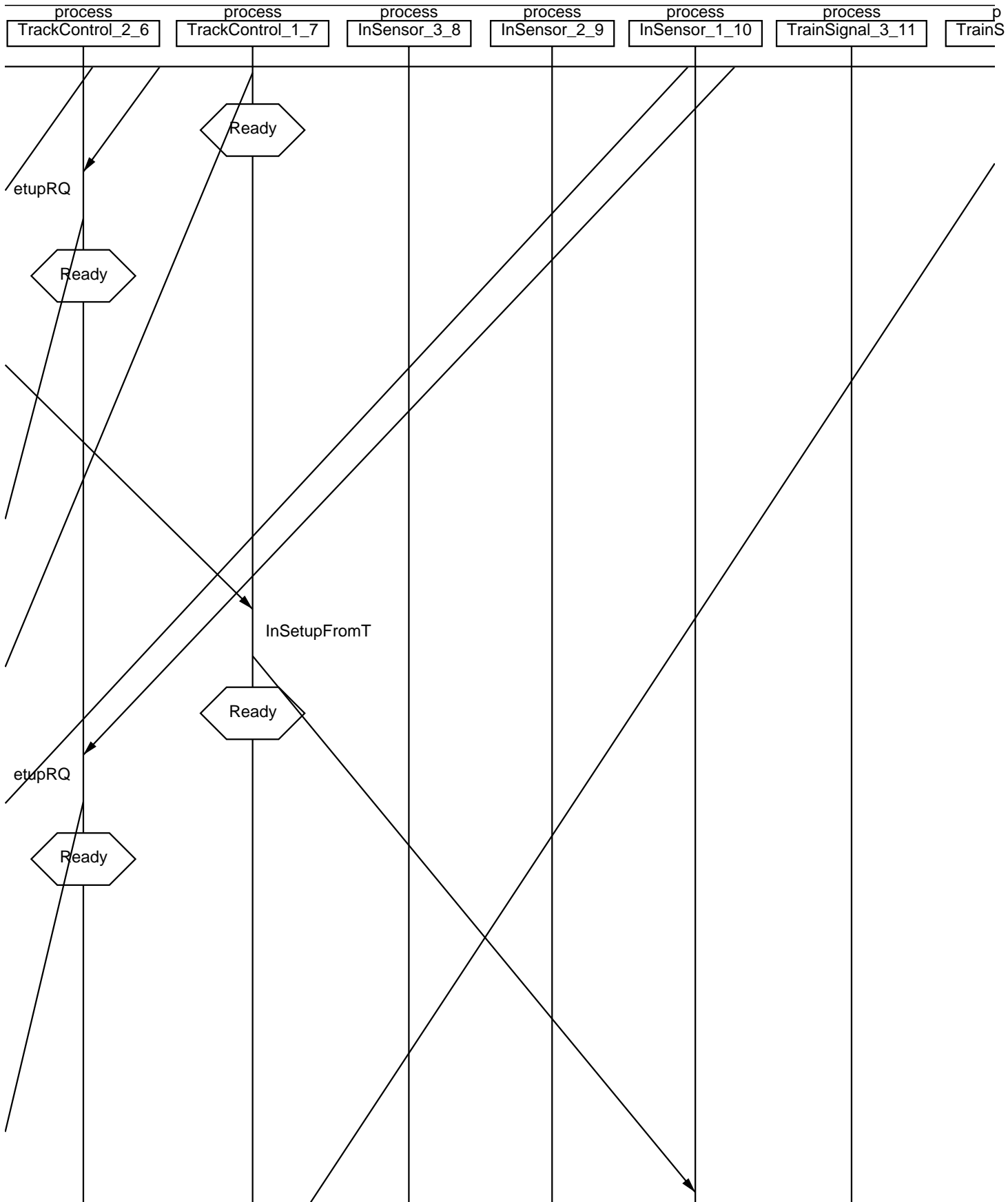


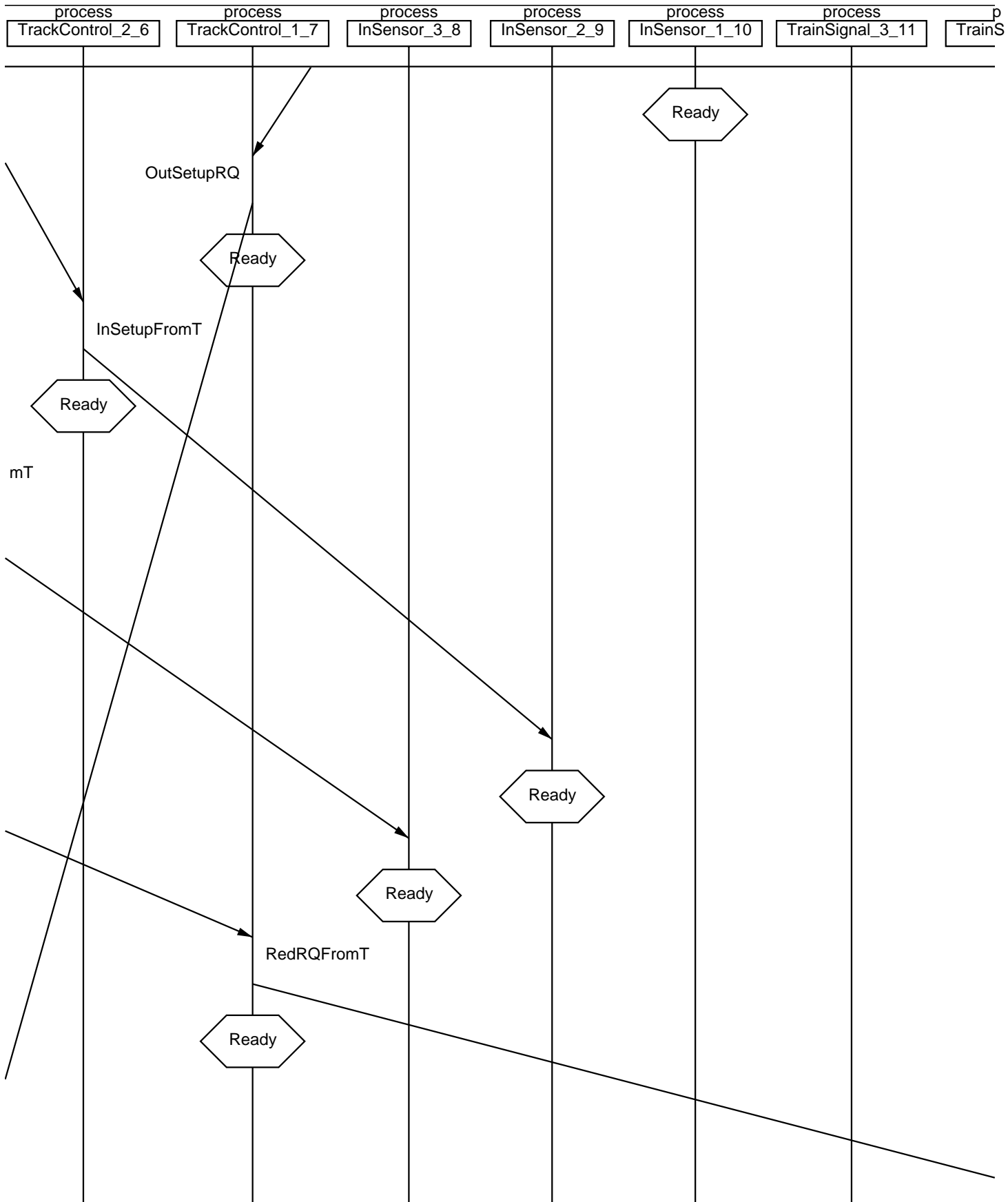




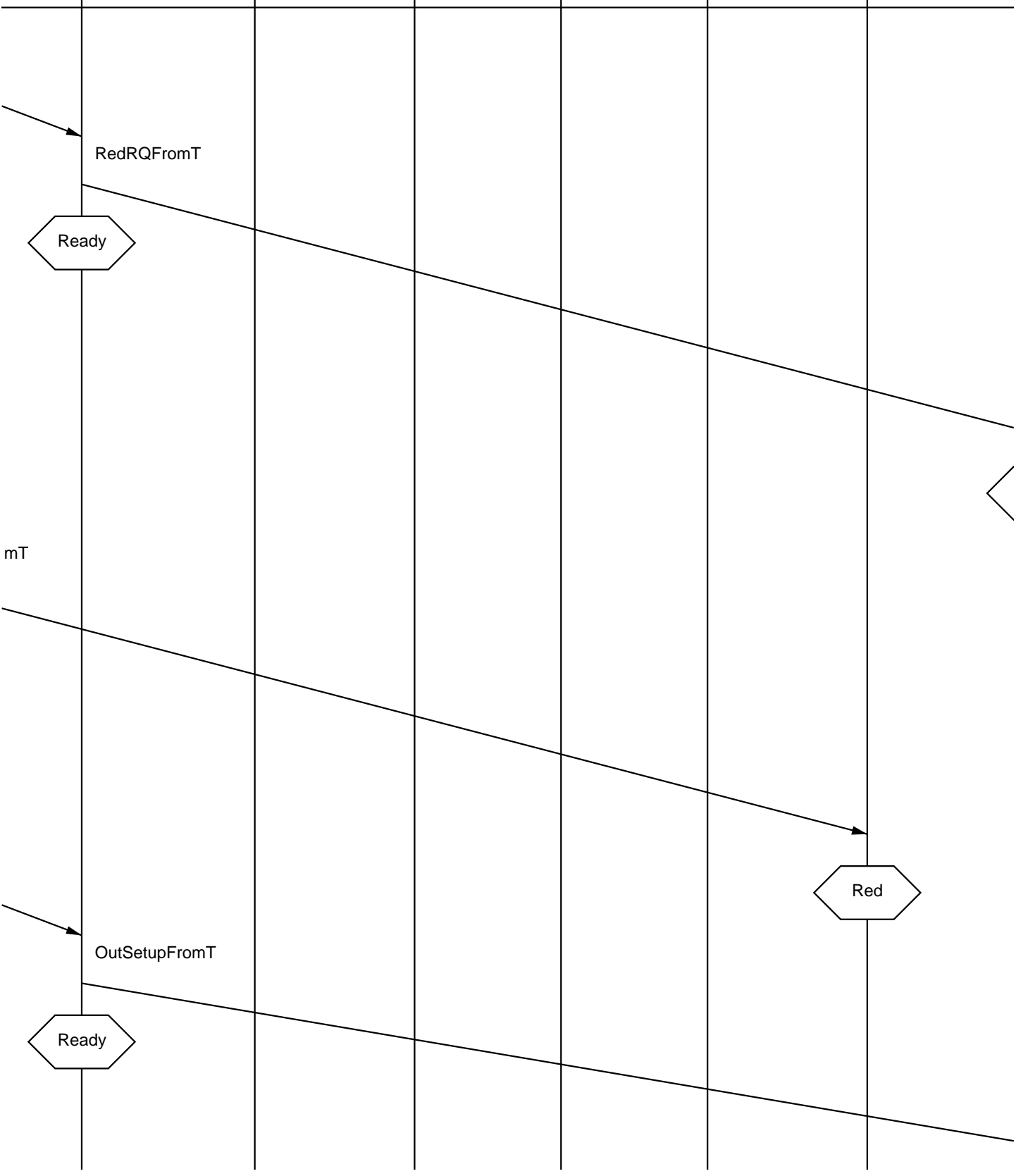


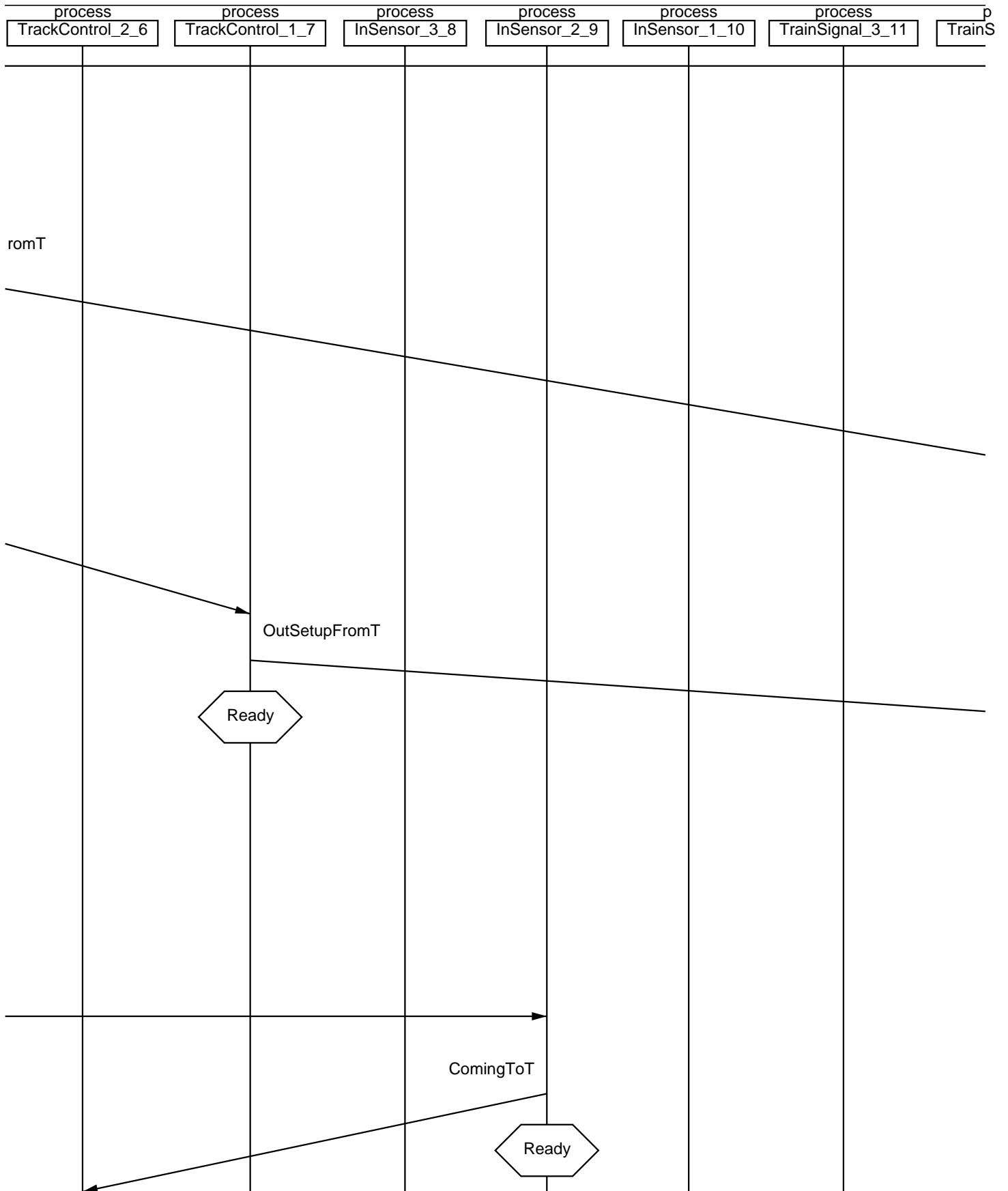


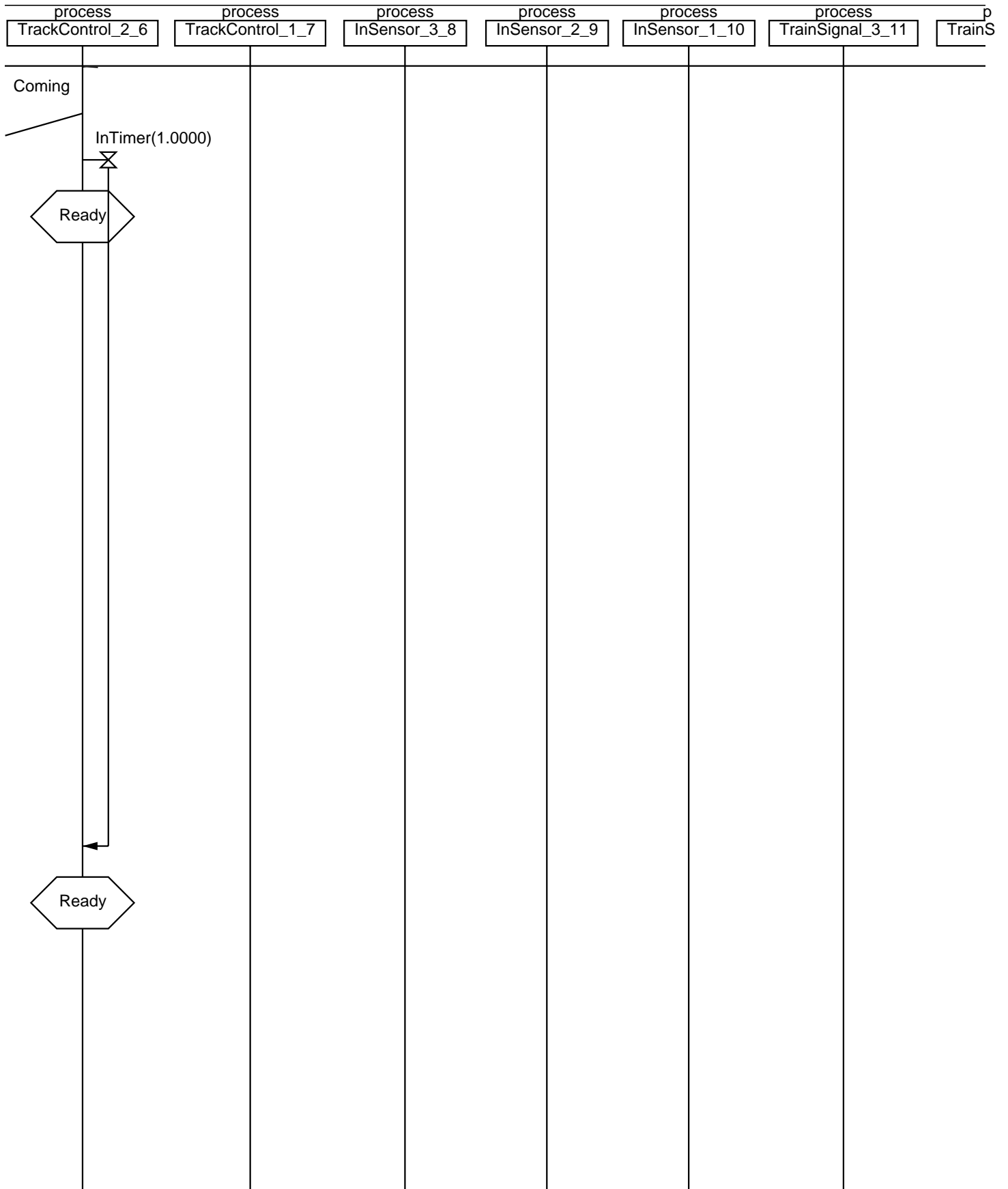


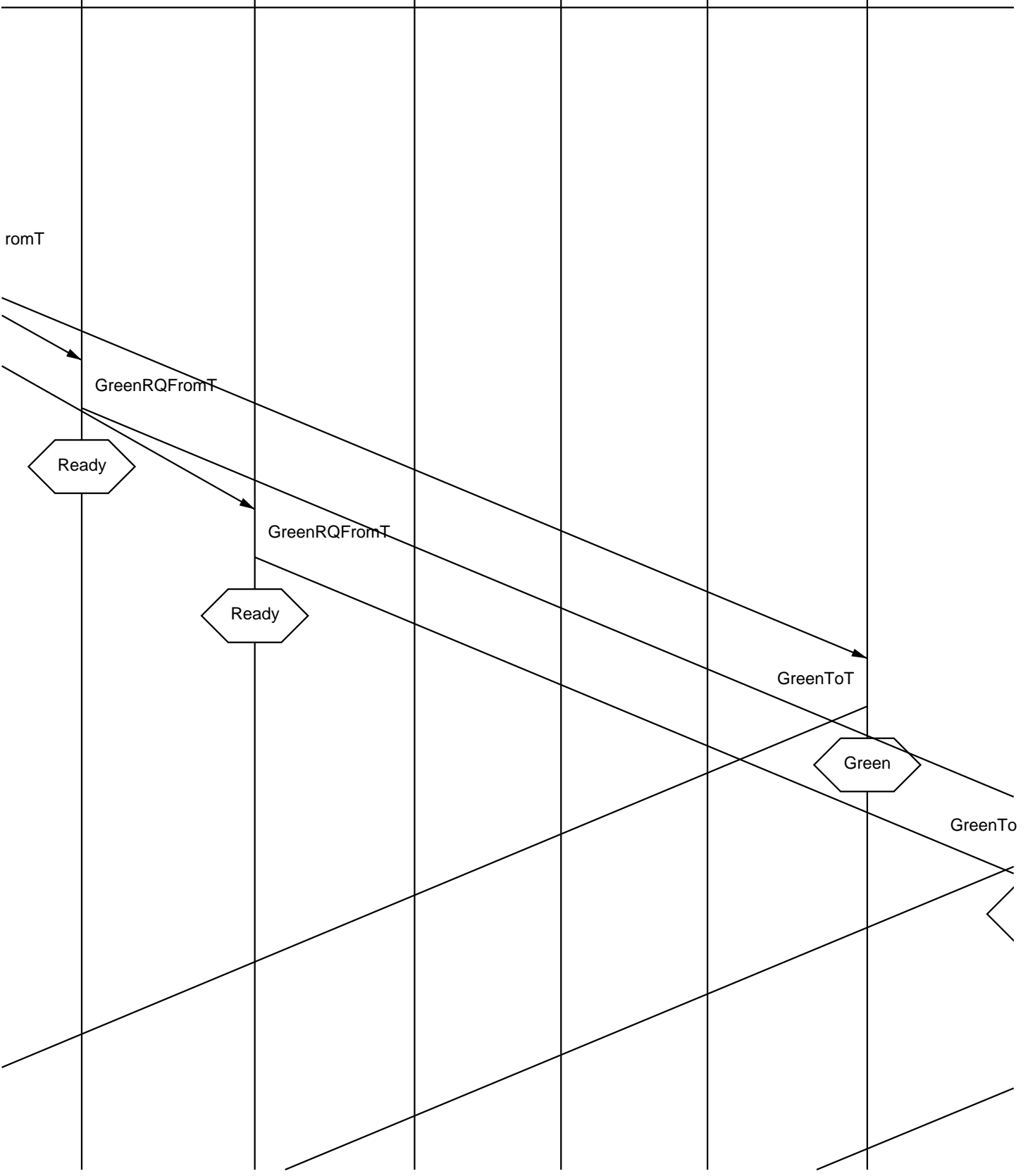
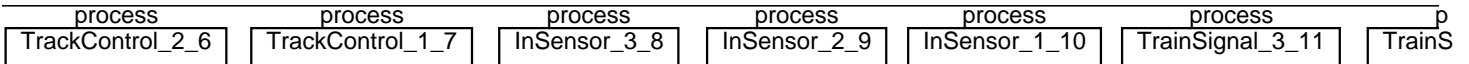


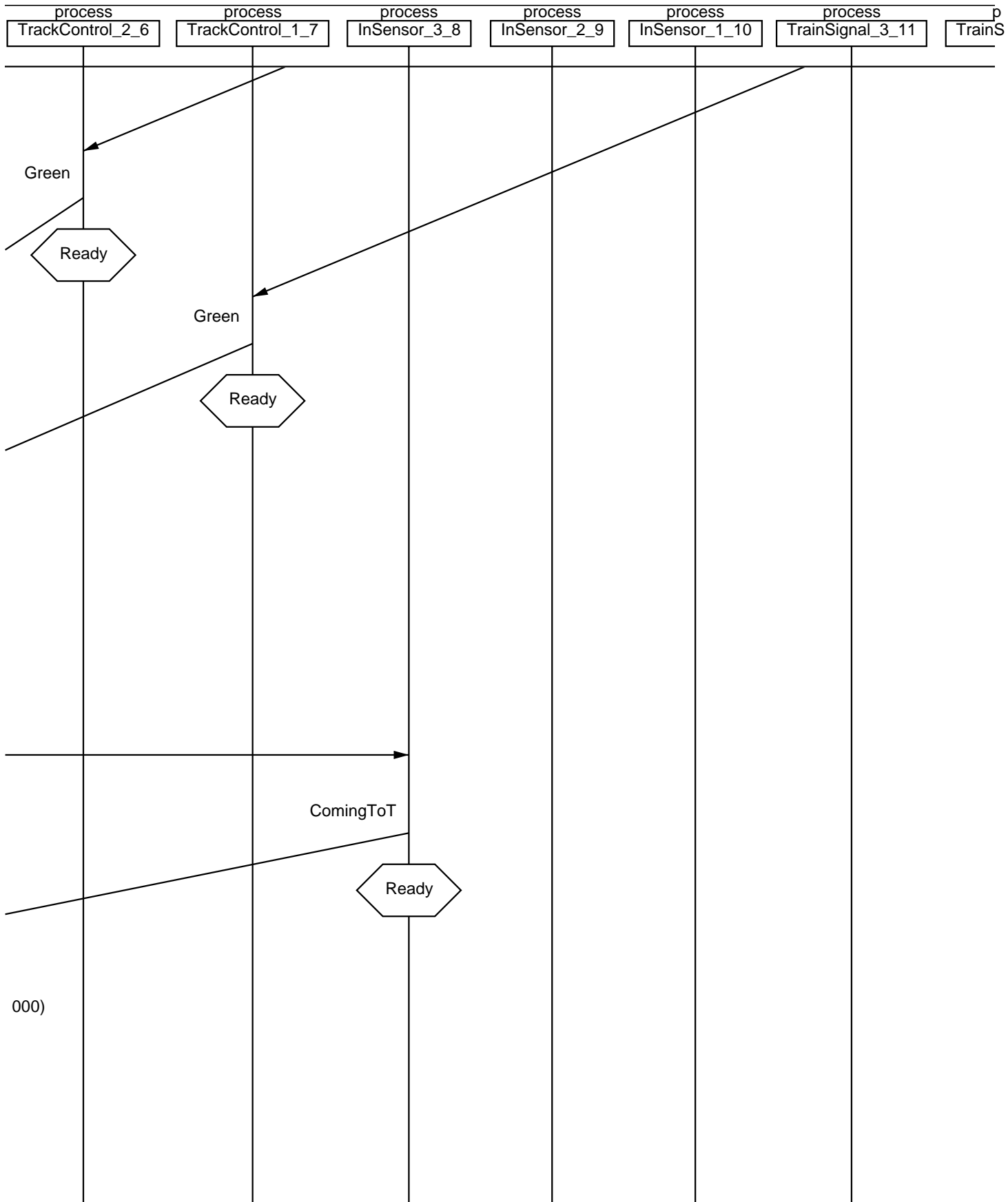
process TrackControl_2_6 process TrackControl_1_7 process InSensor_3_8 process InSensor_2_9 process InSensor_1_10 process TrainSignal_3_11 process TrainS

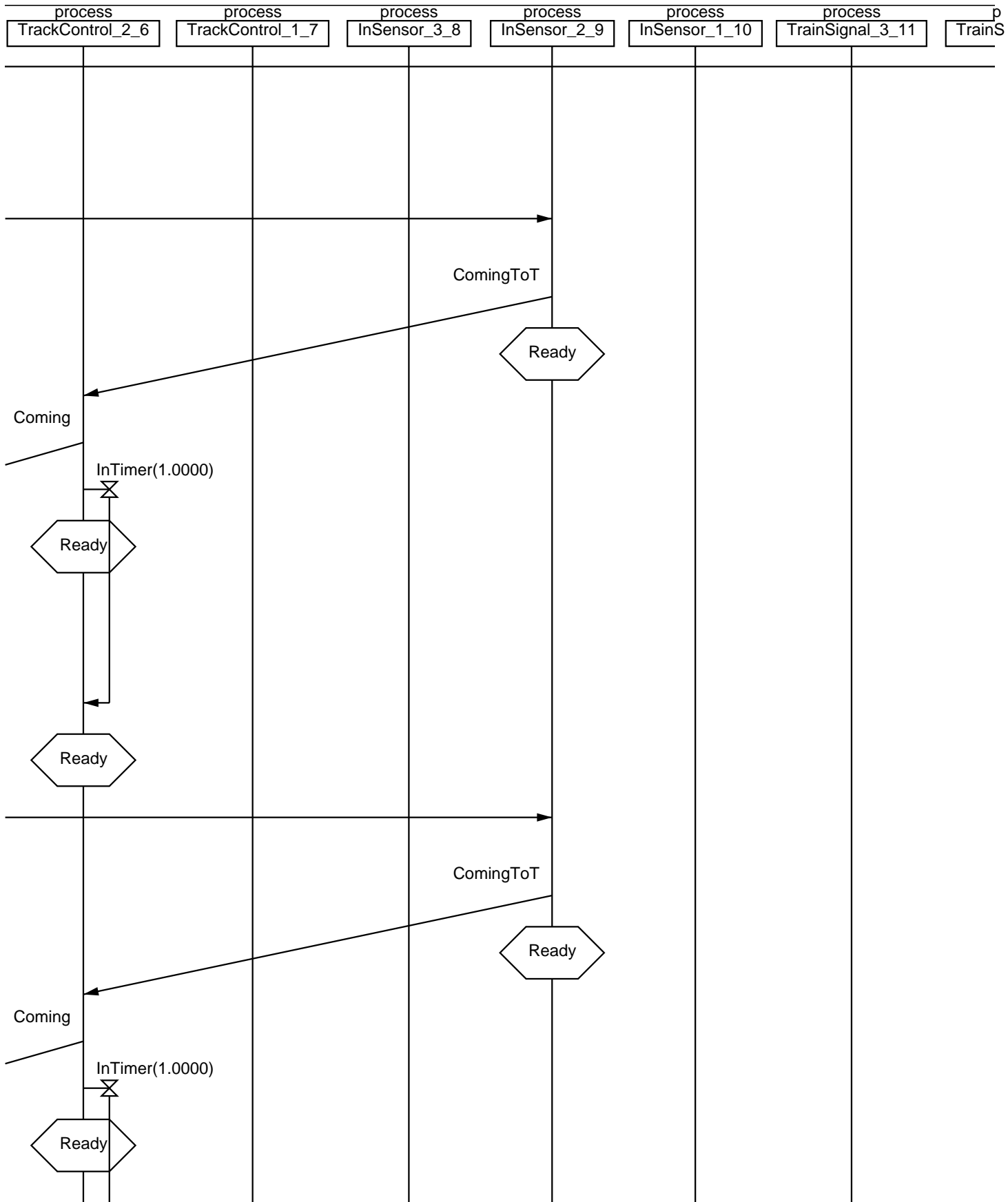


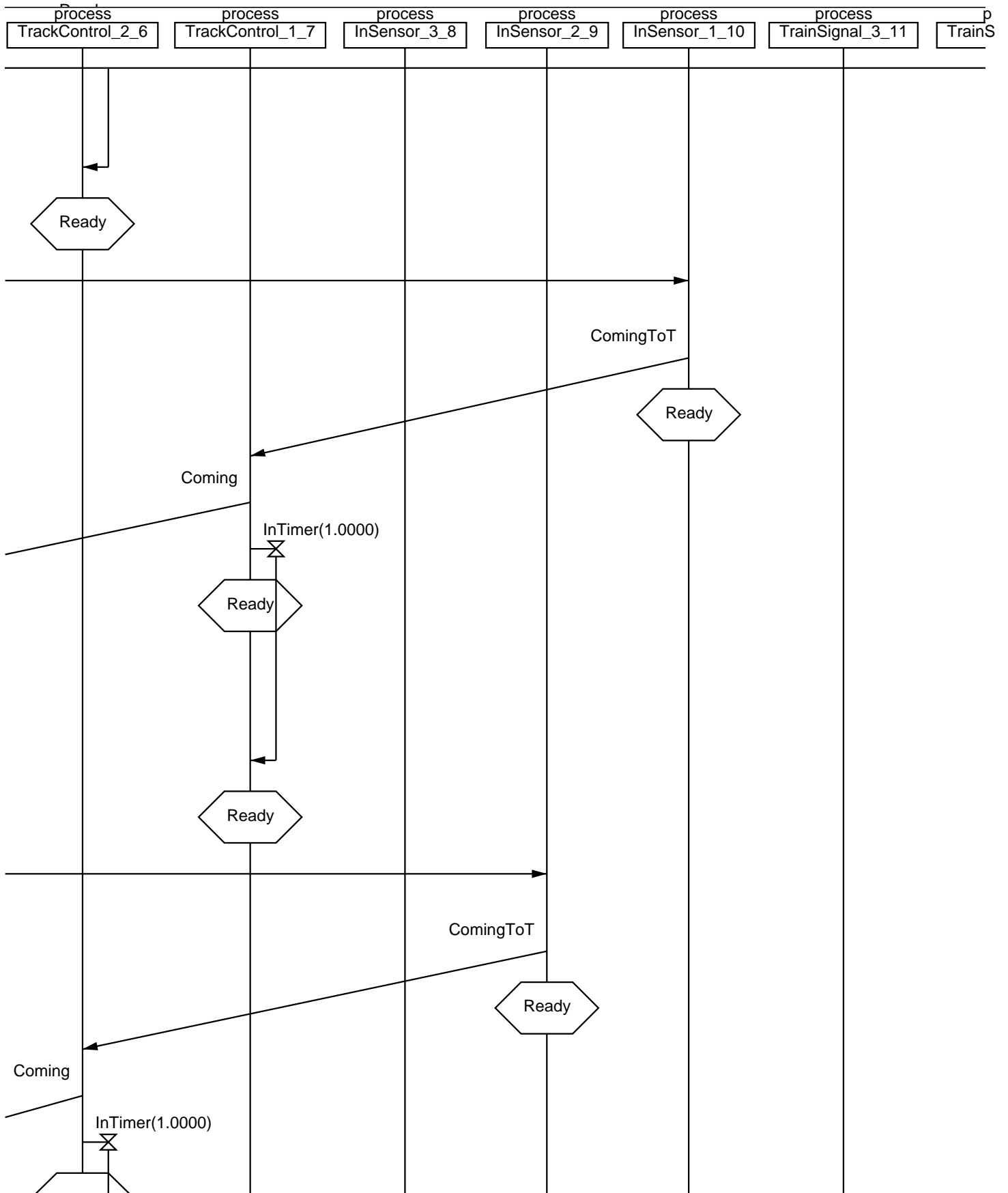


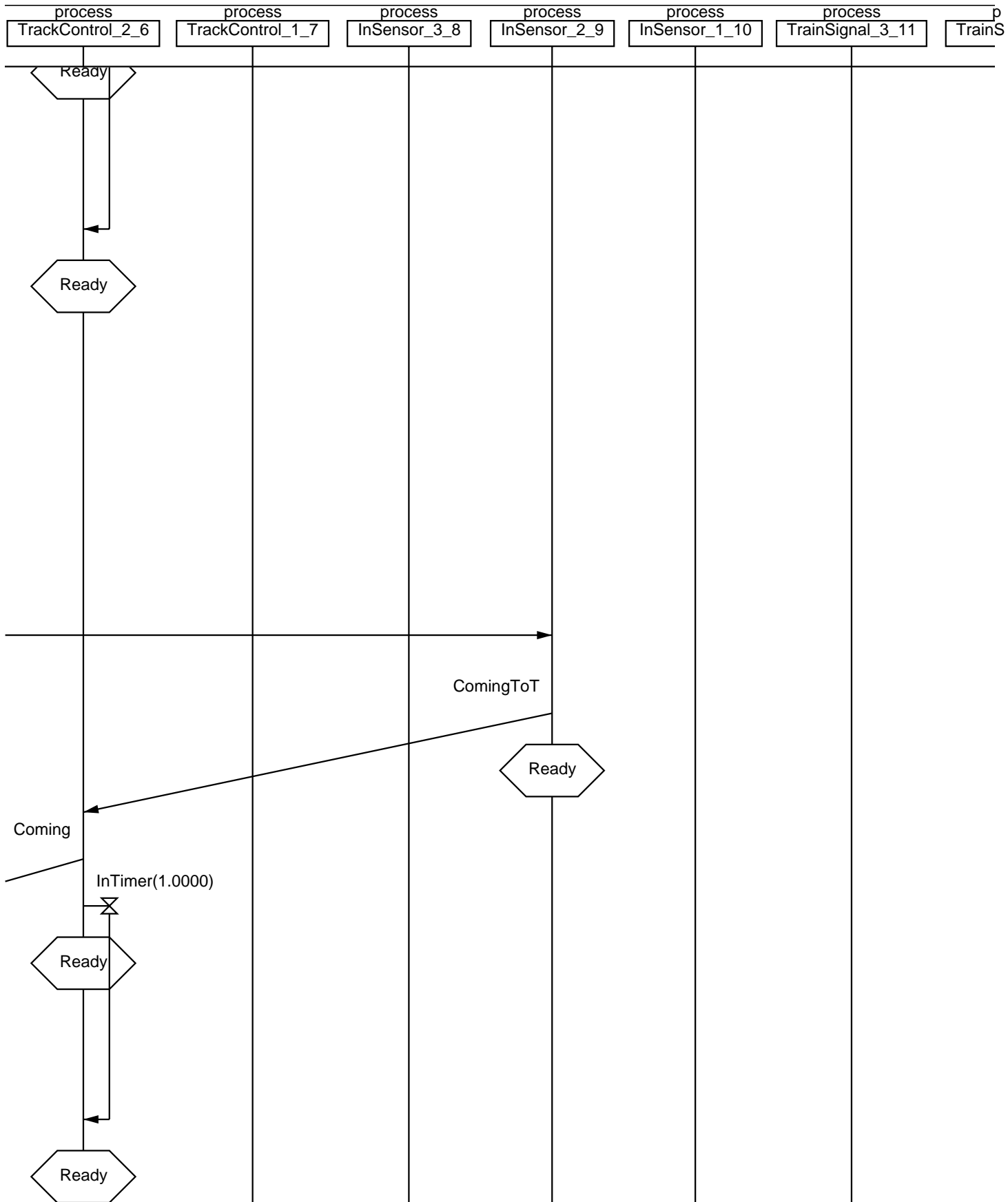


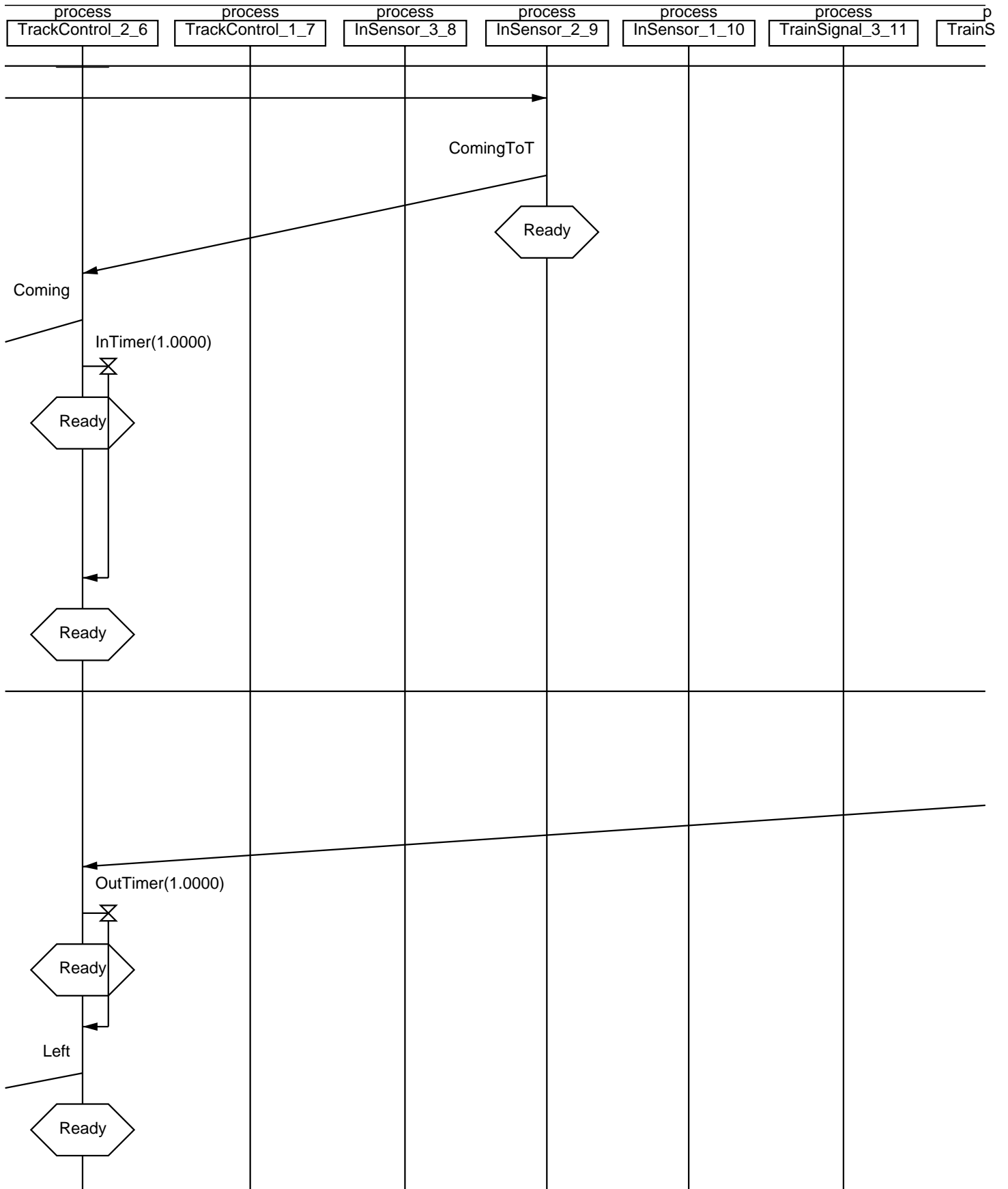


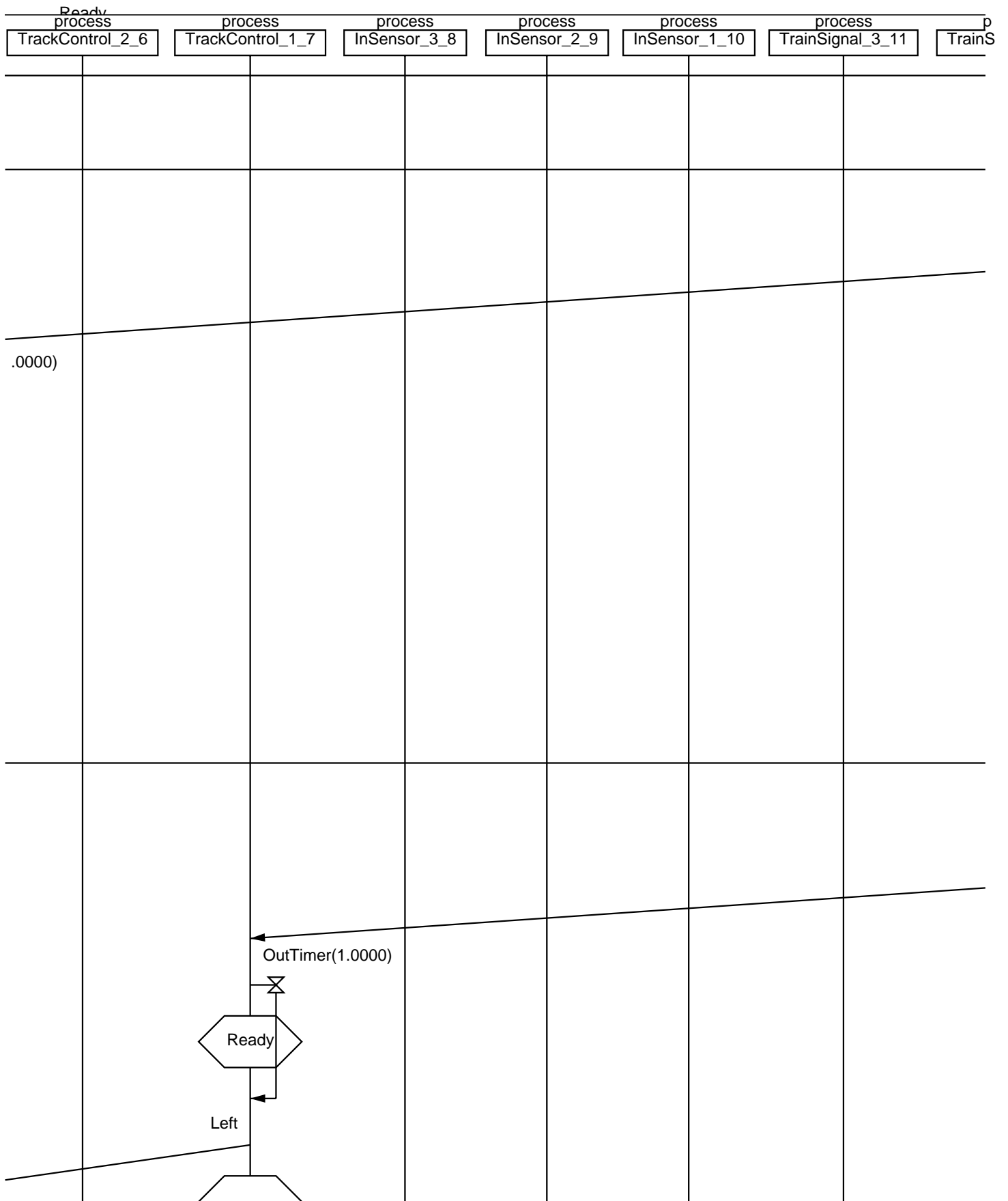


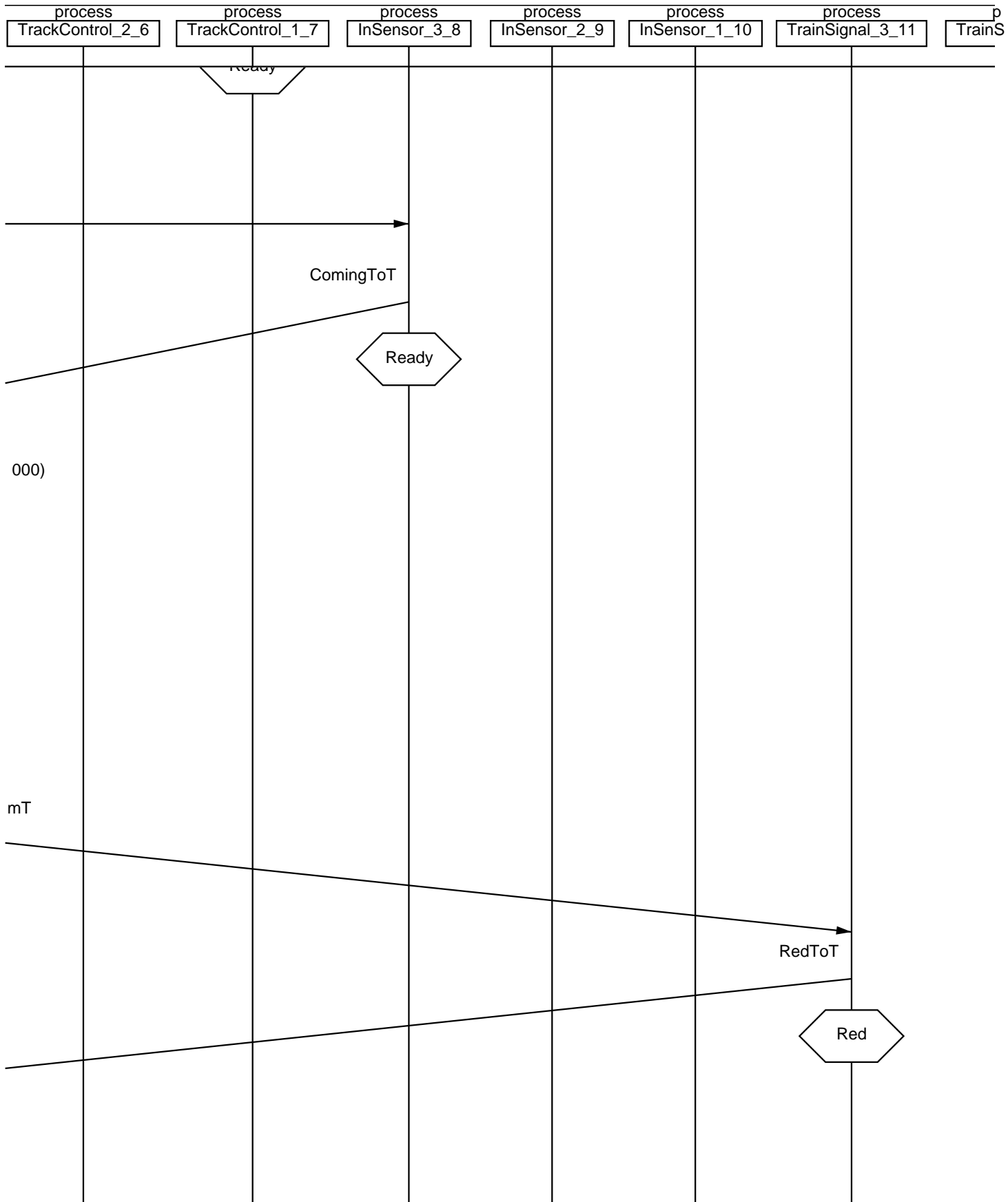




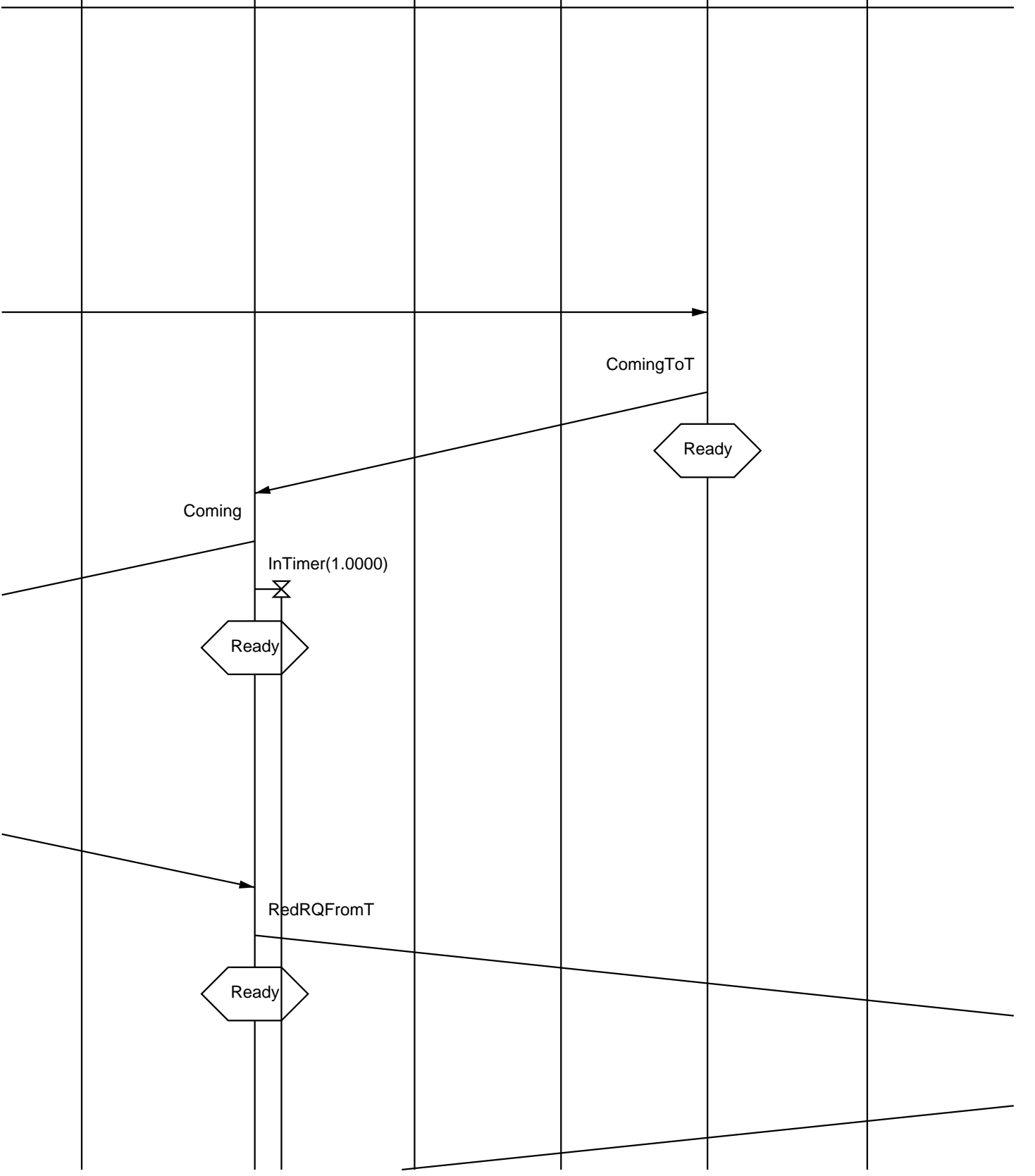


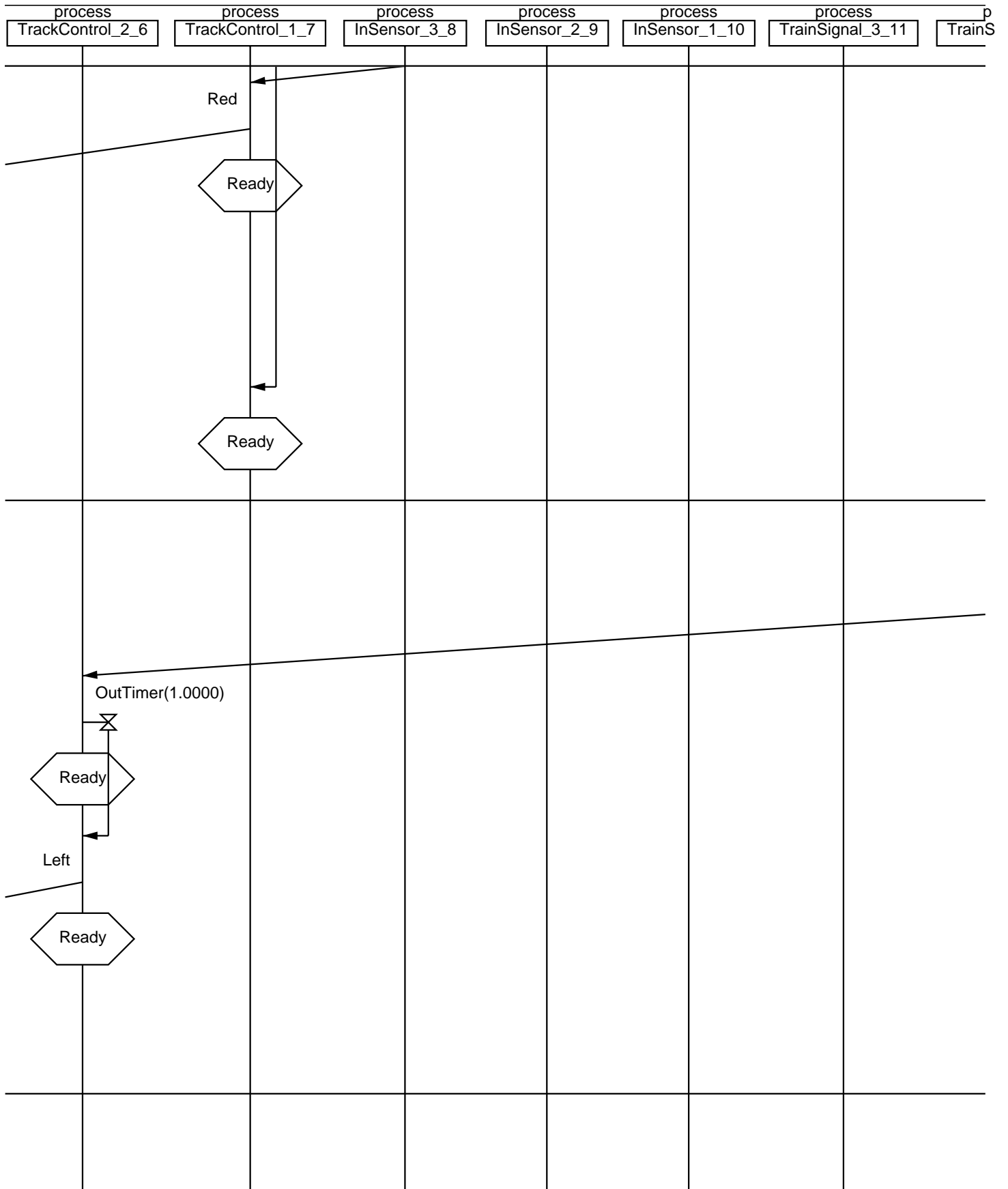


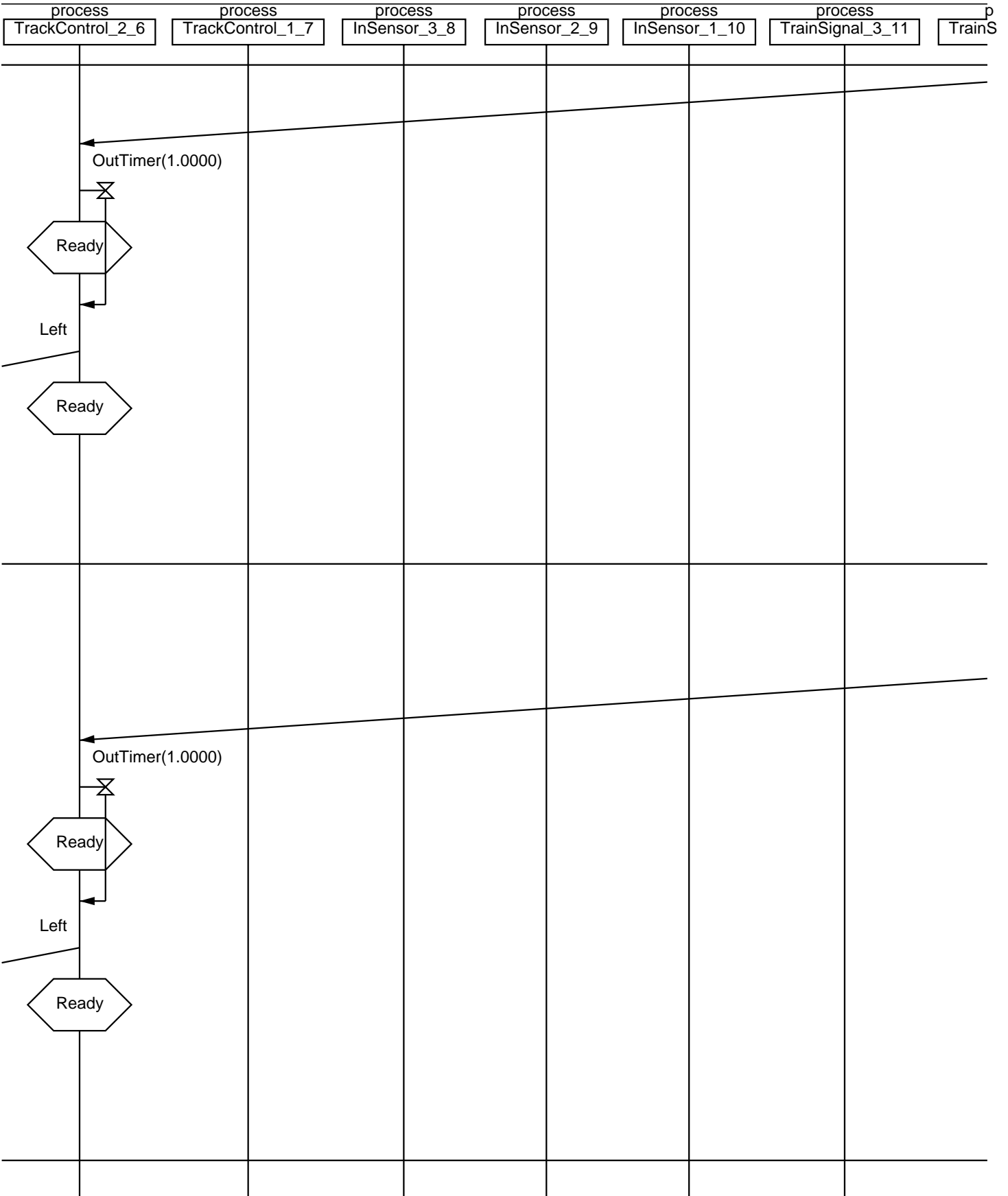


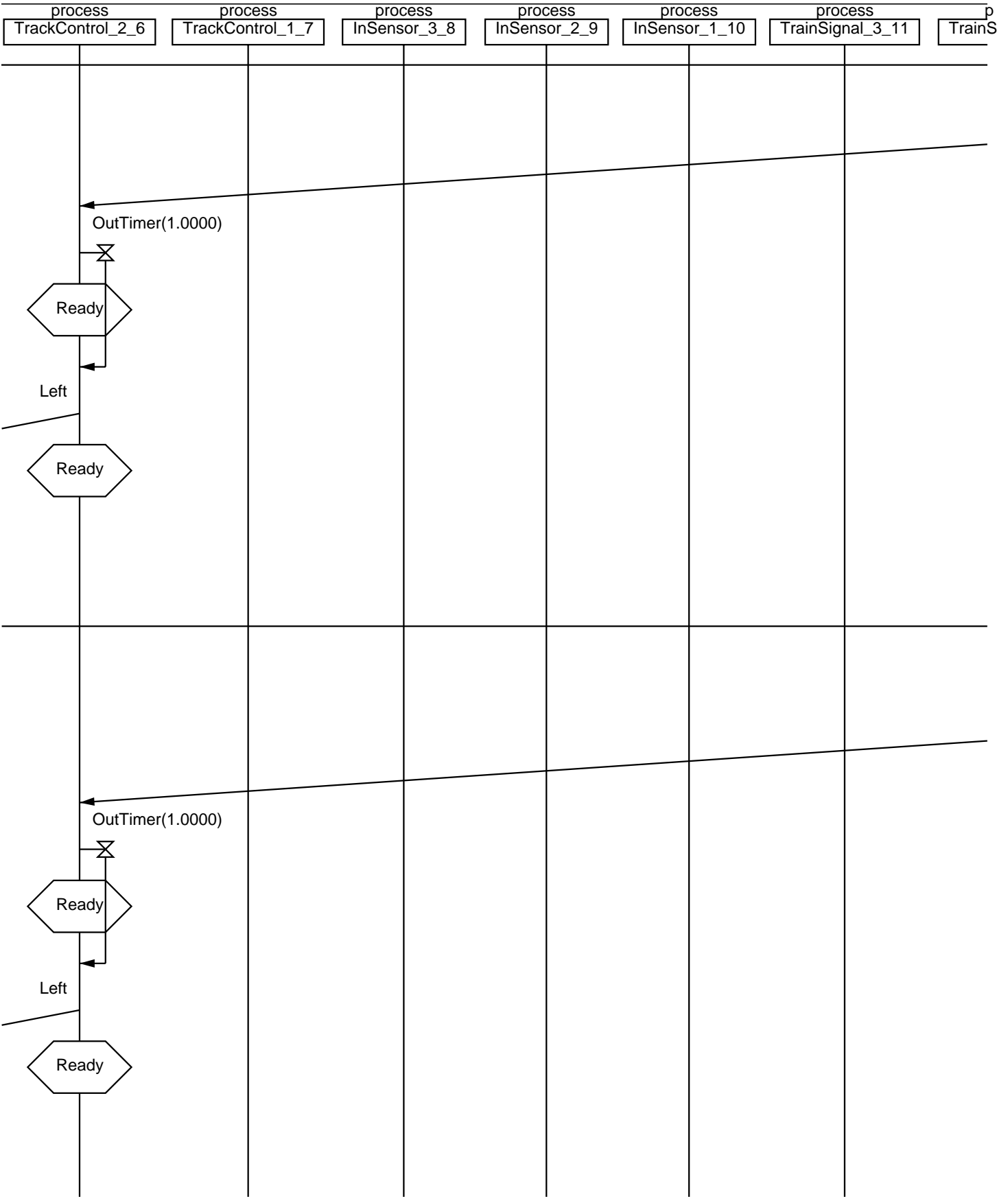


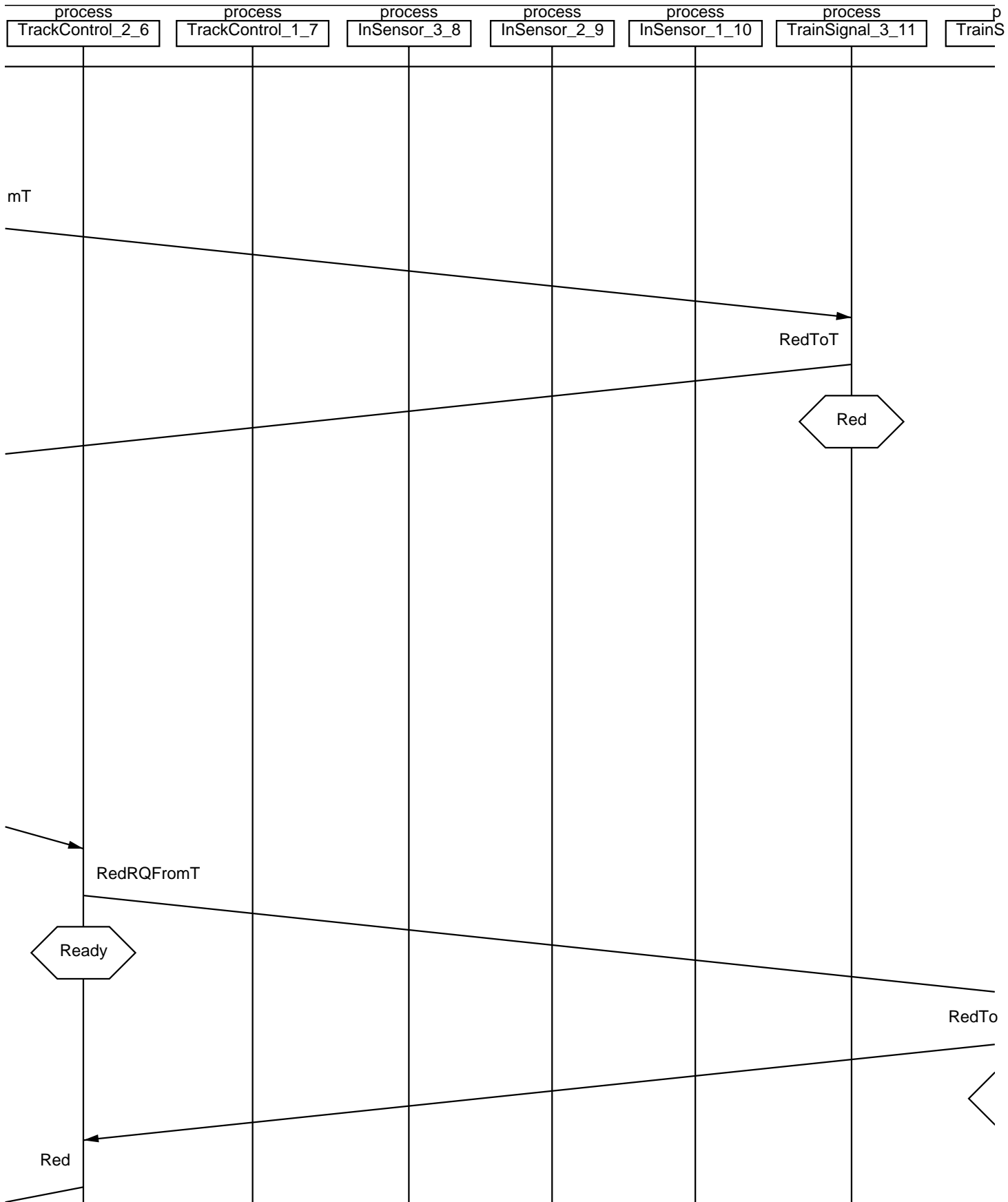
process TrackControl_2_6 process TrackControl_1_7 process InSensor_3_8 process InSensor_2_9 process InSensor_1_10 process TrainSignal_3_11 process TrainS

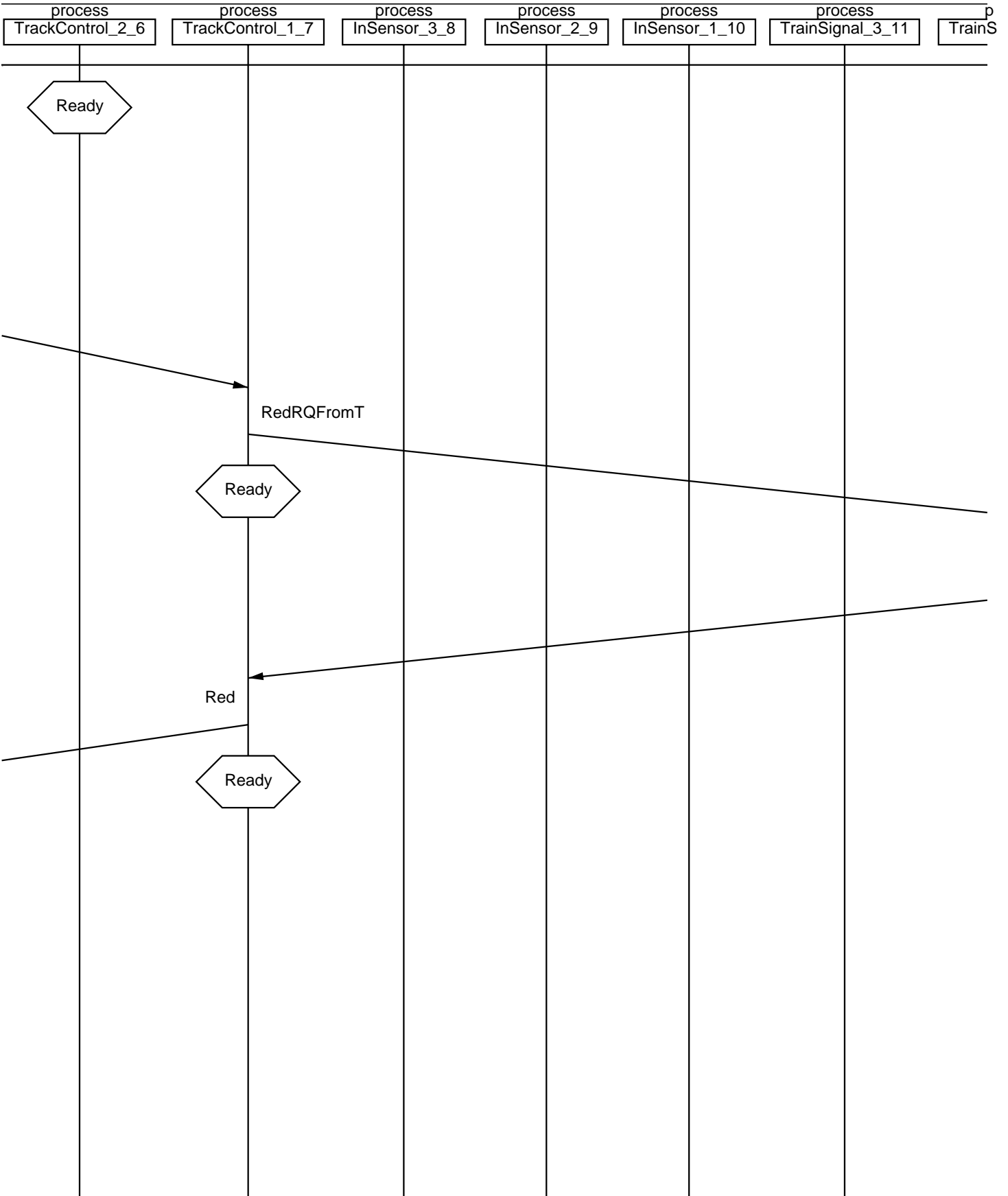




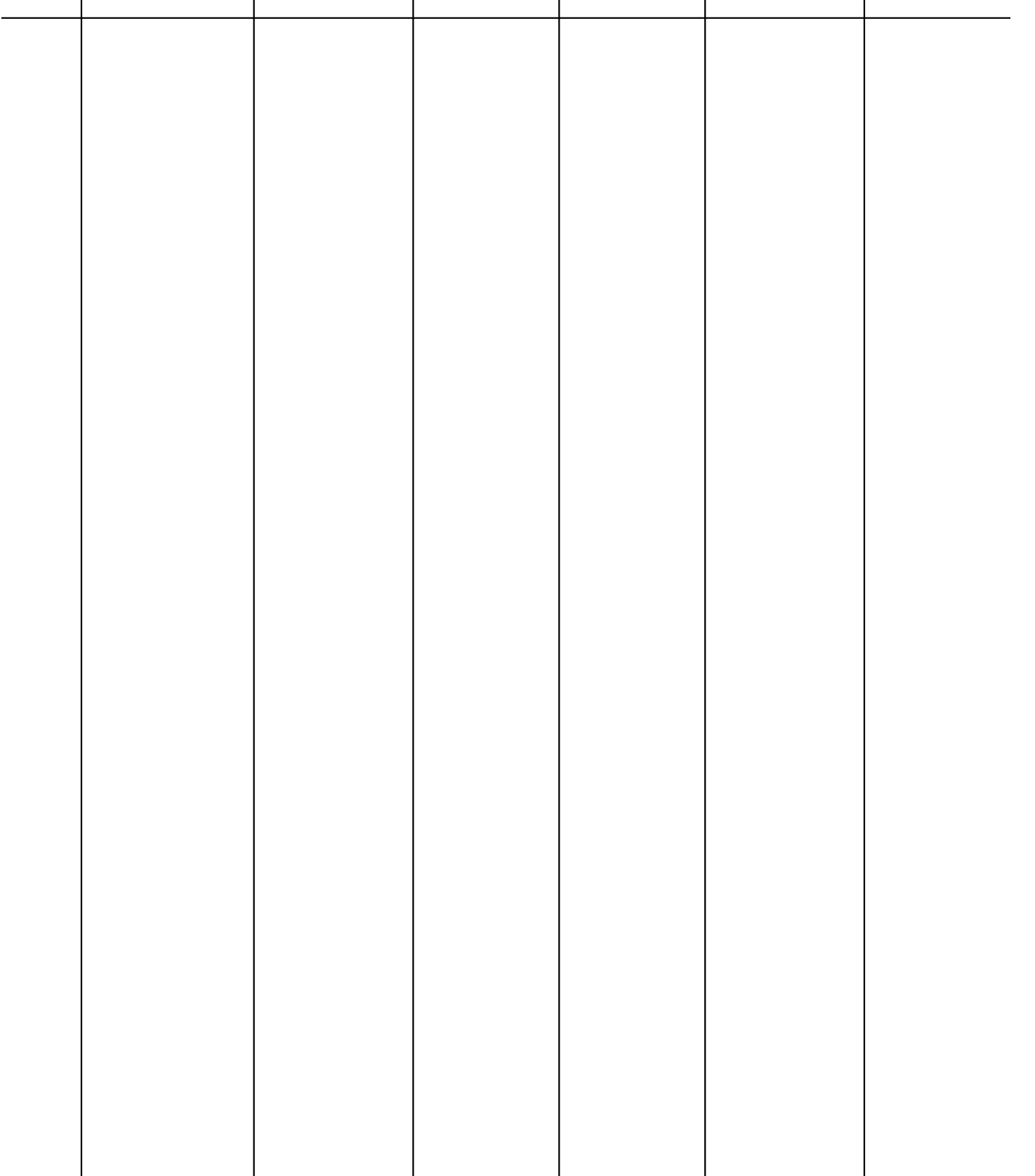


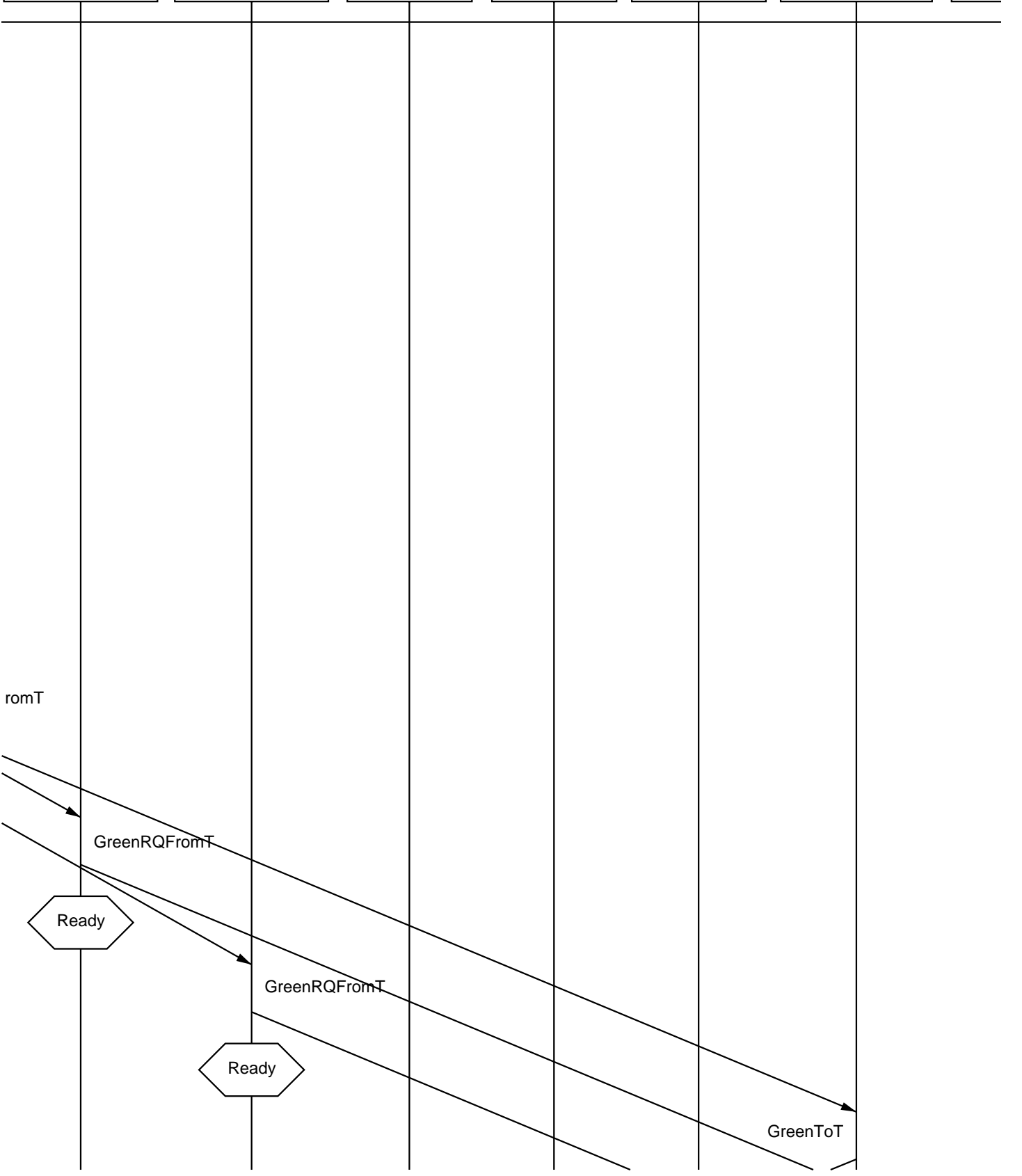
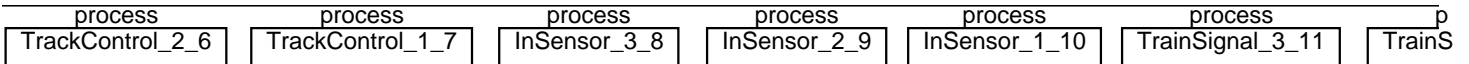






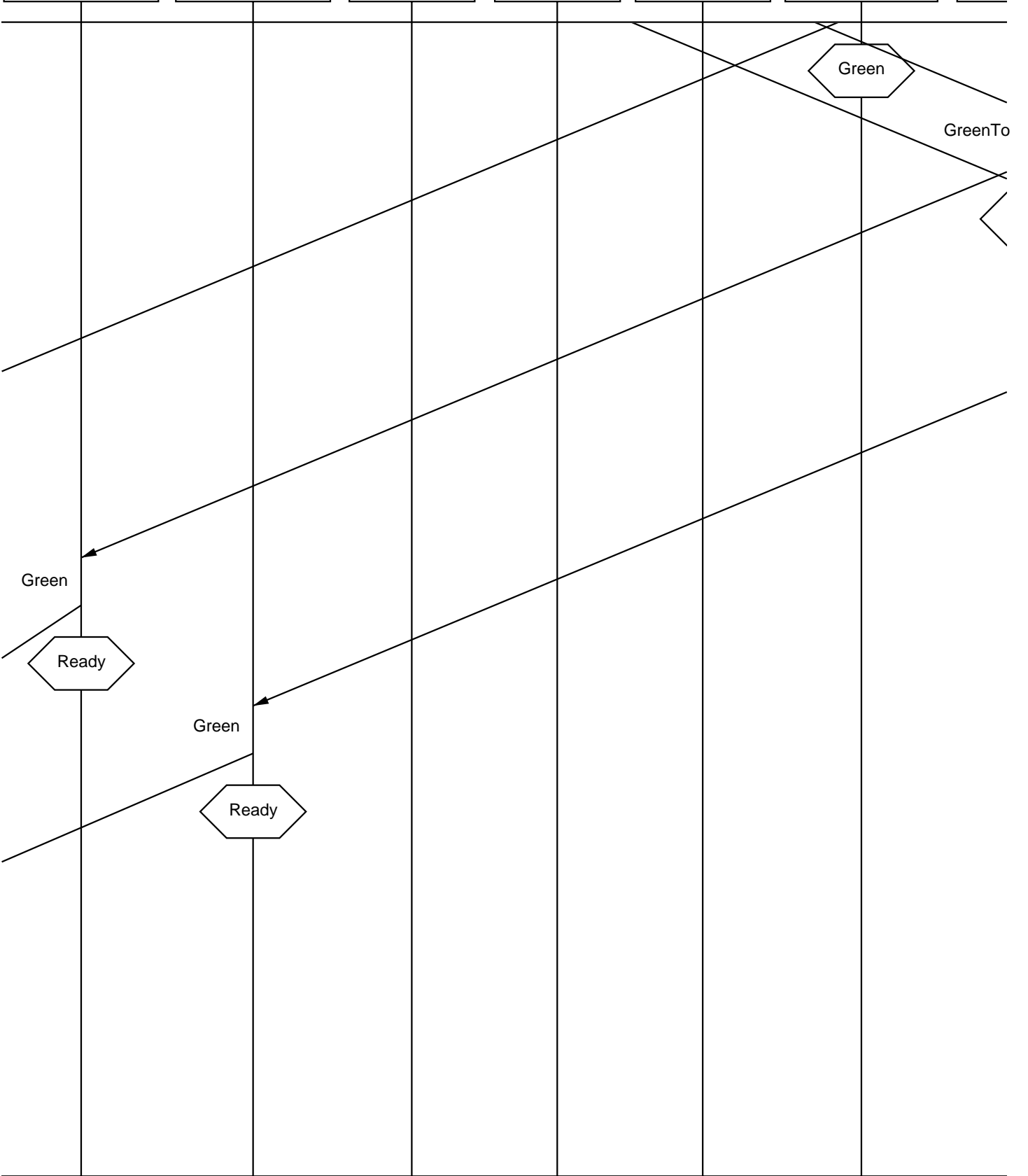
process	process	process	process	process	process	p
TrackControl_2_6	TrackControl_1_7	InSensor_3_8	InSensor_2_9	InSensor_1_10	TrainSignal_3_11	TrainS

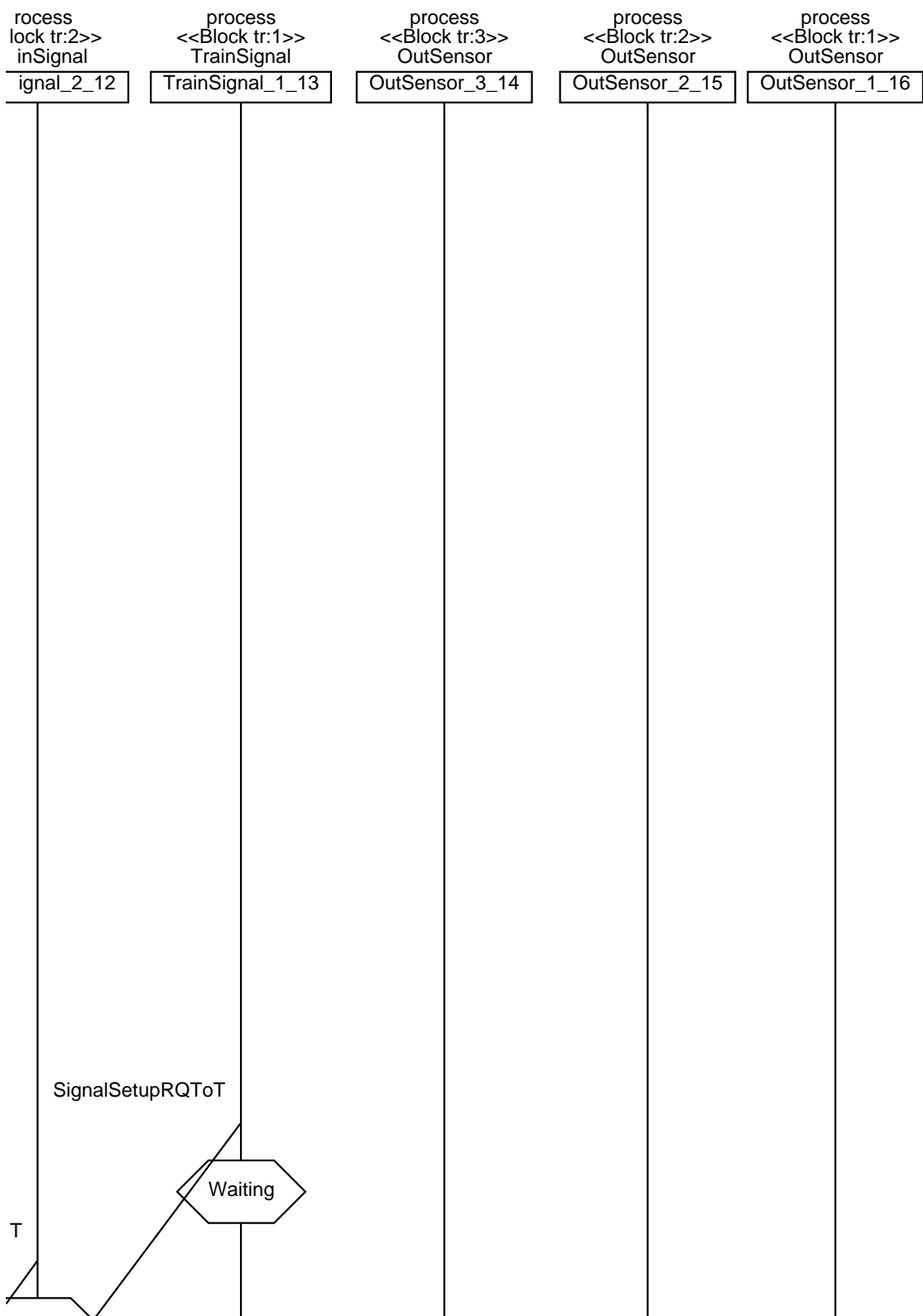


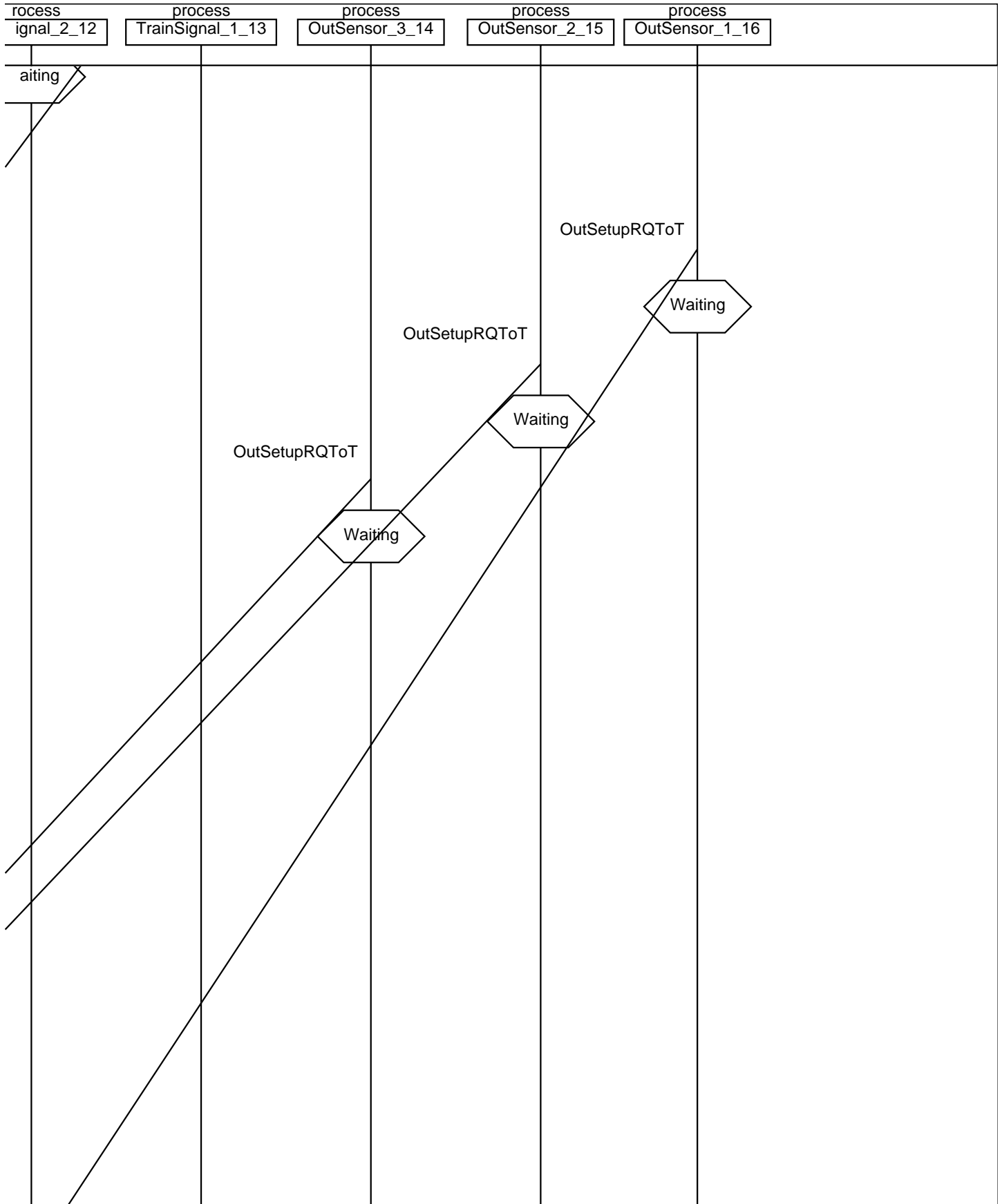


process process process process process process p

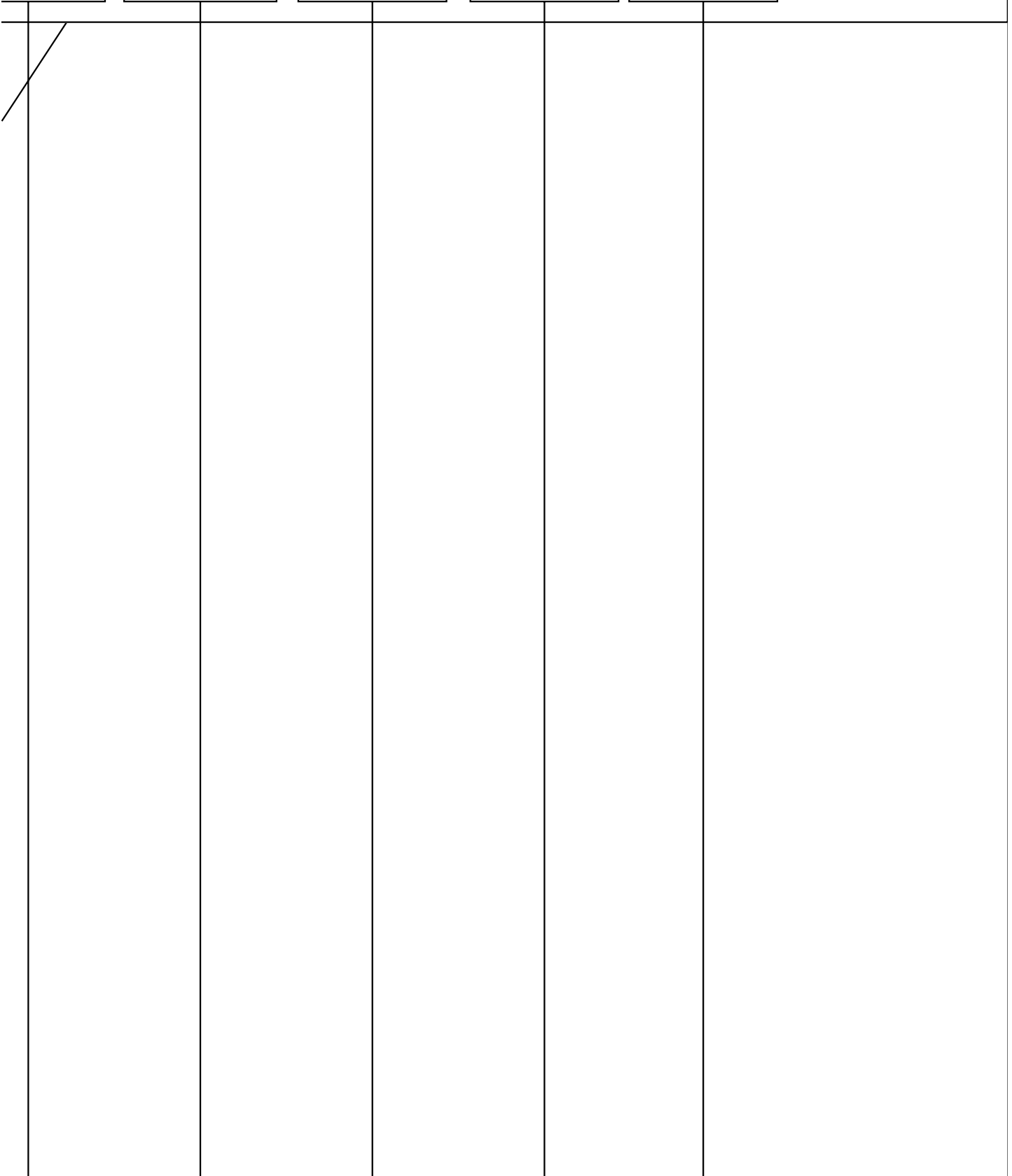
TrackControl_2_6 TrackControl_1_7 InSensor_3_8 InSensor_2_9 InSensor_1_10 TrainSignal_3_11 TrainS



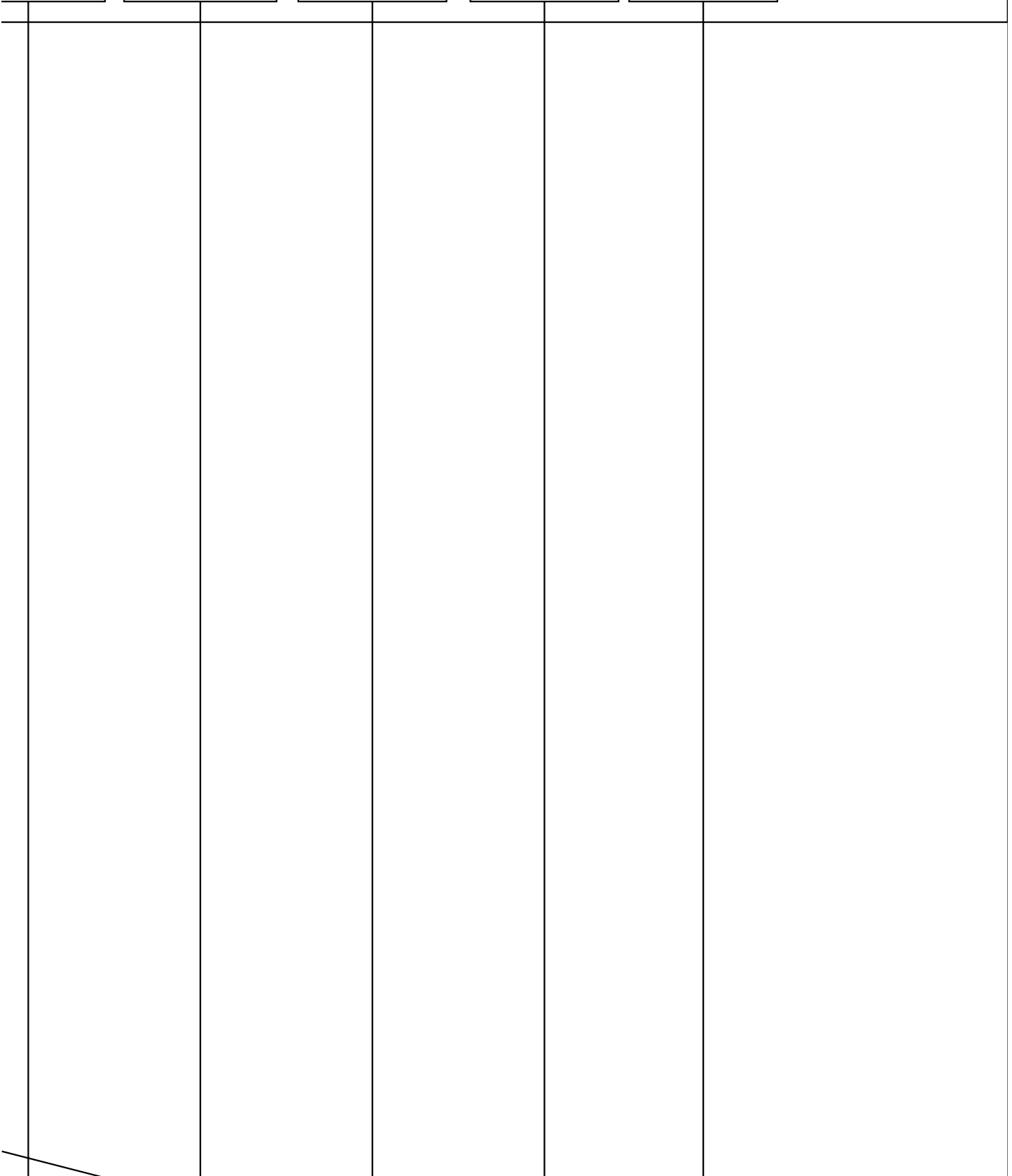


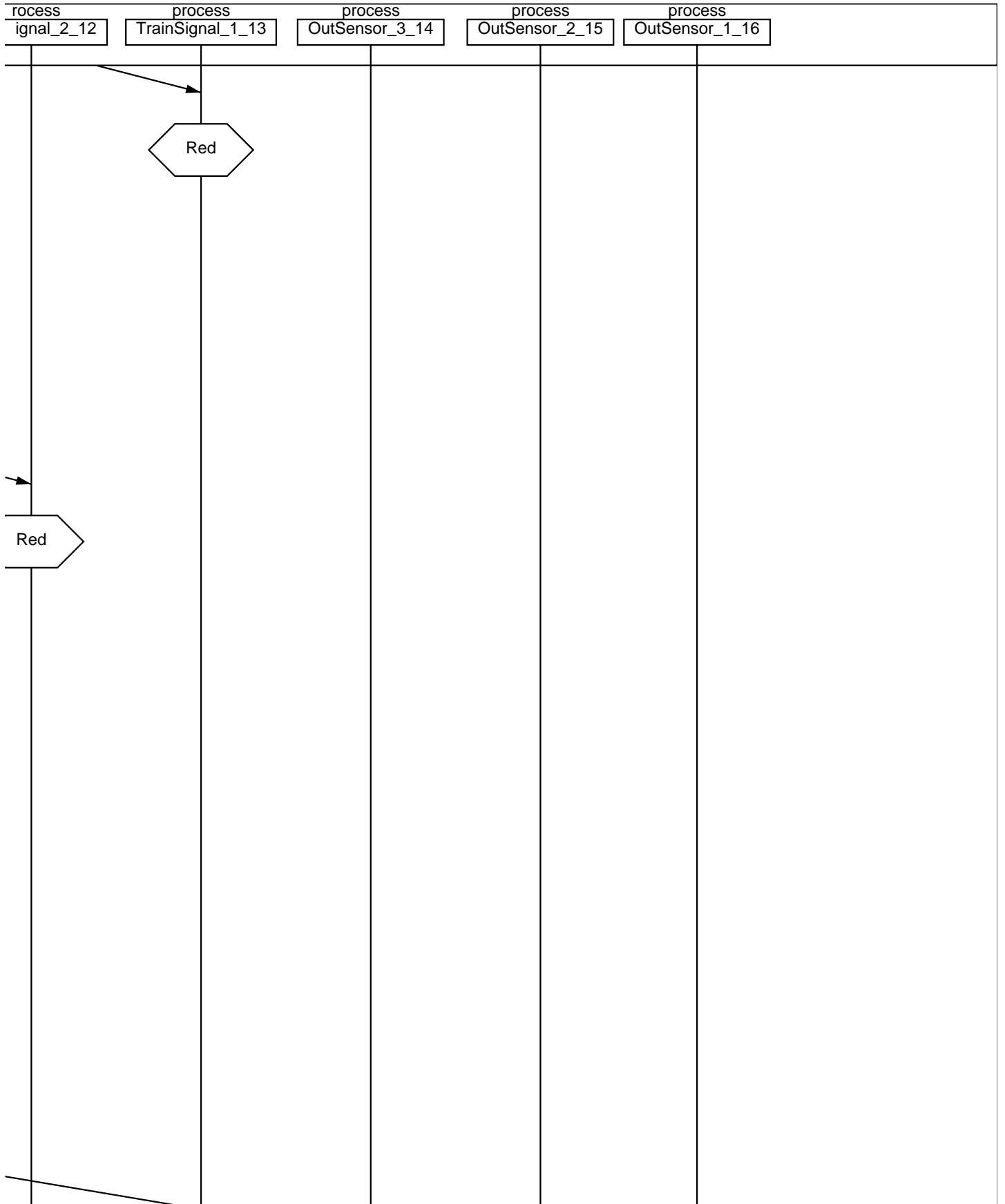


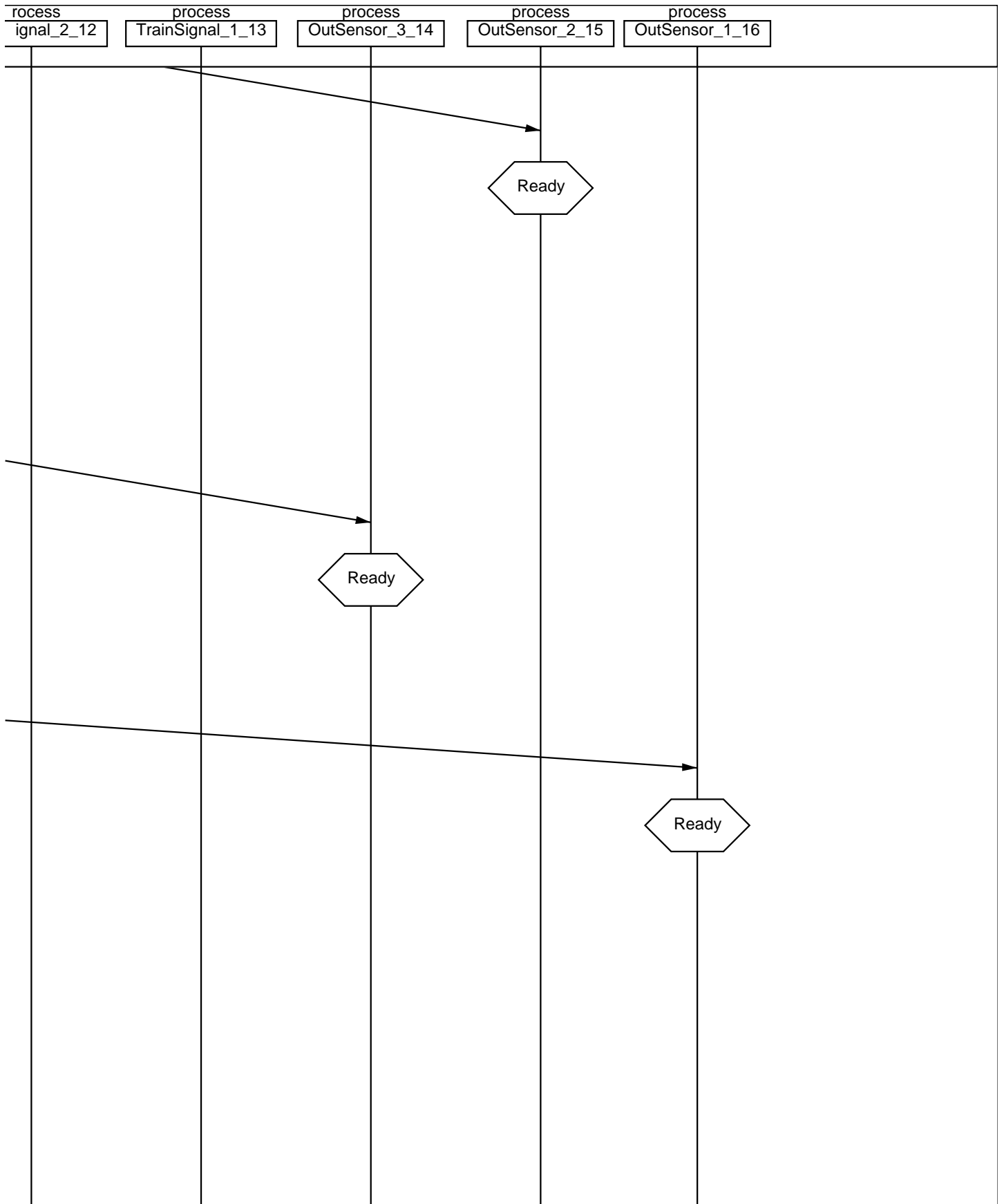
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------



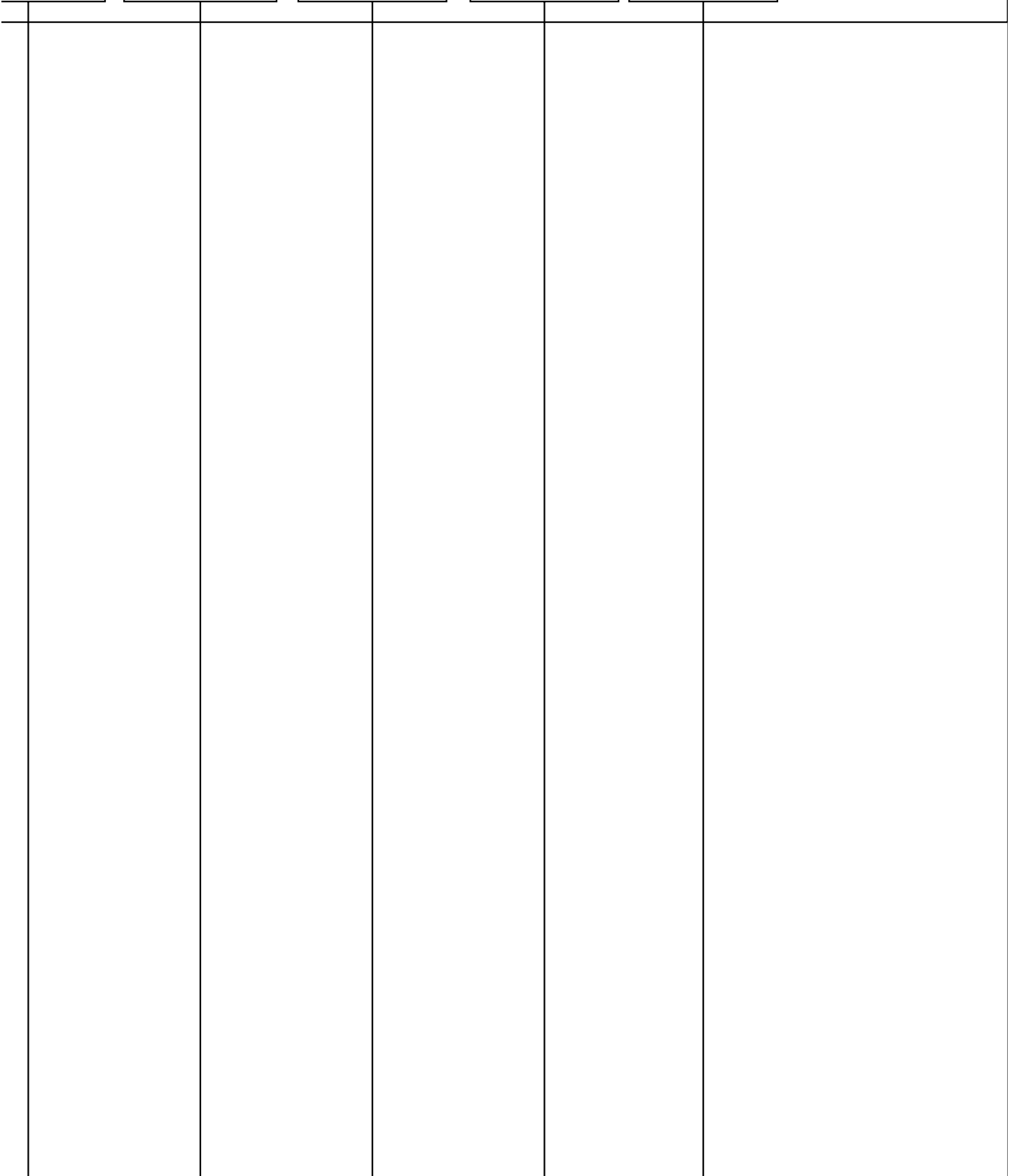
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

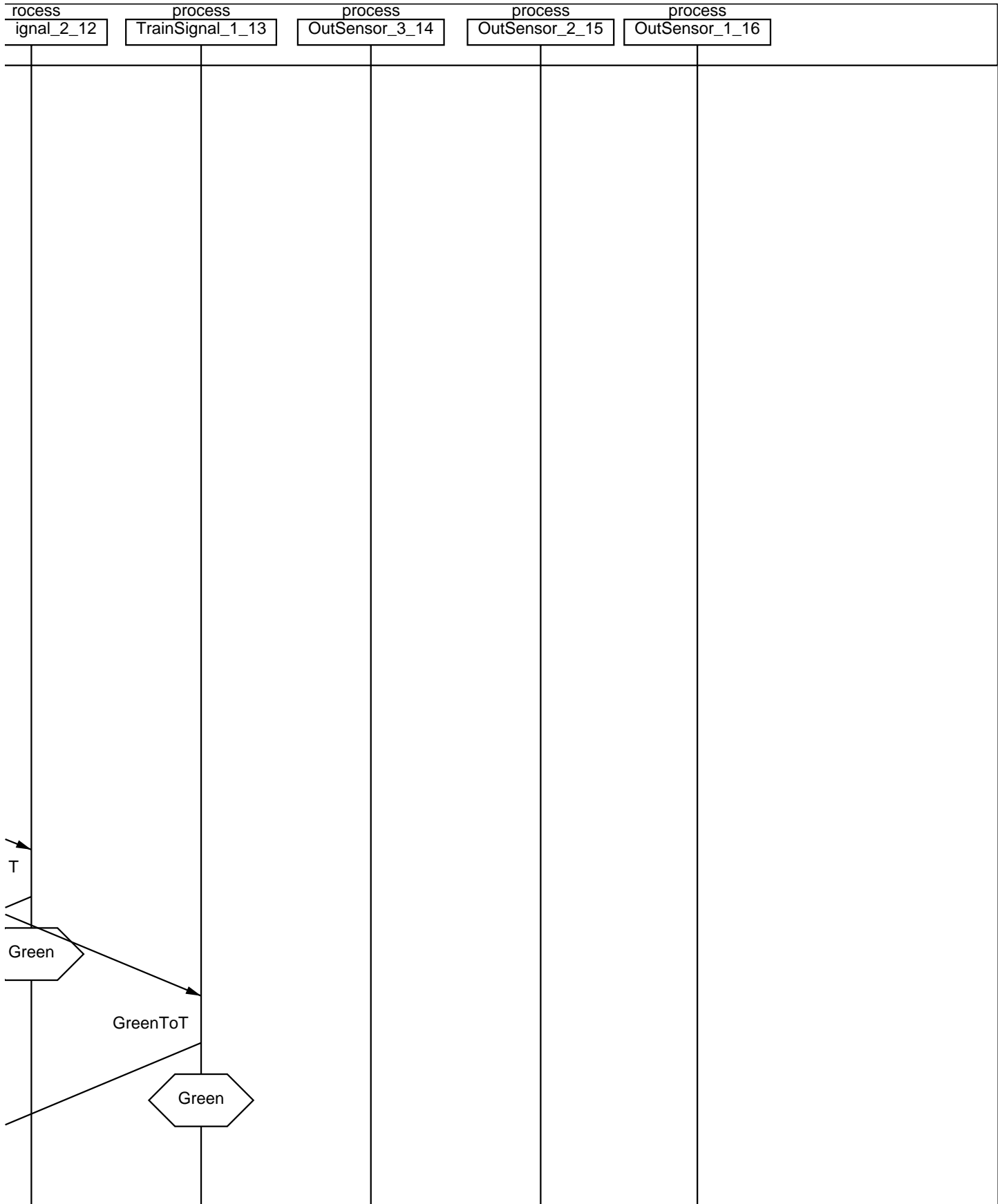




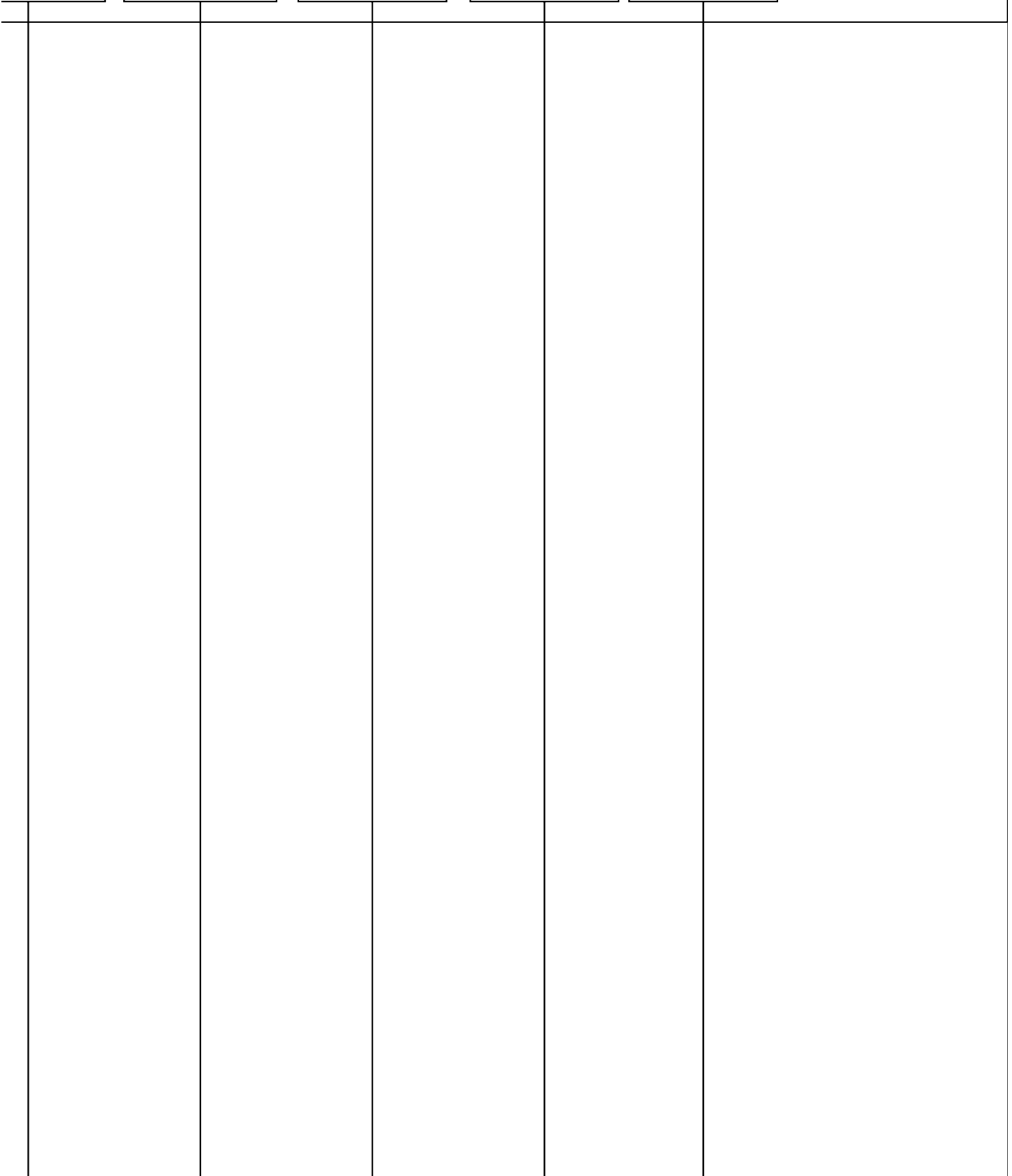


rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

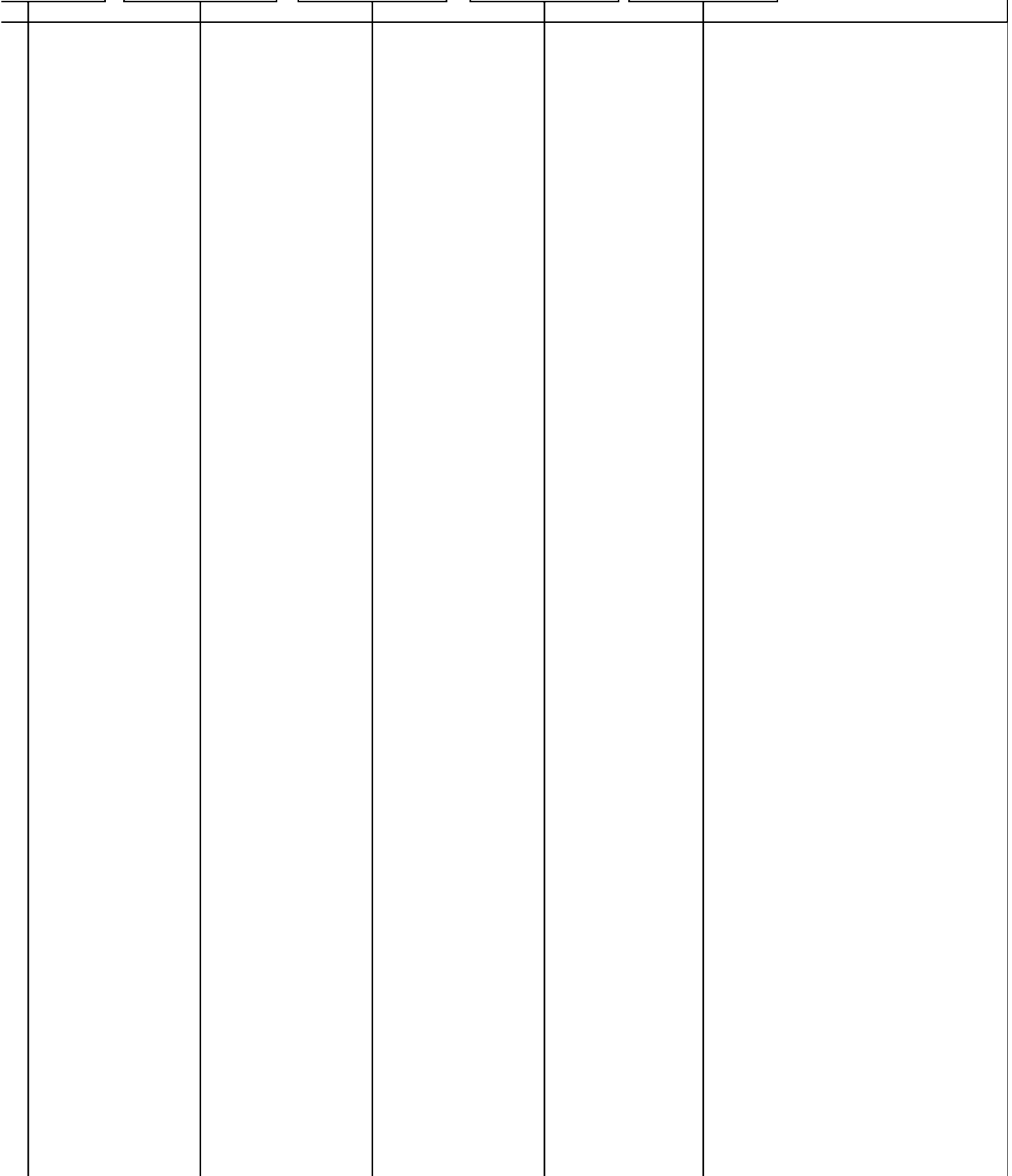




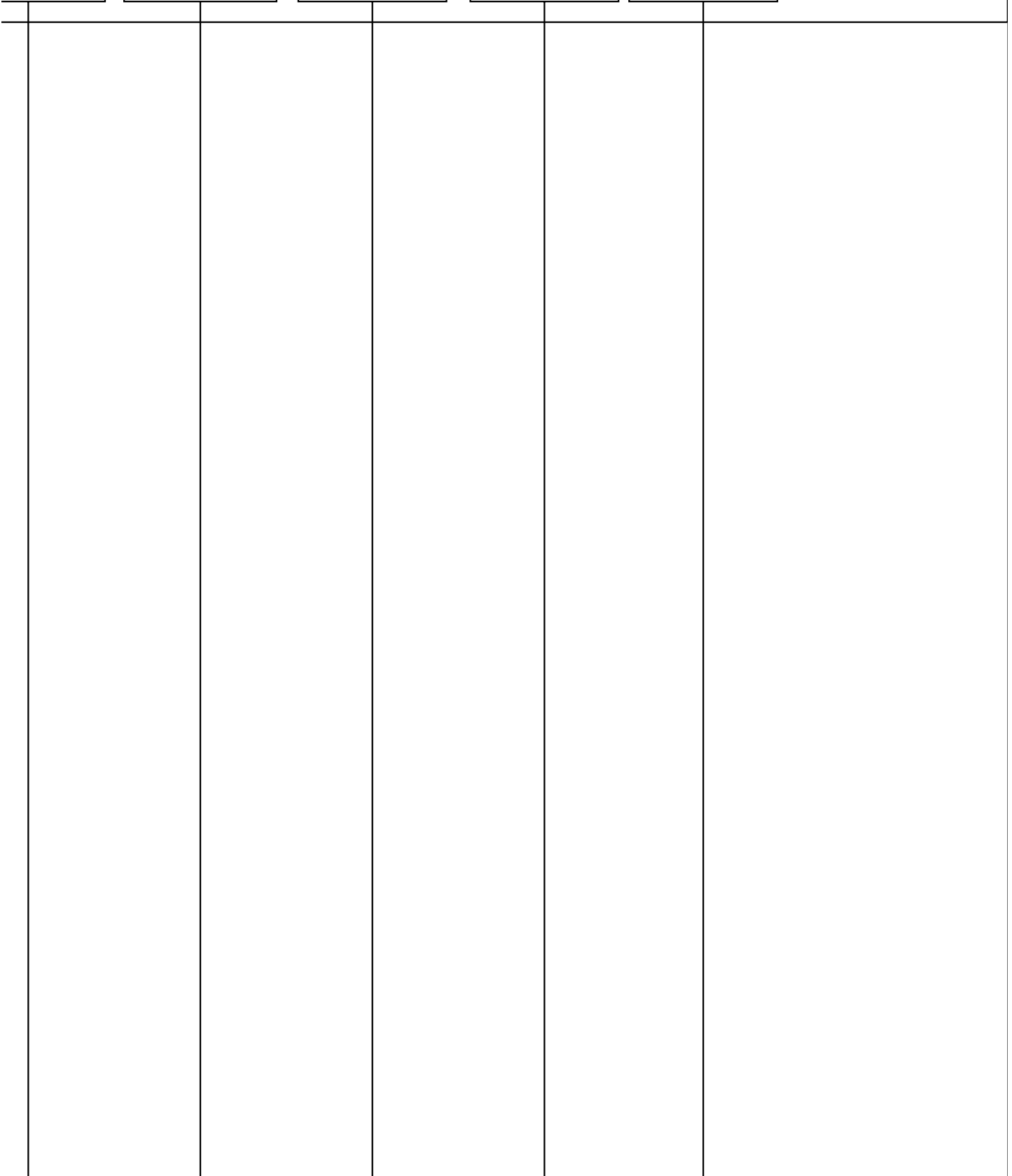
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------



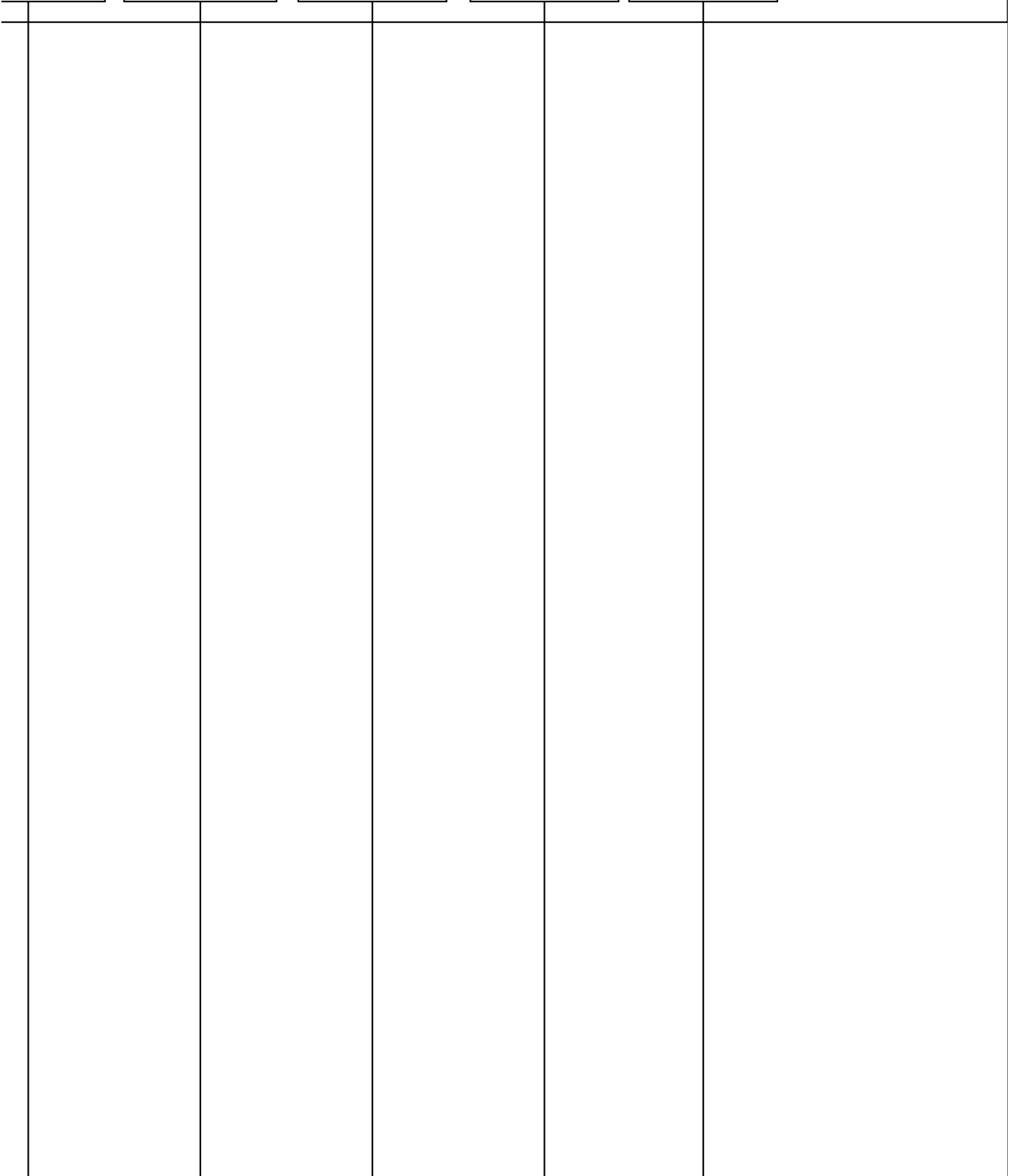
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

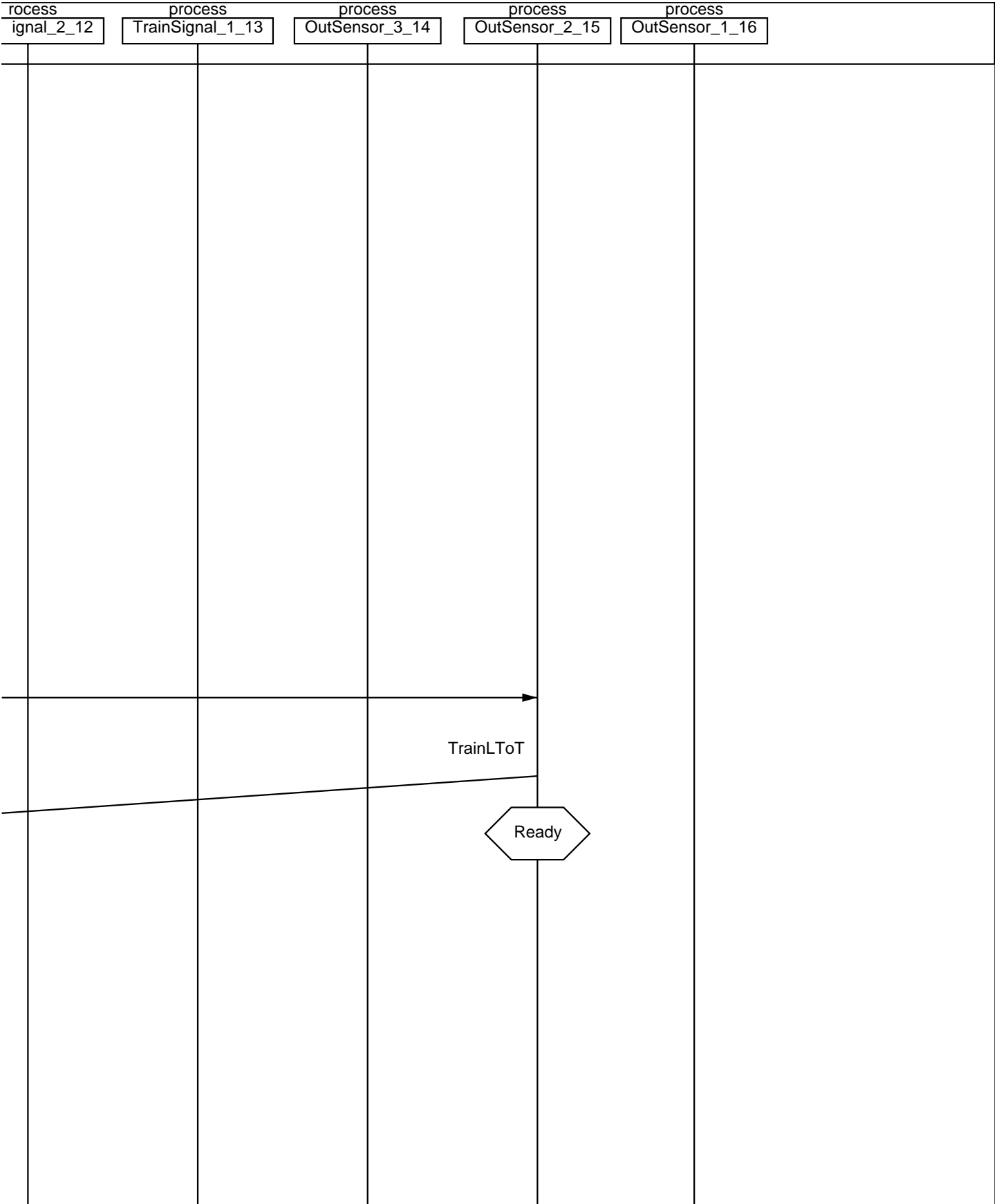


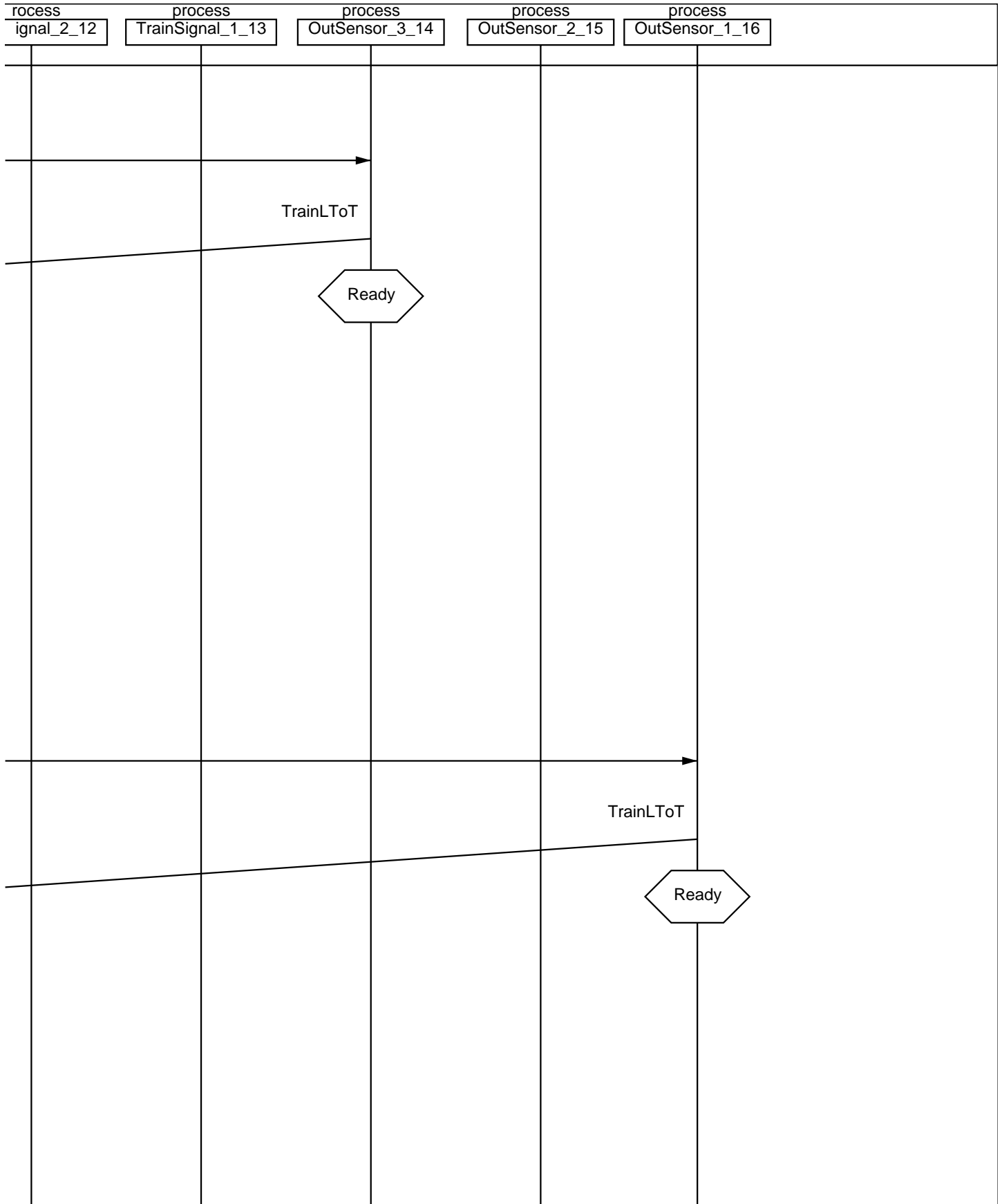
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------



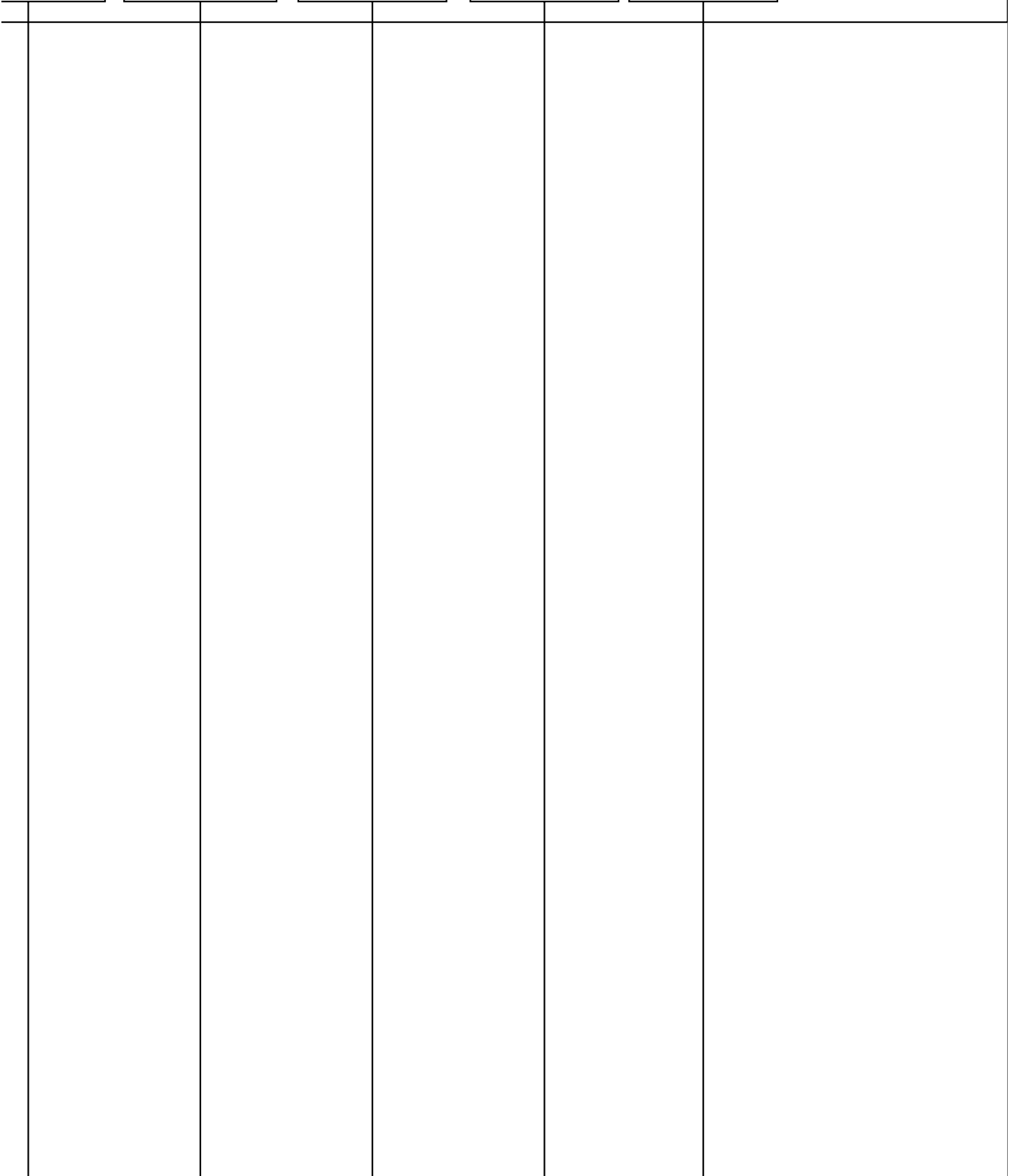
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

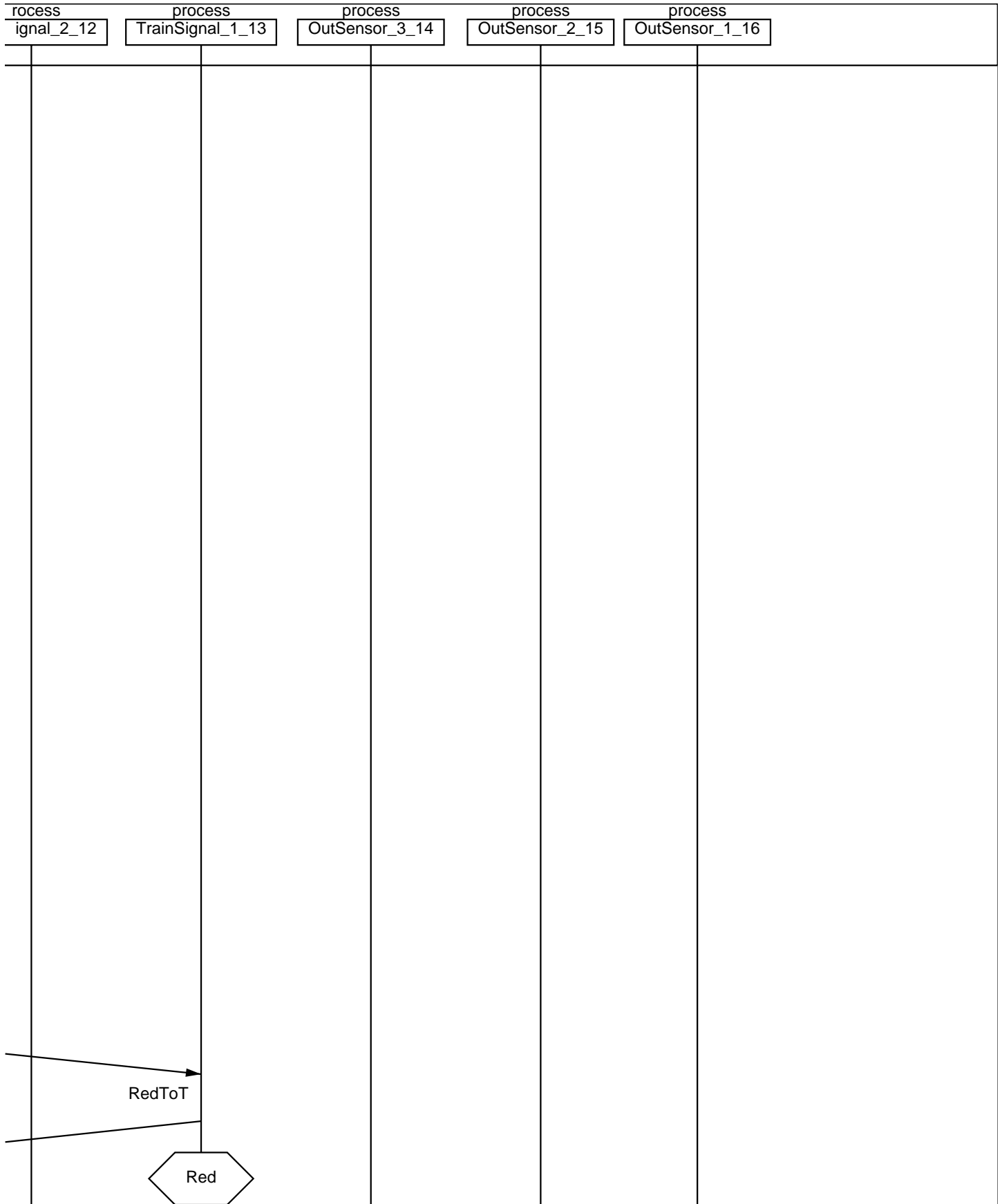


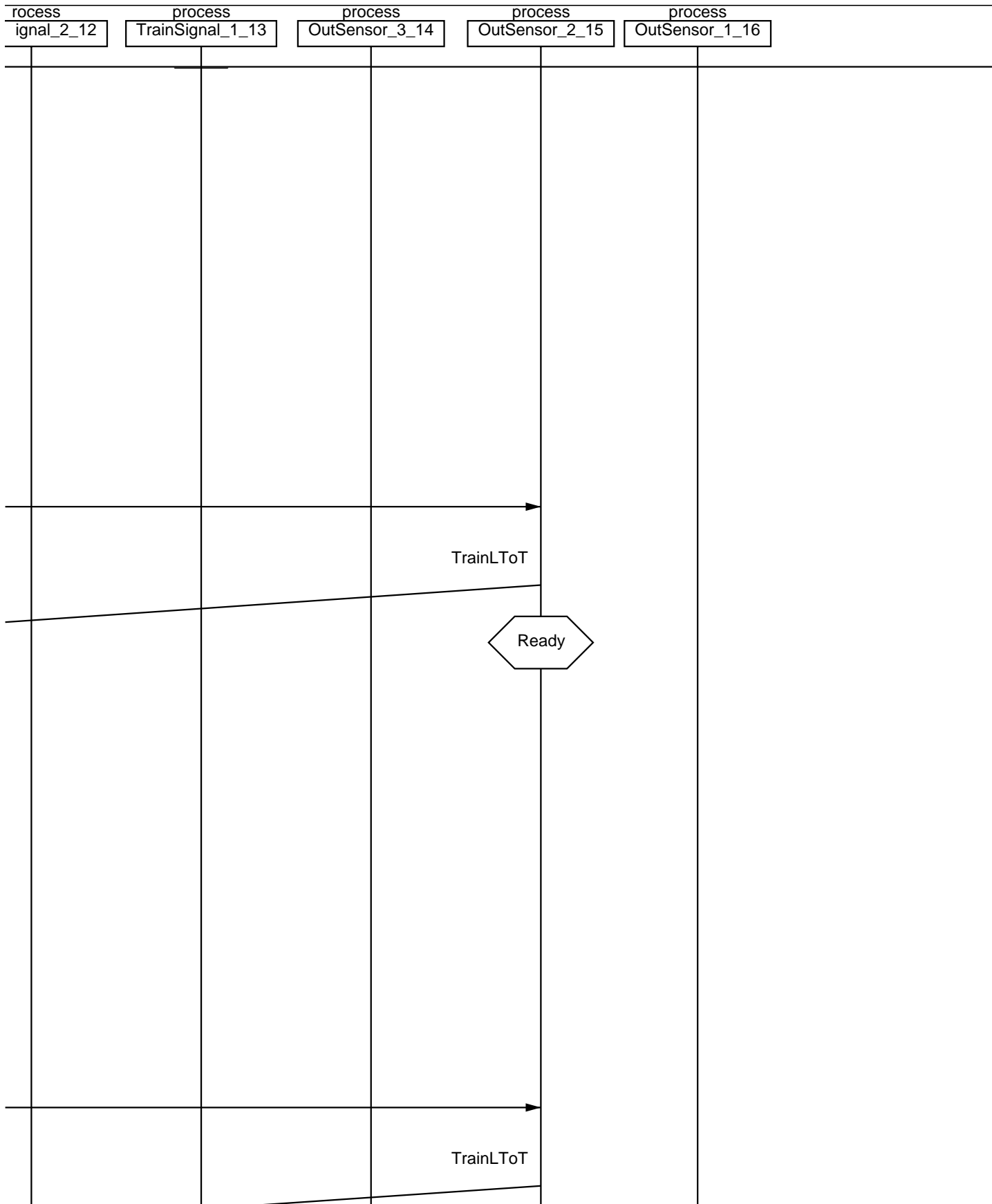


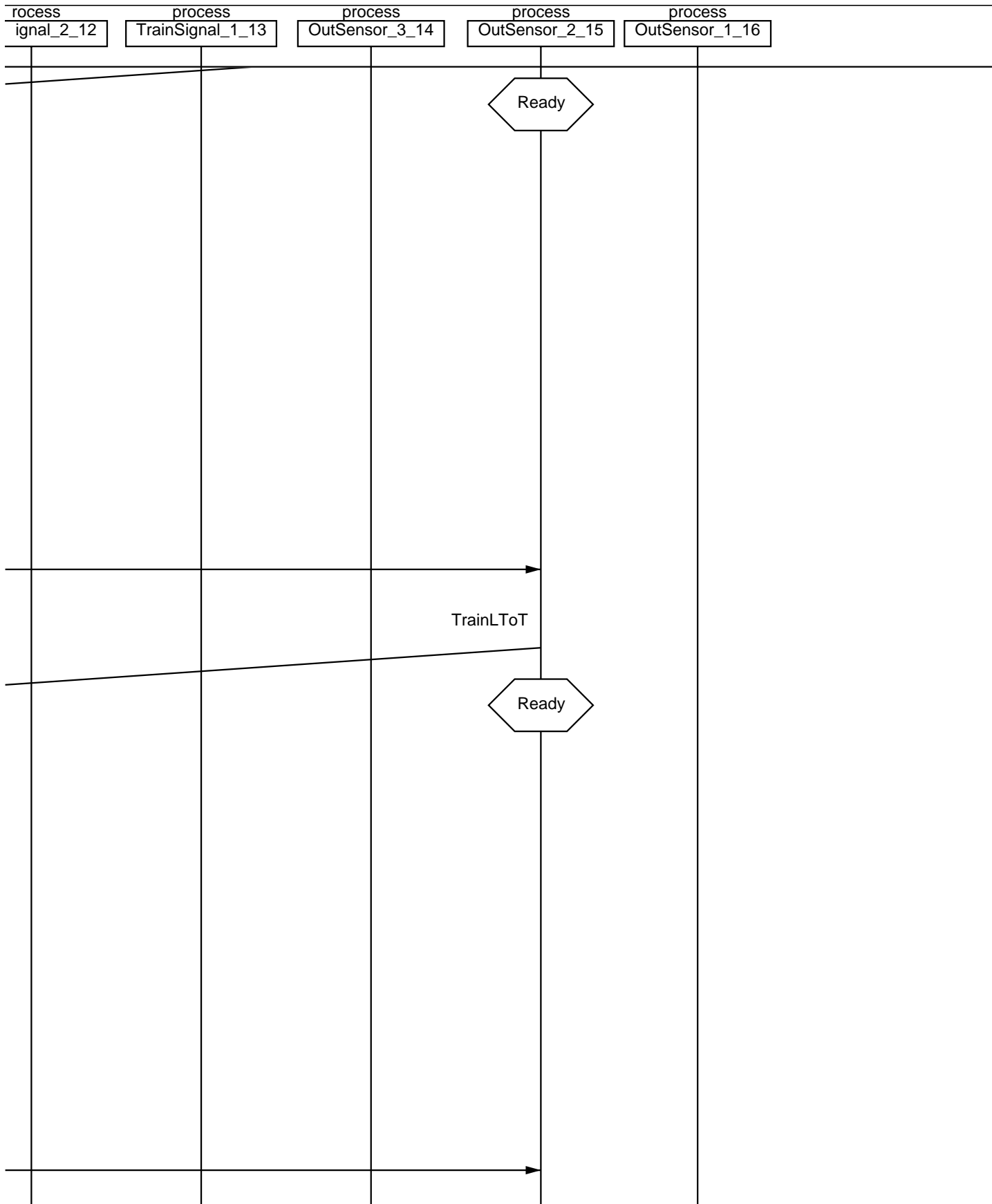


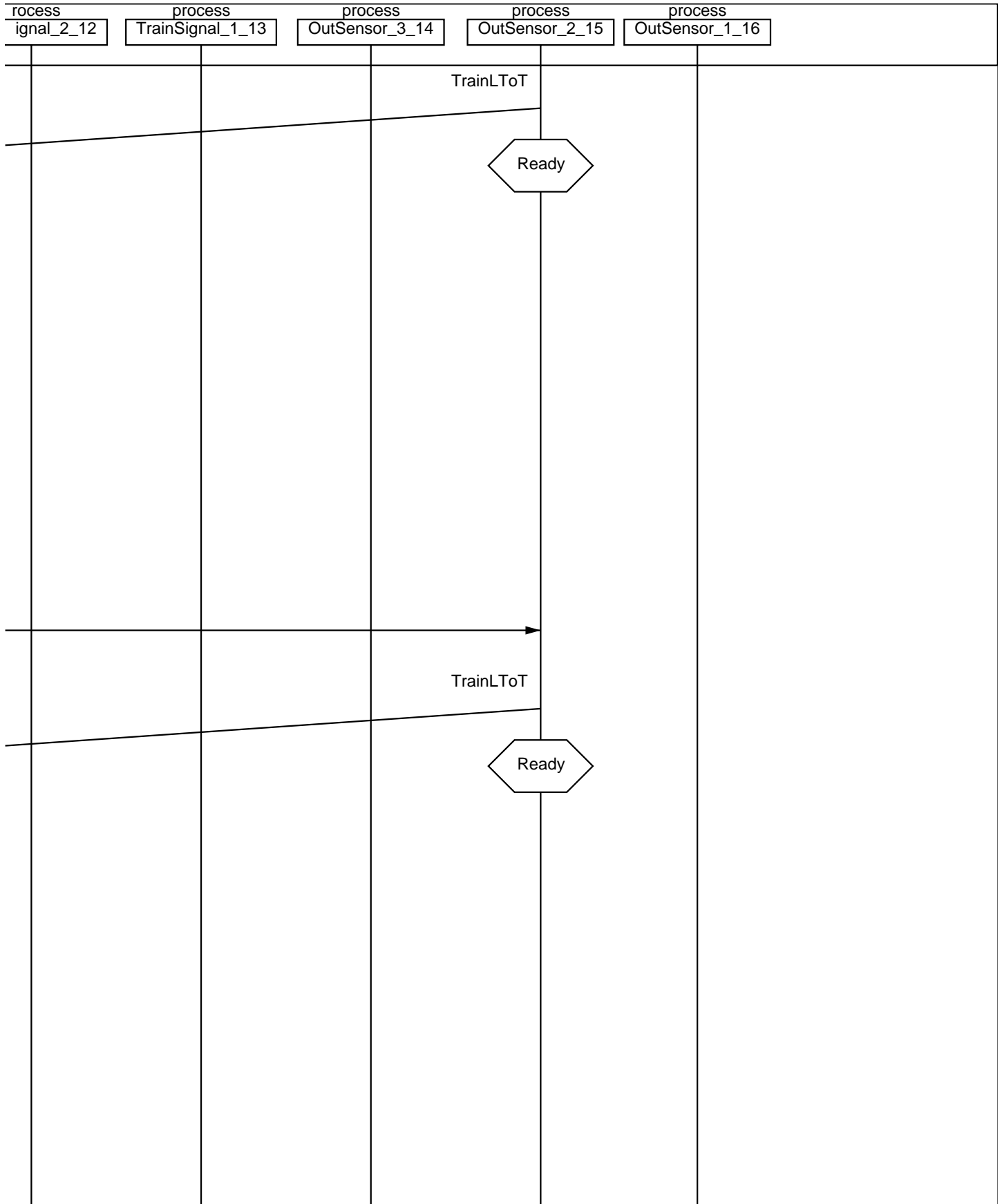
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

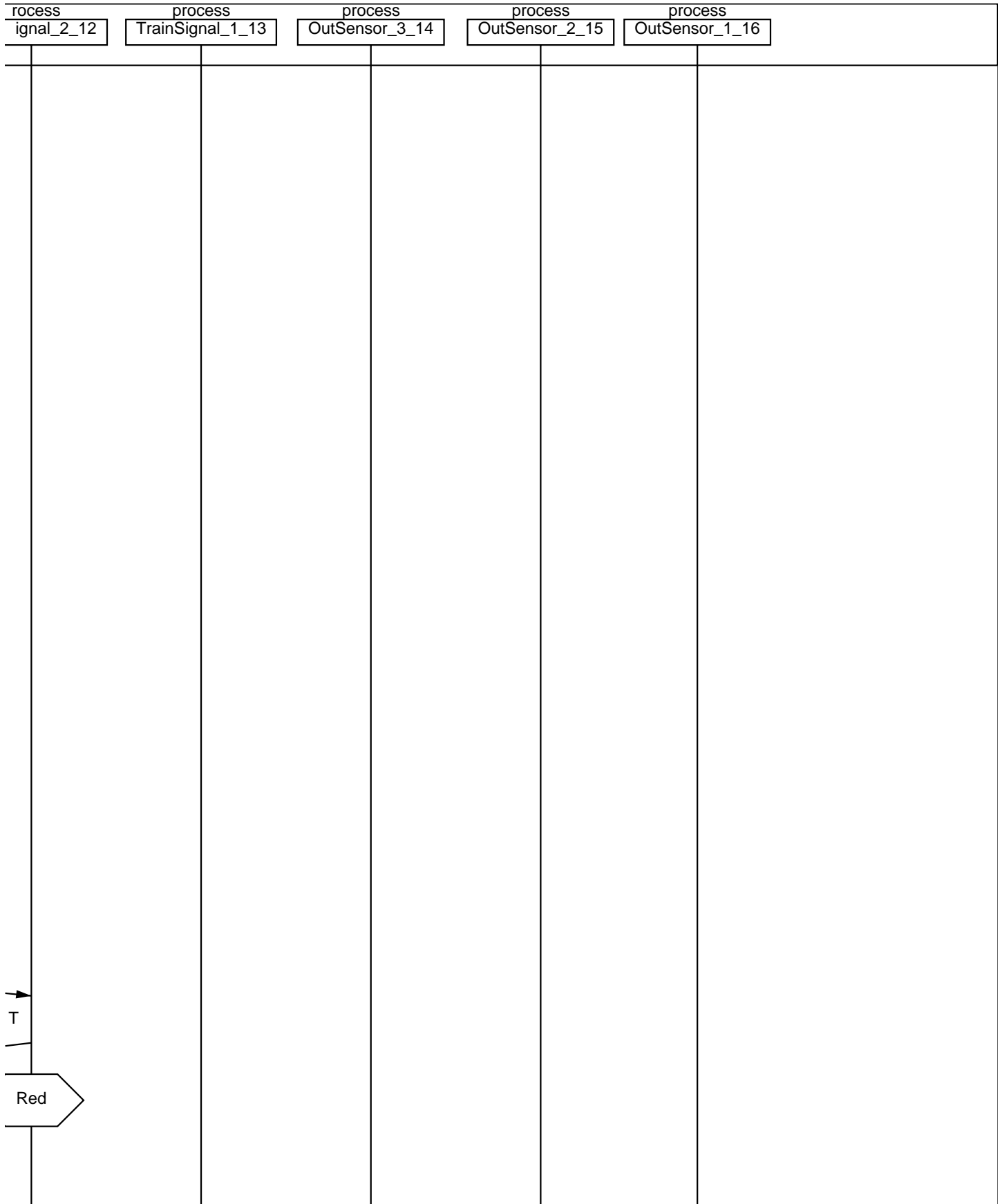


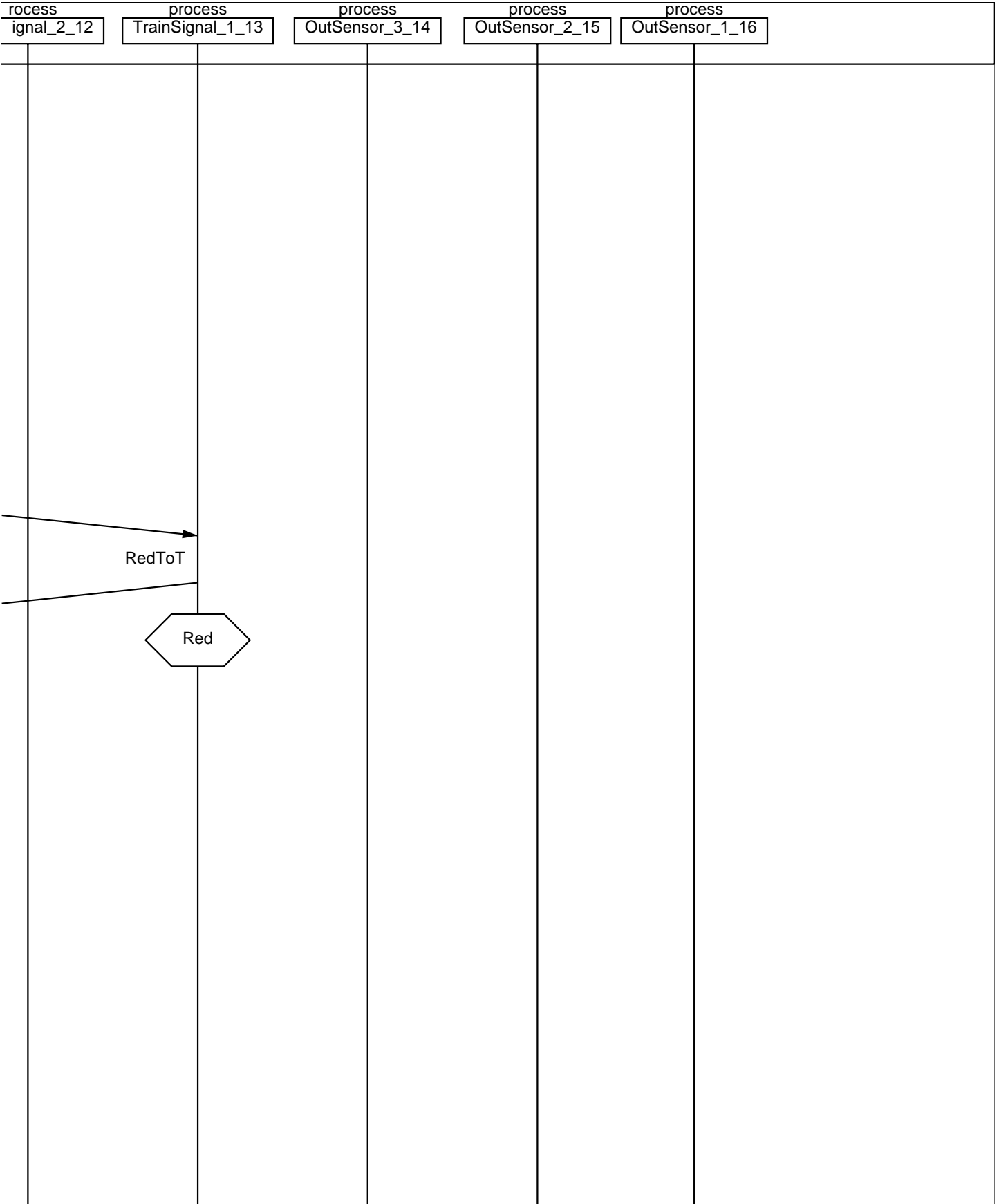




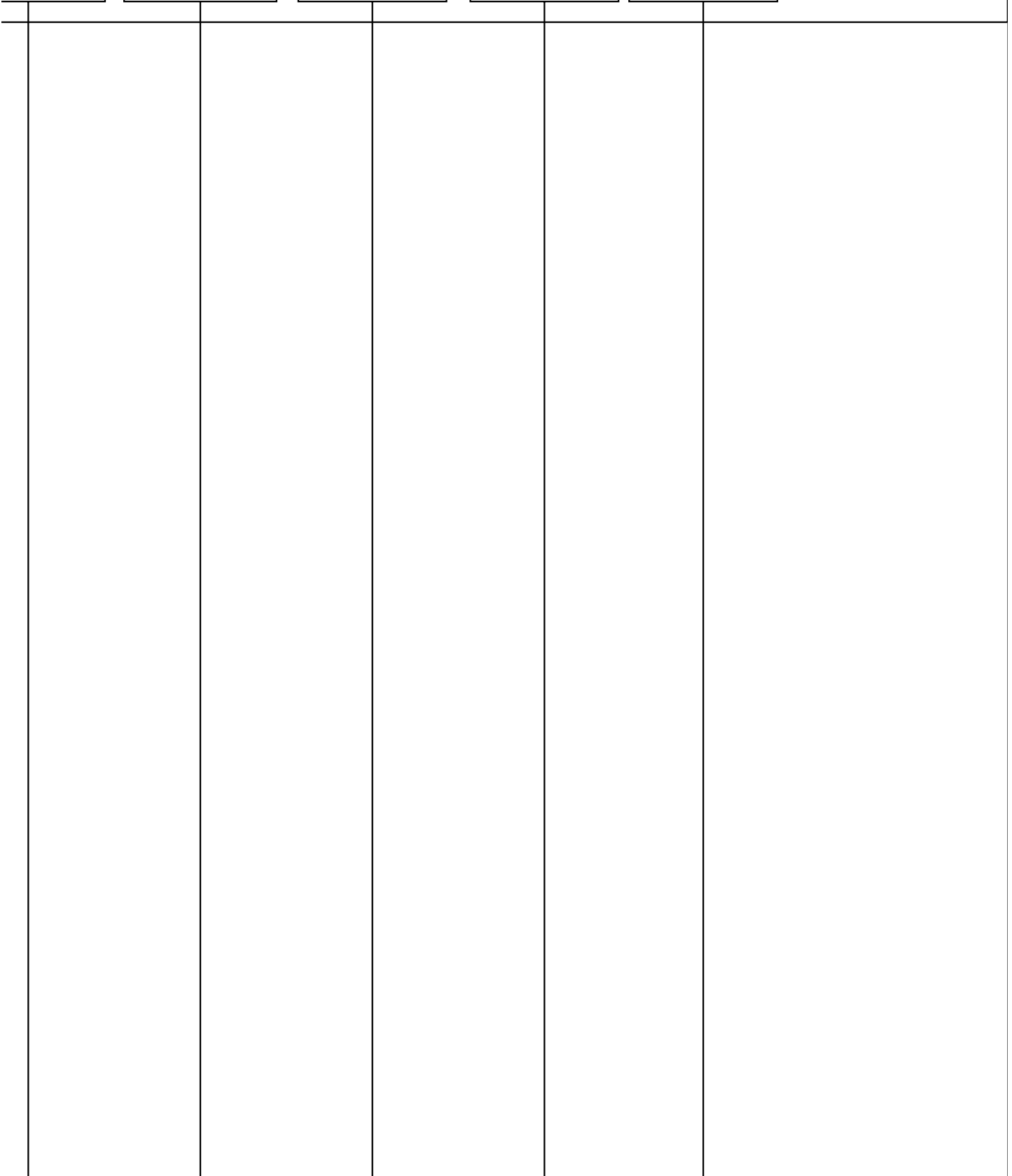




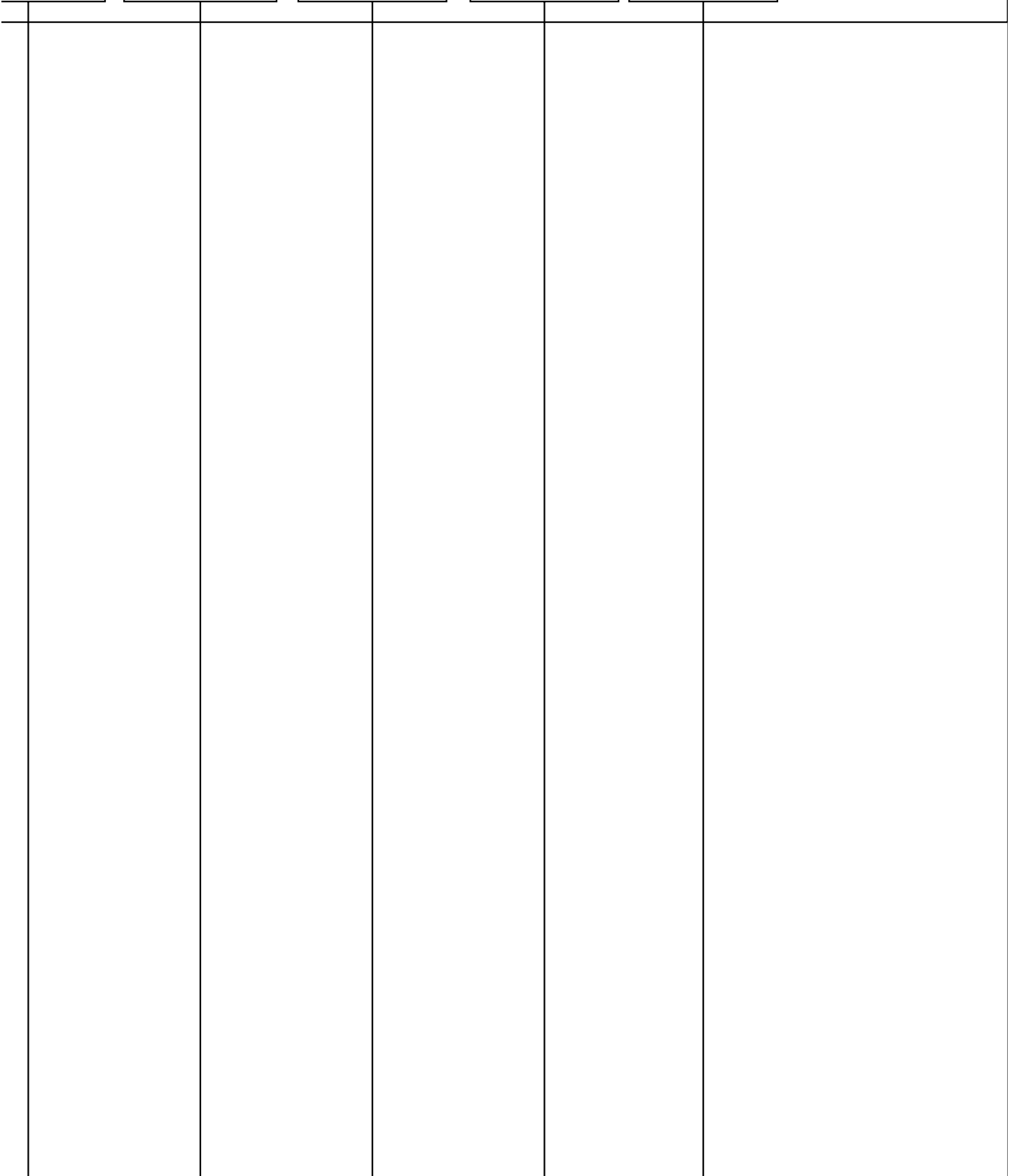


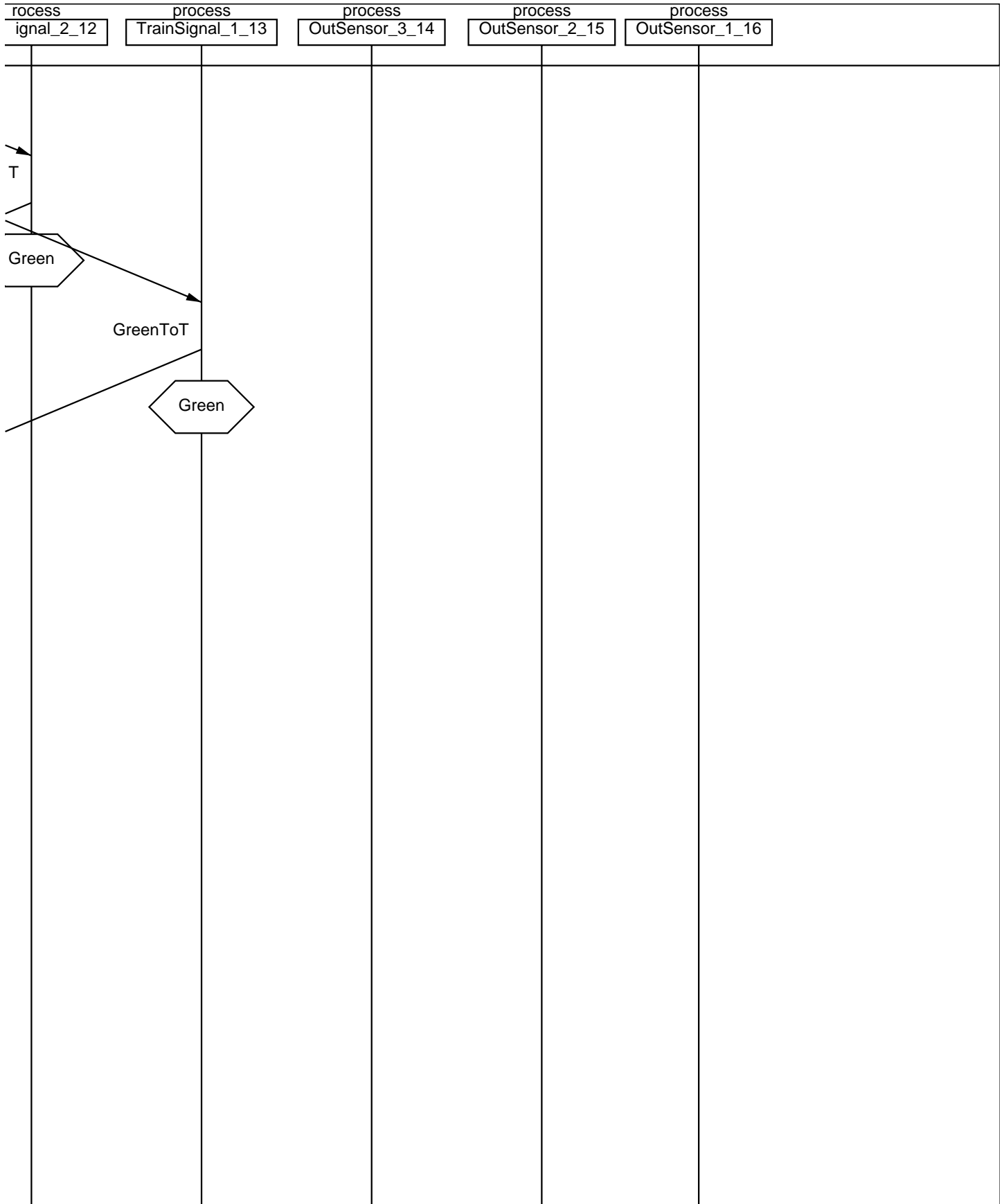


rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------



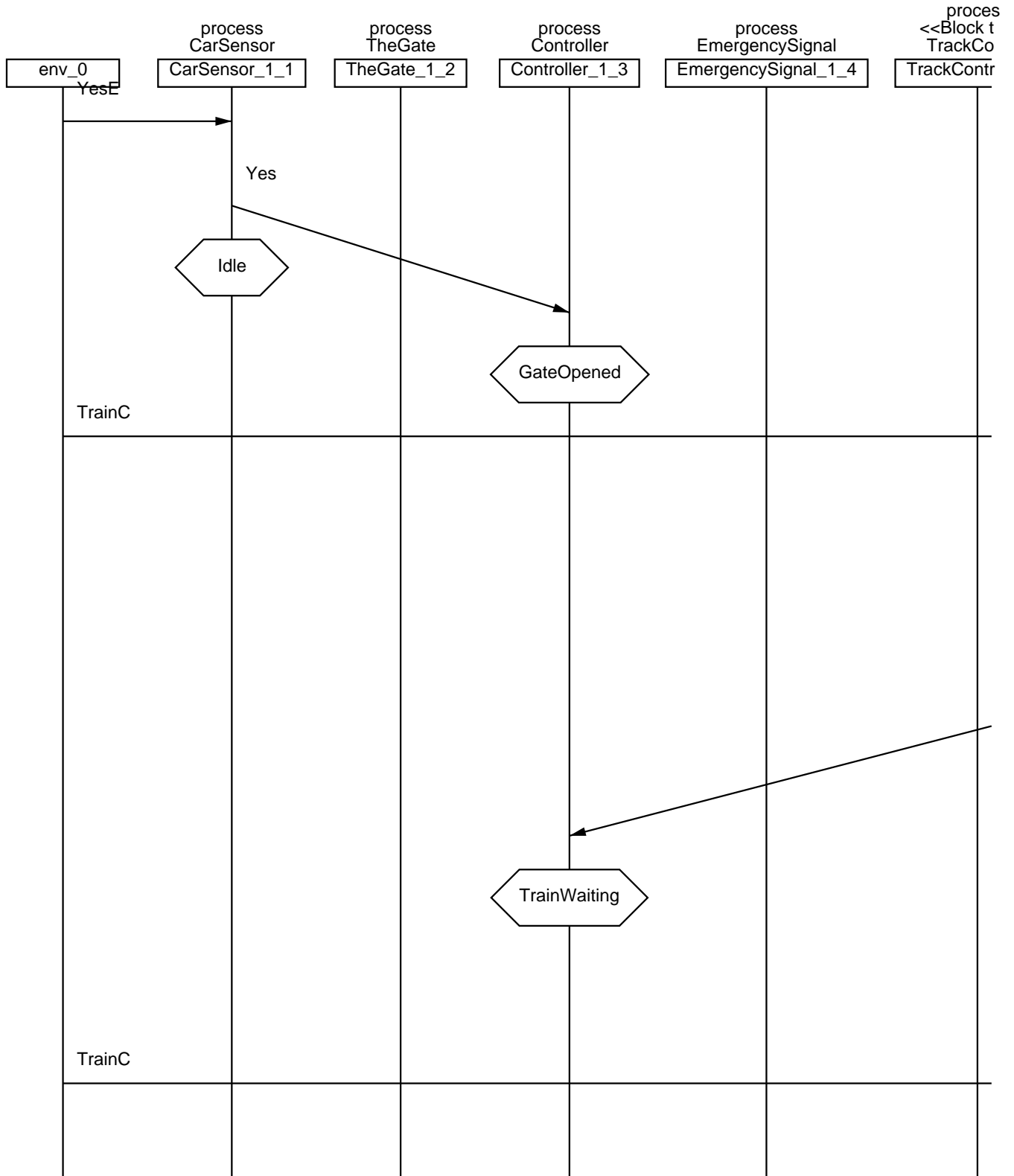
rocess ignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
----------------------	-----------------------------	---------------------------	---------------------------	---------------------------

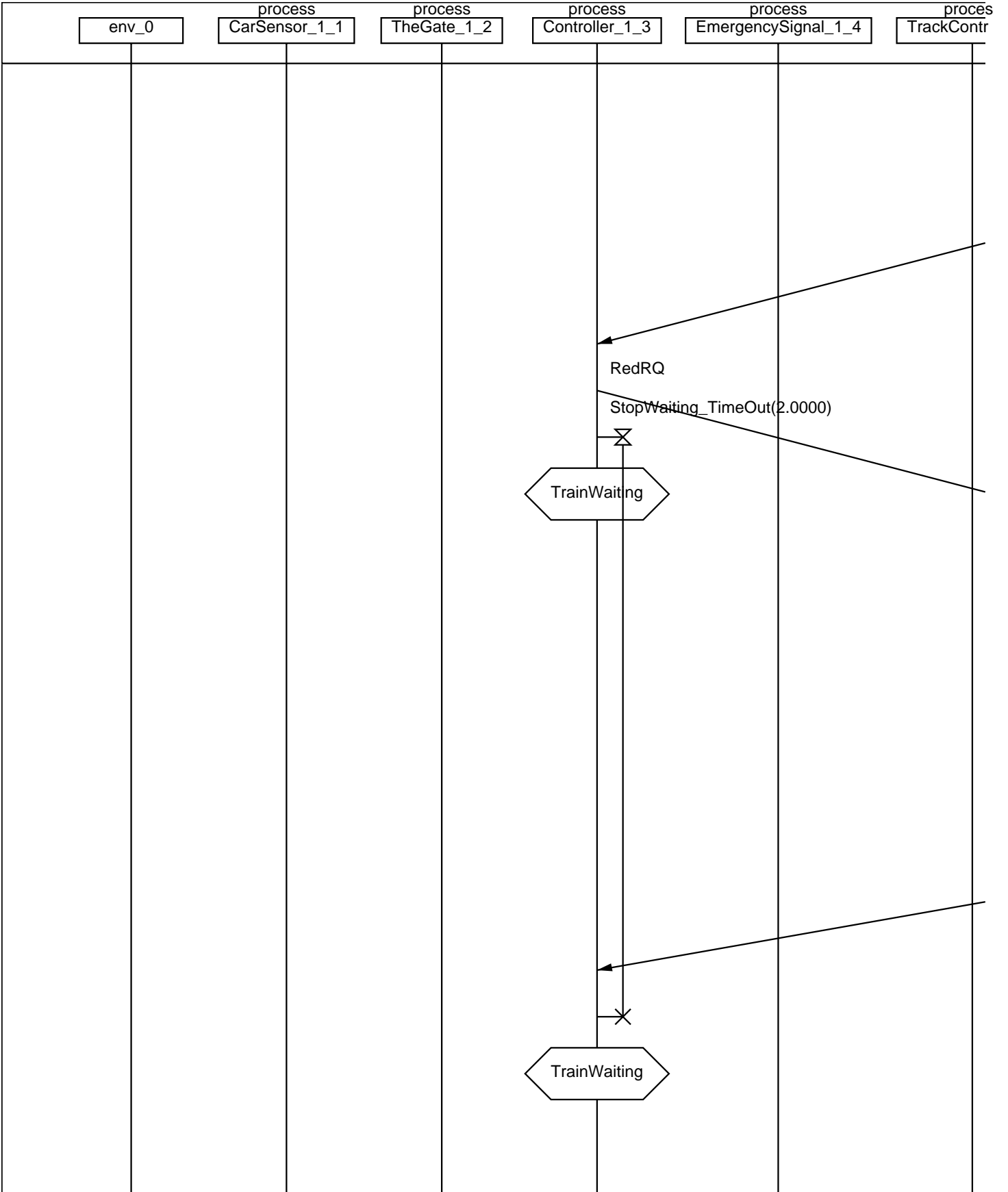


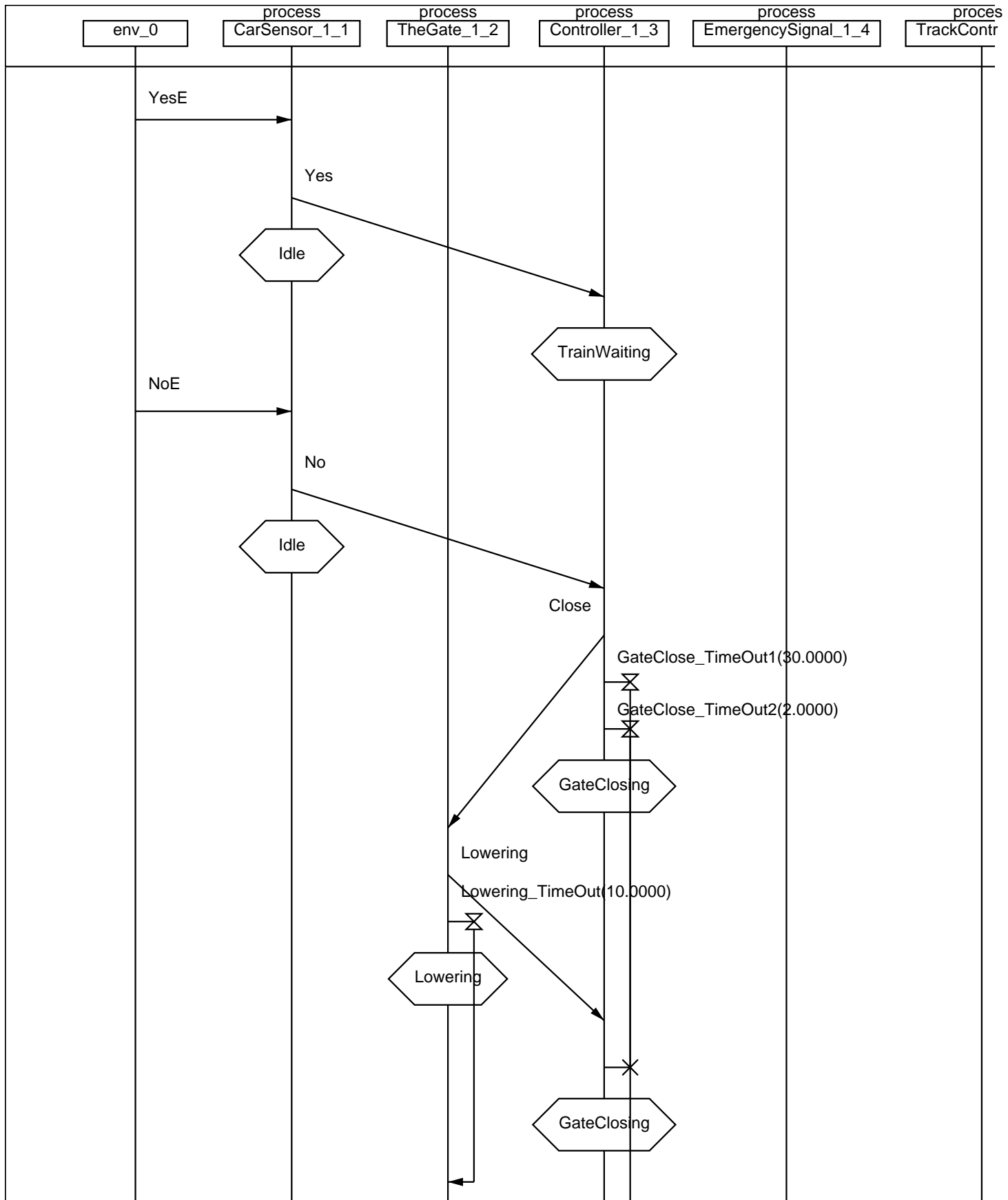


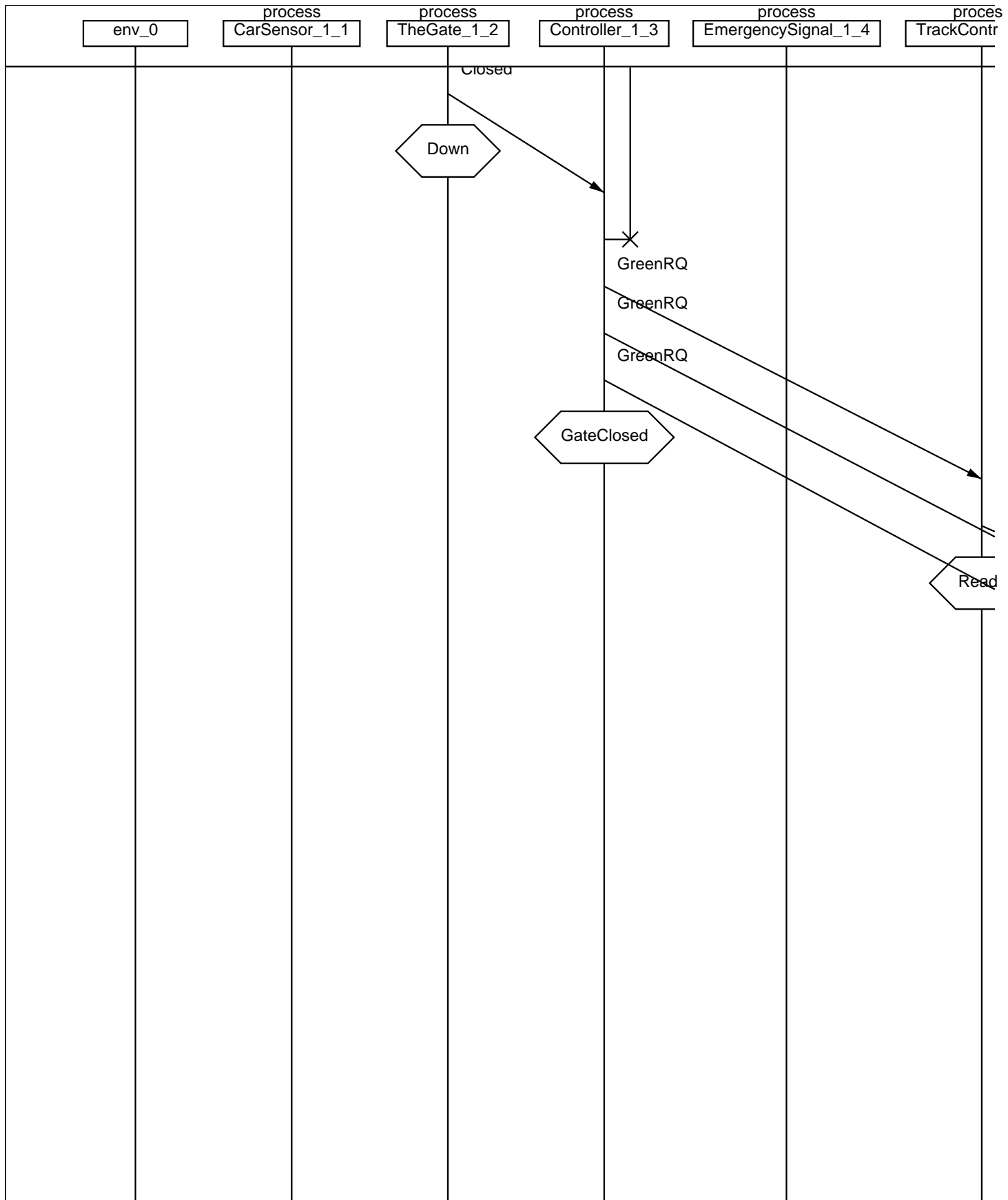
MSC CompleteMSC_TestCaseE

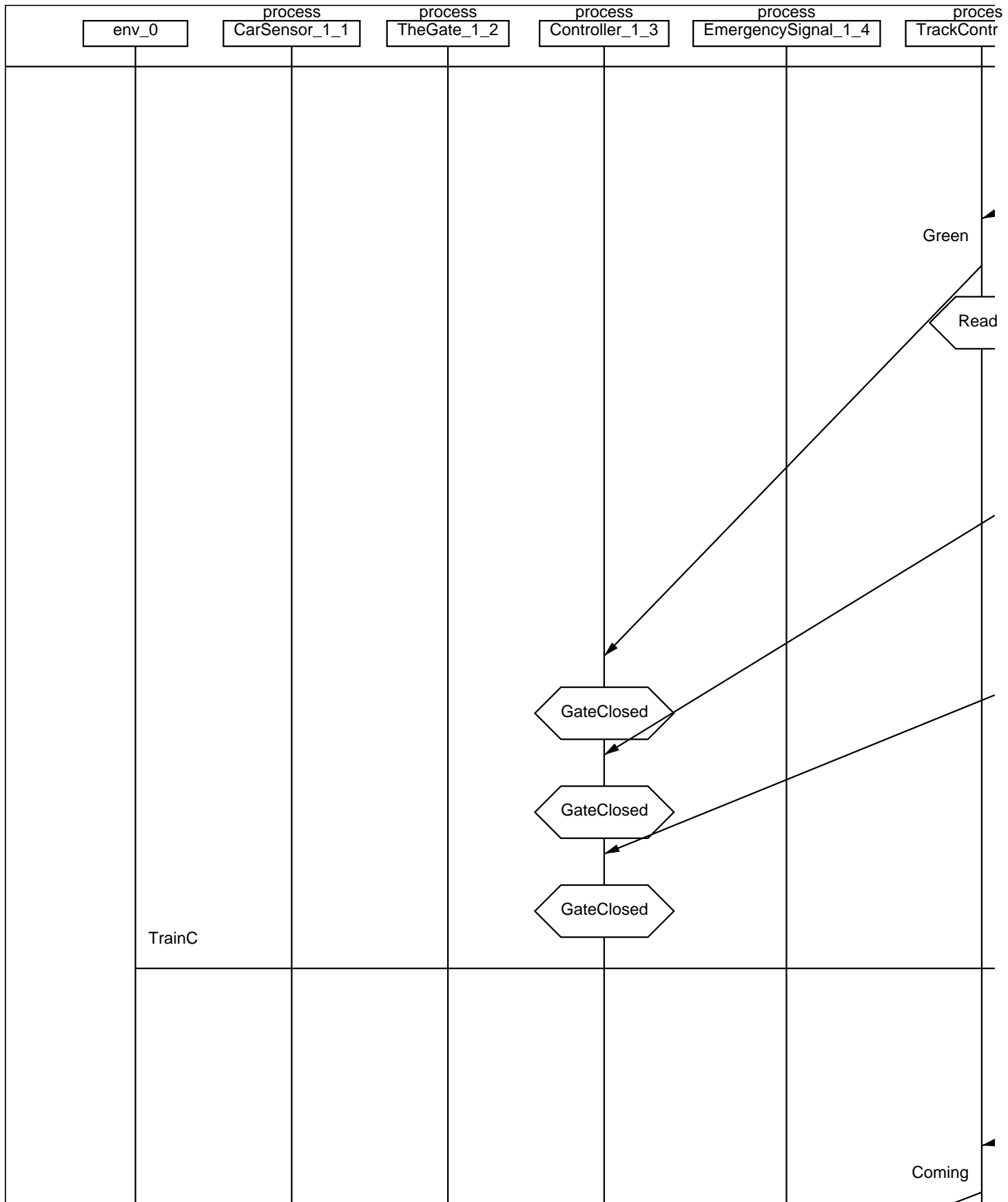
Simulation trace
generated by
SDL Simulator 4.3

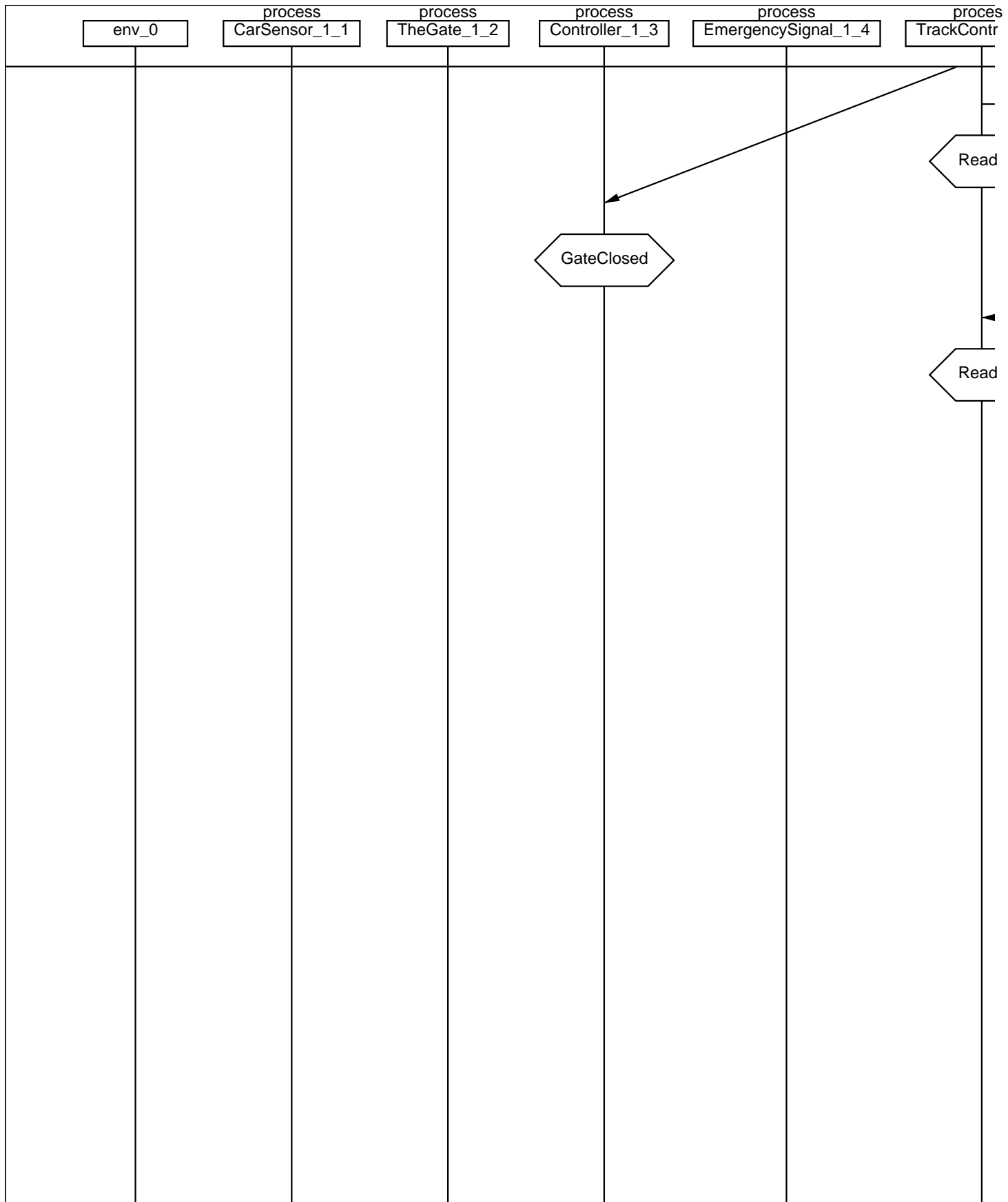


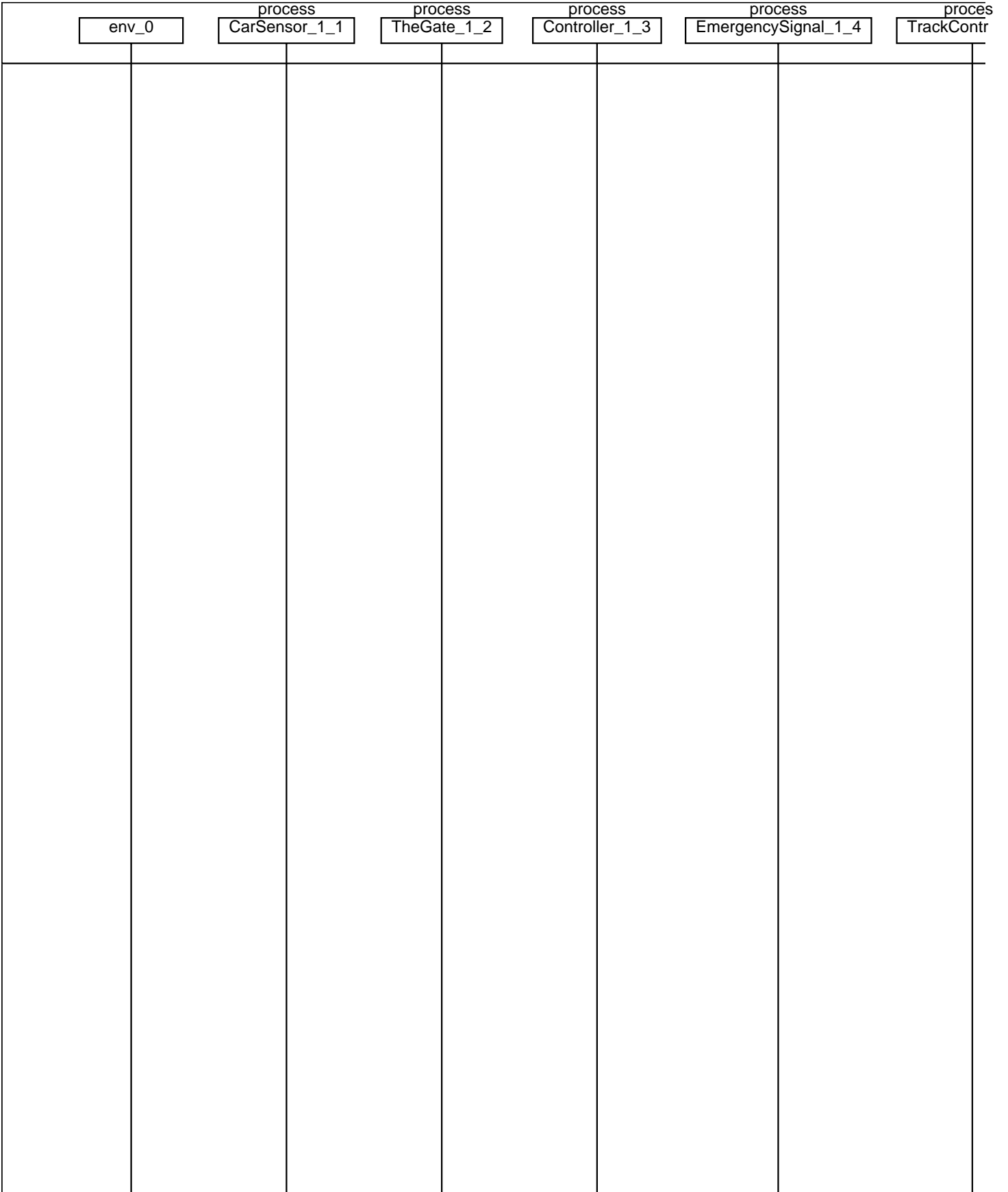


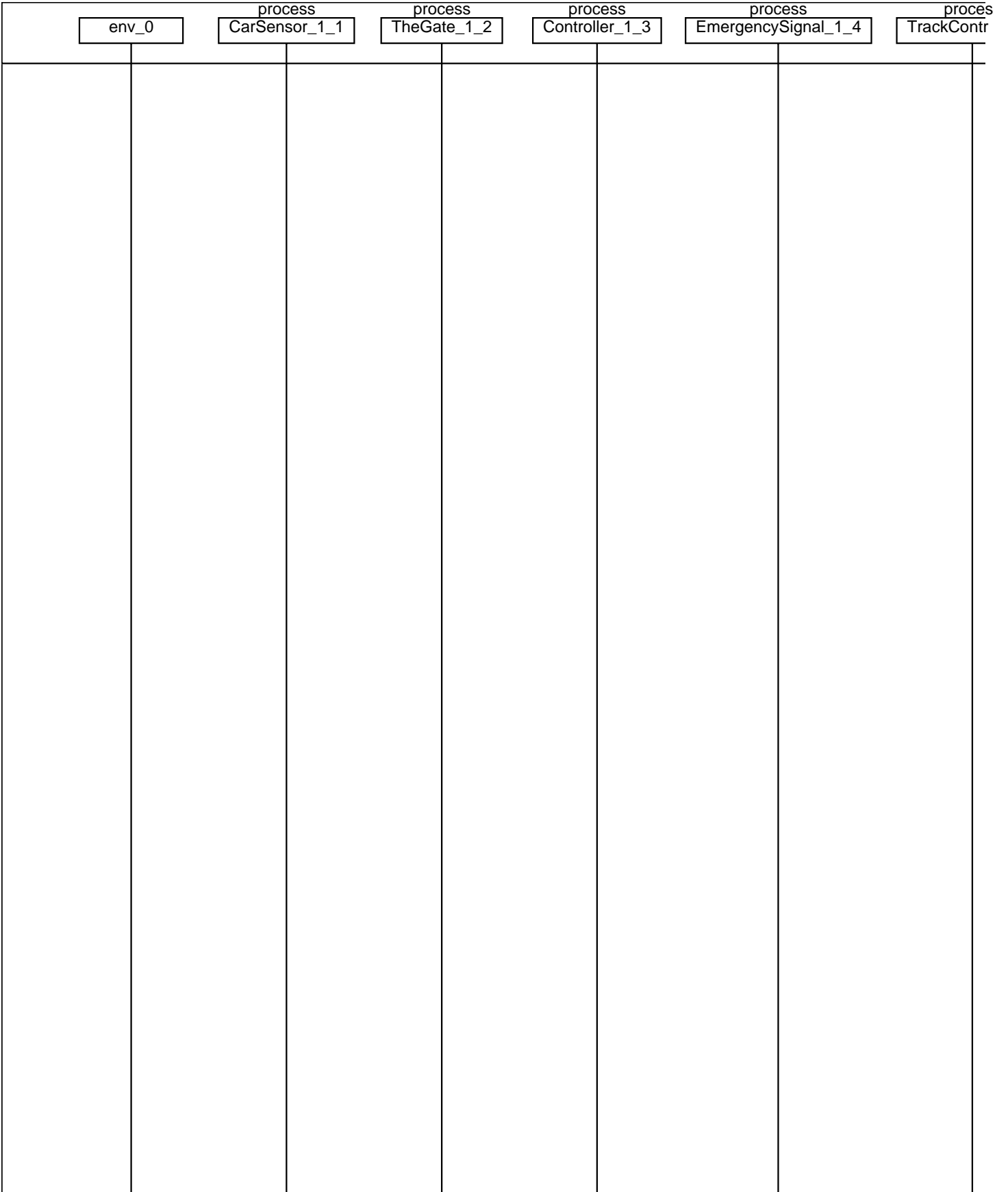


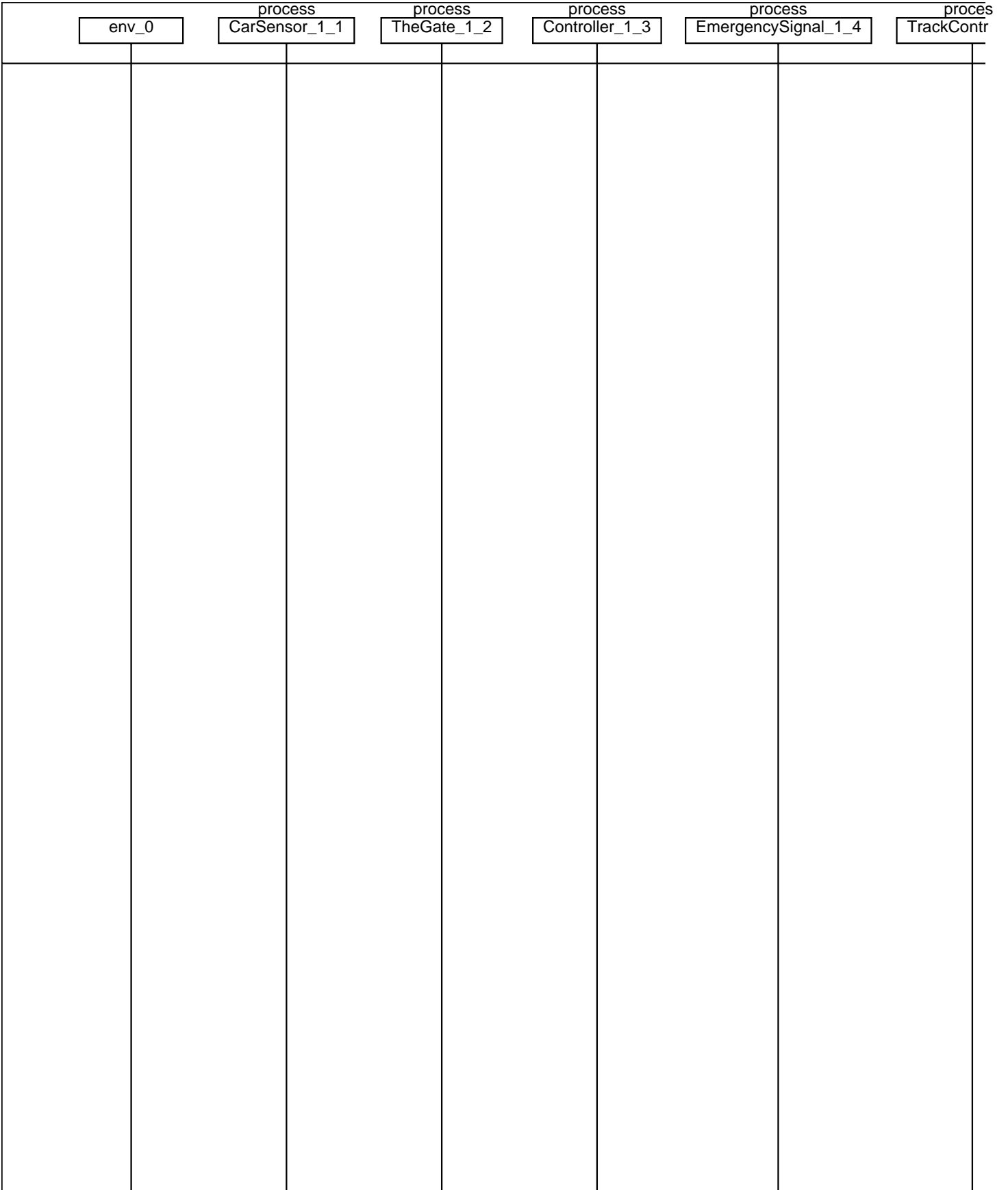


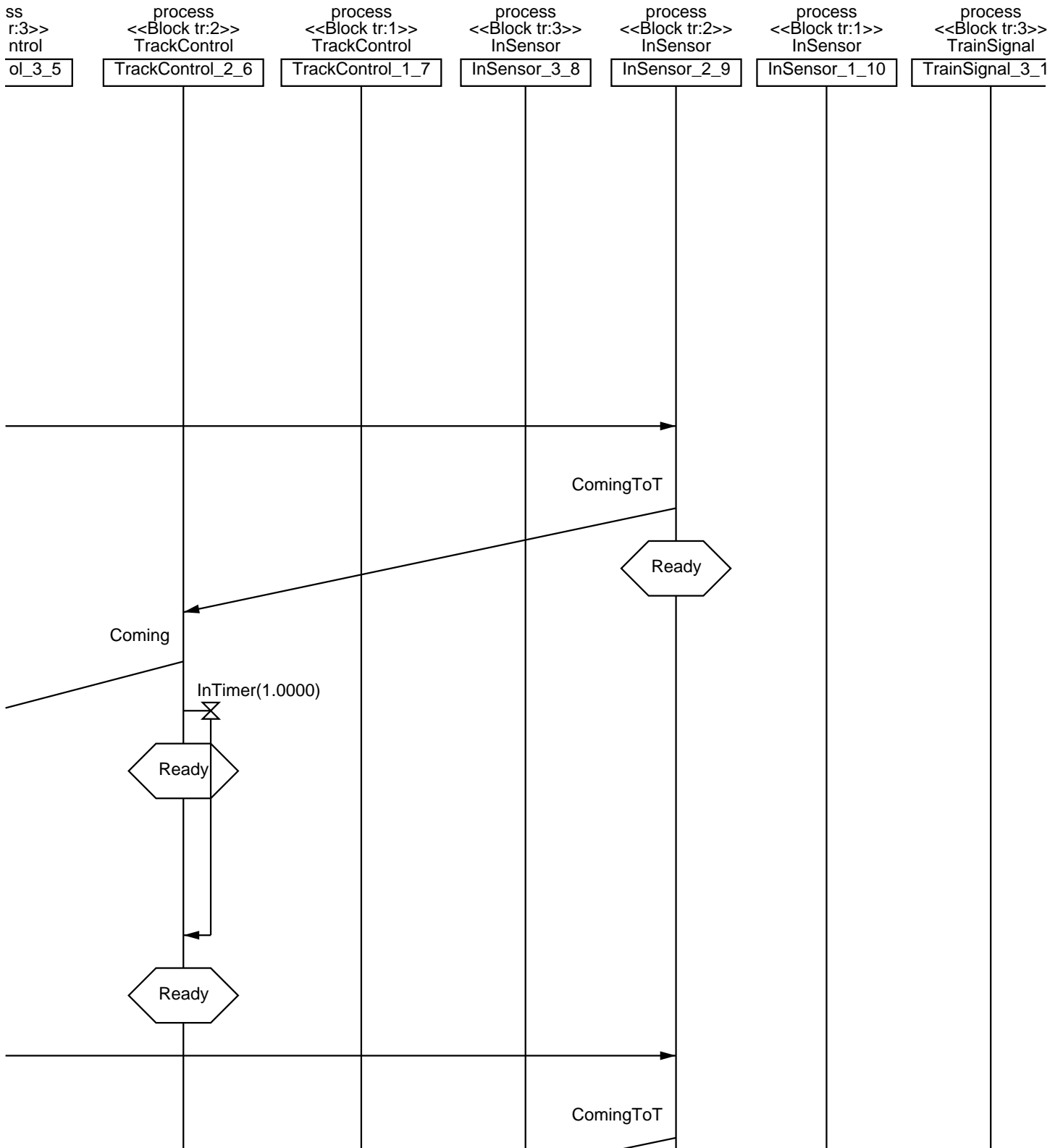


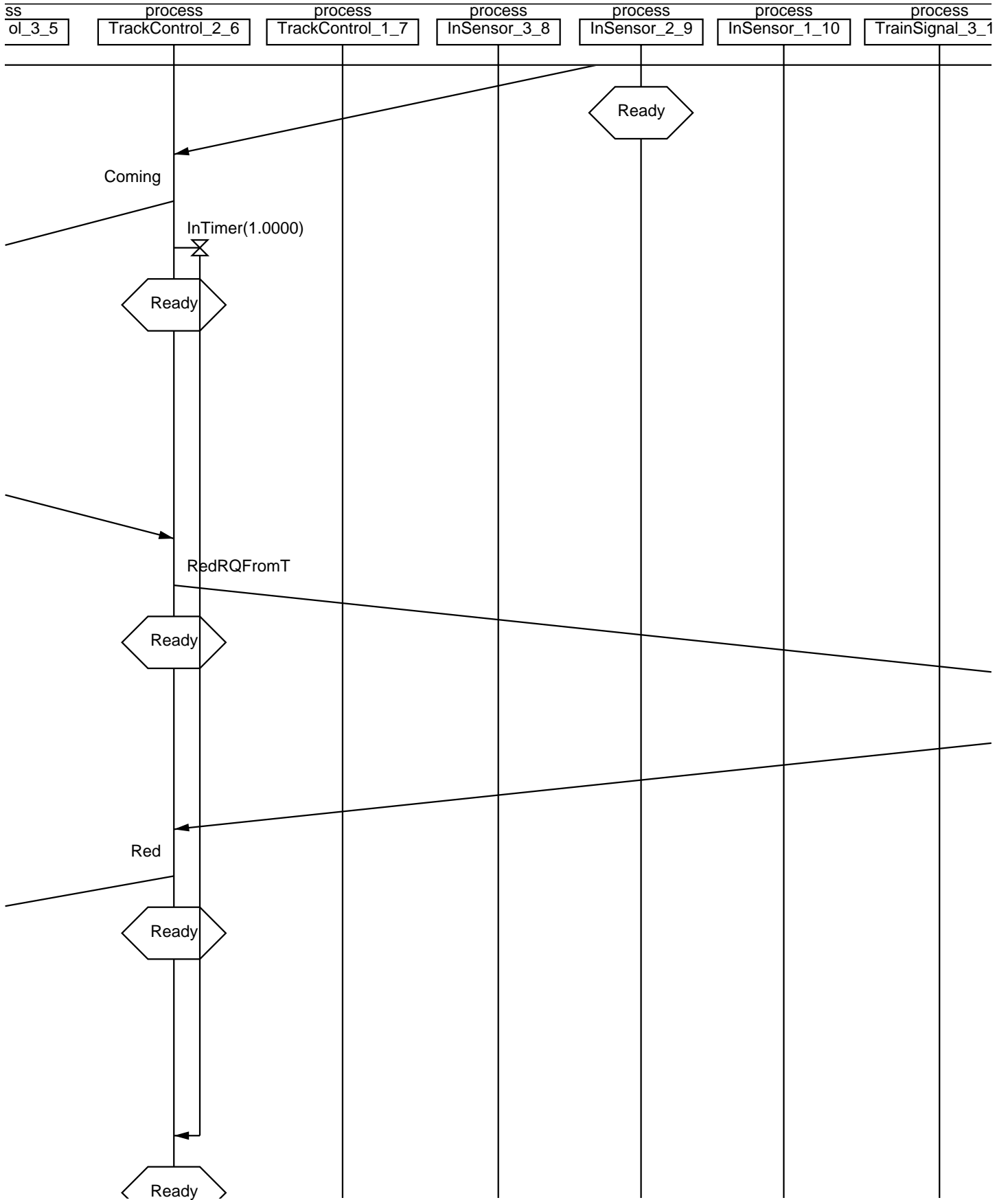




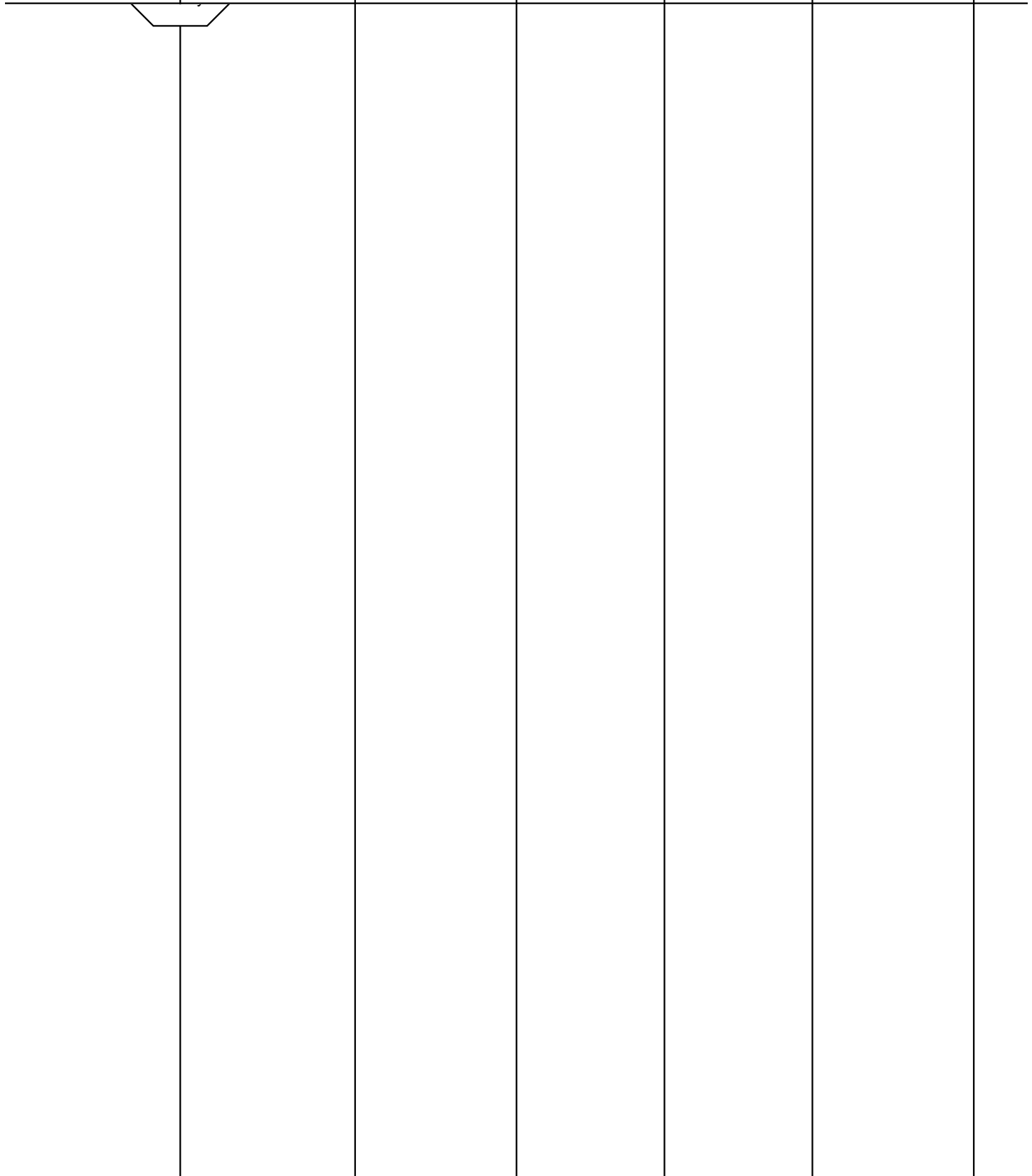


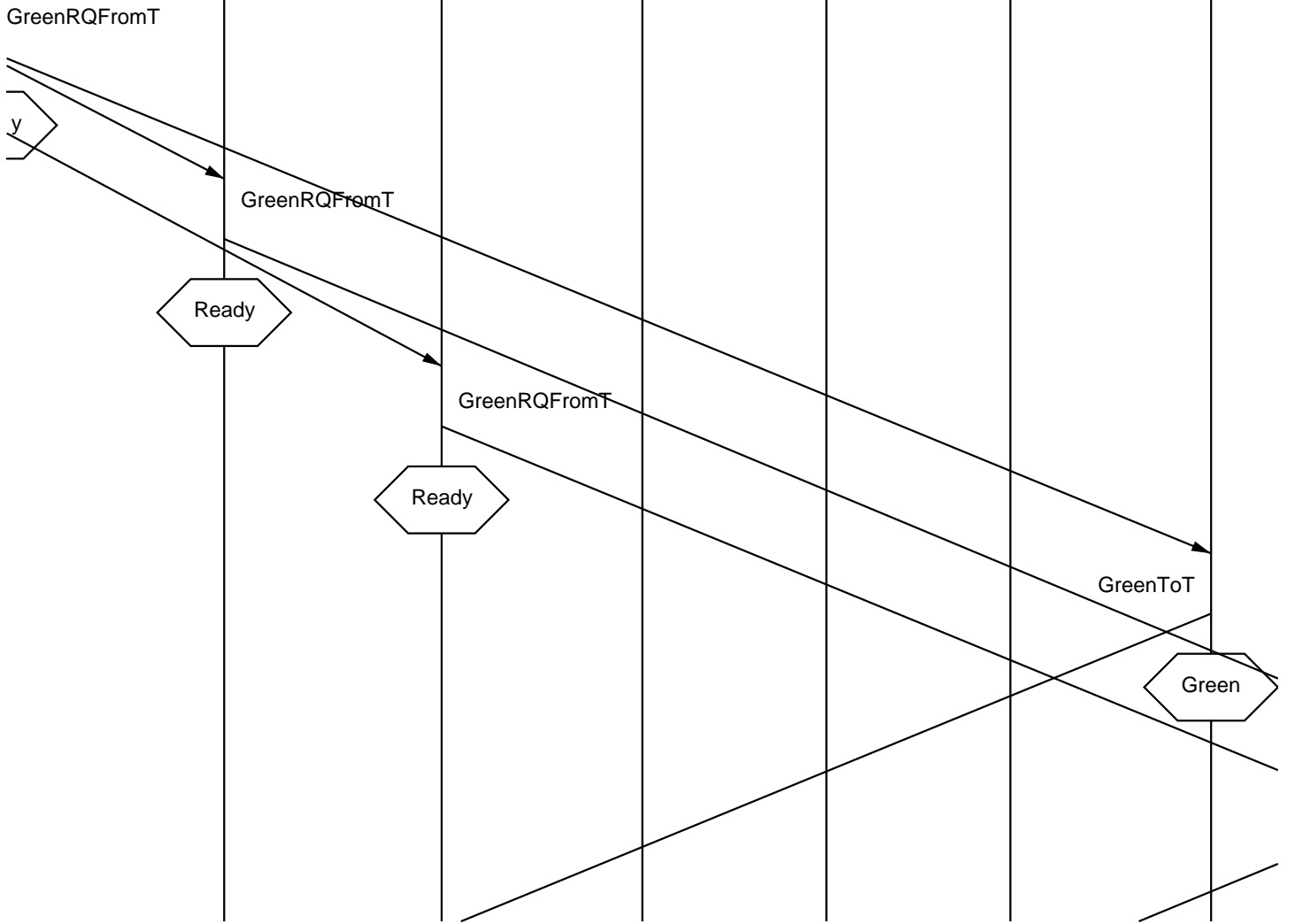
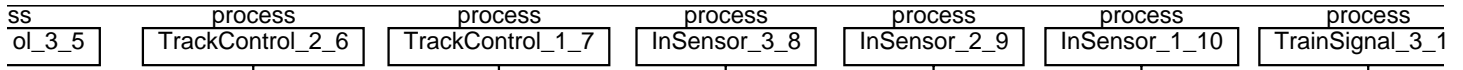


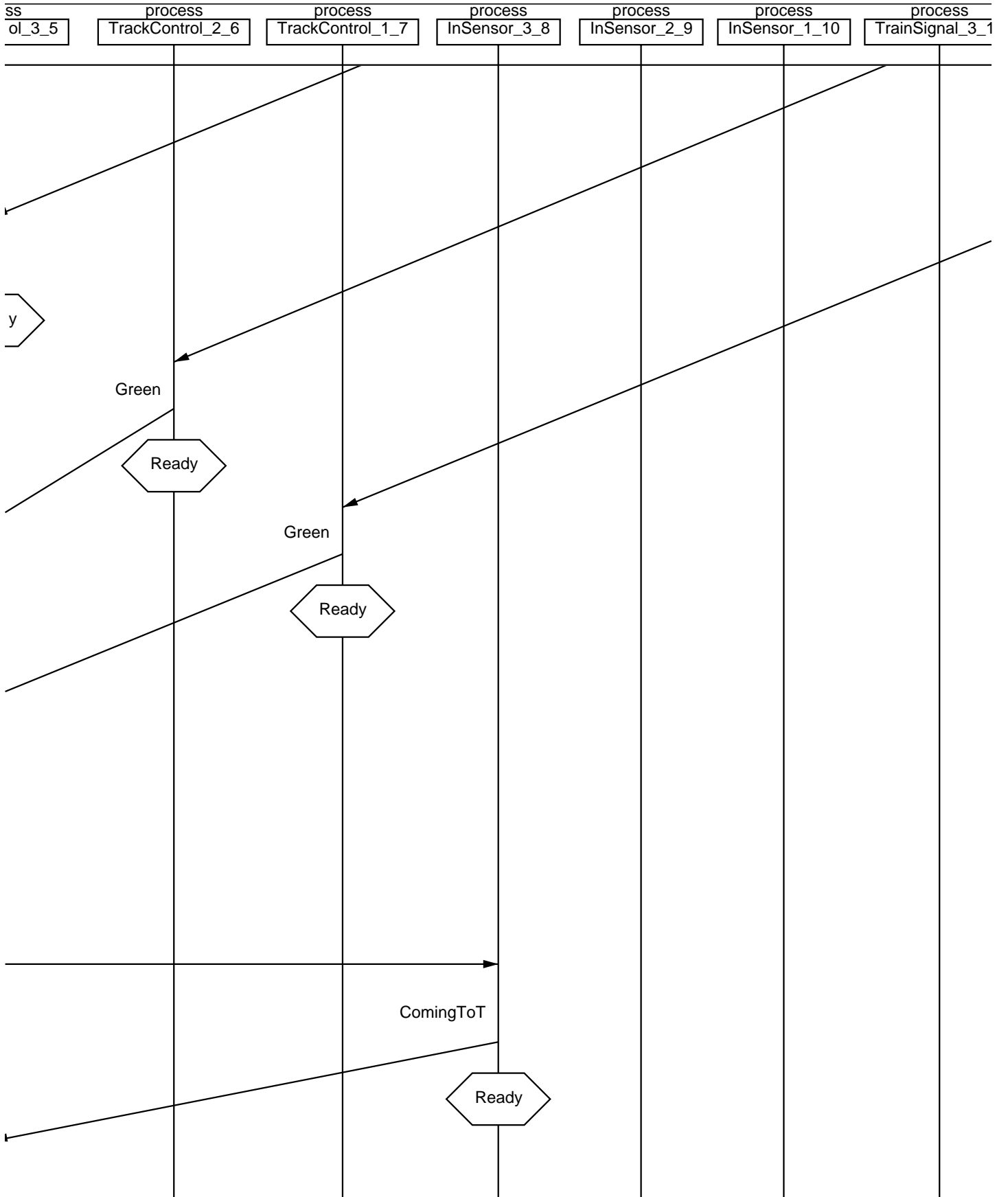


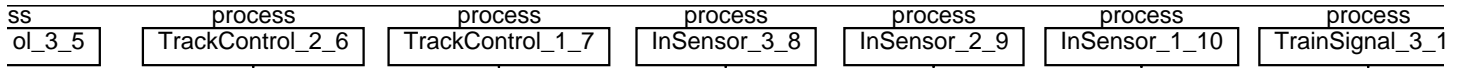


ss ol_3_5 process TrackControl_2_6 process TrackControl_1_7 process InSensor_3_8 process InSensor_2_9 process InSensor_1_10 process TrainSignal_3_1

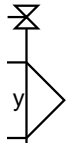




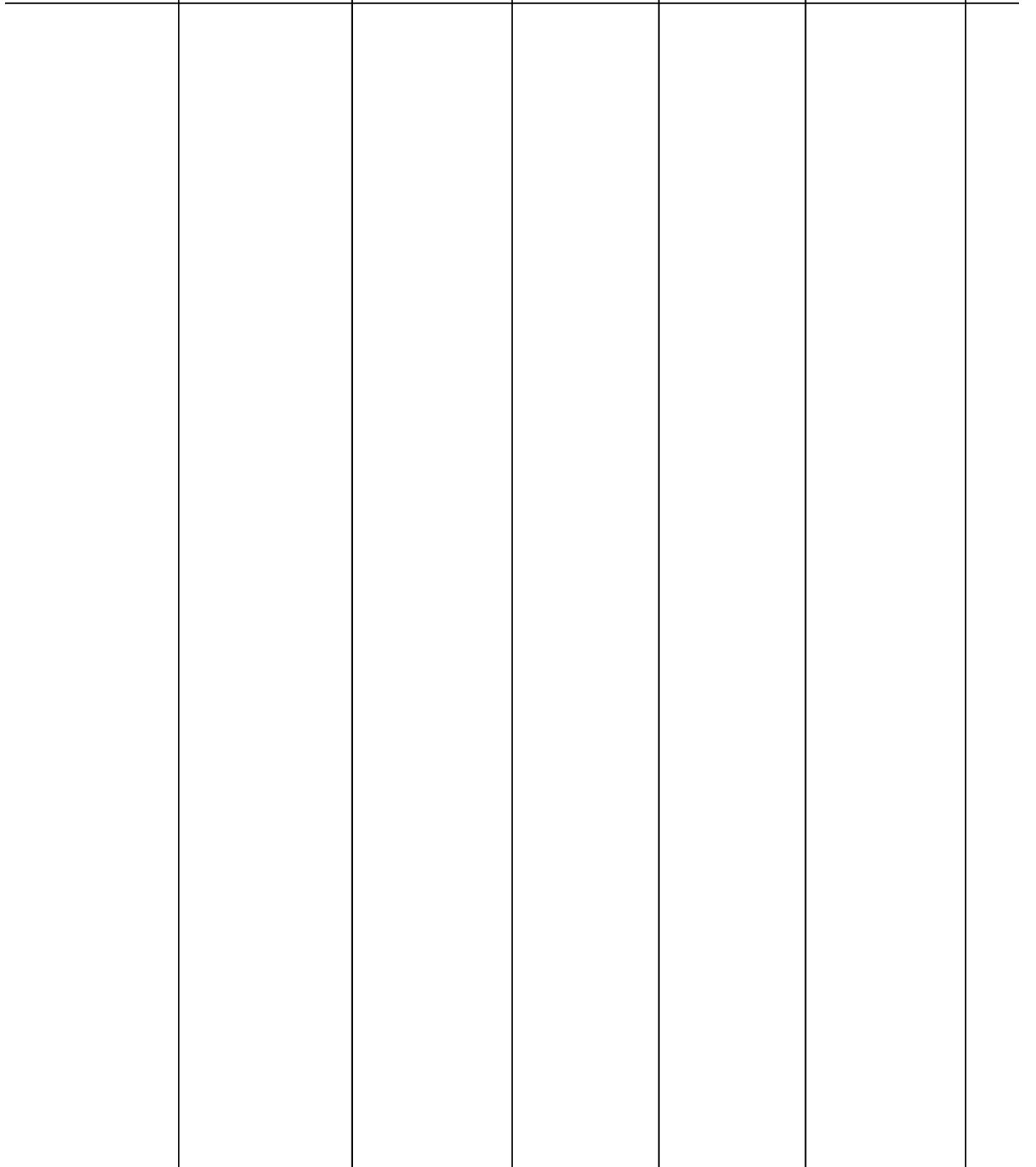




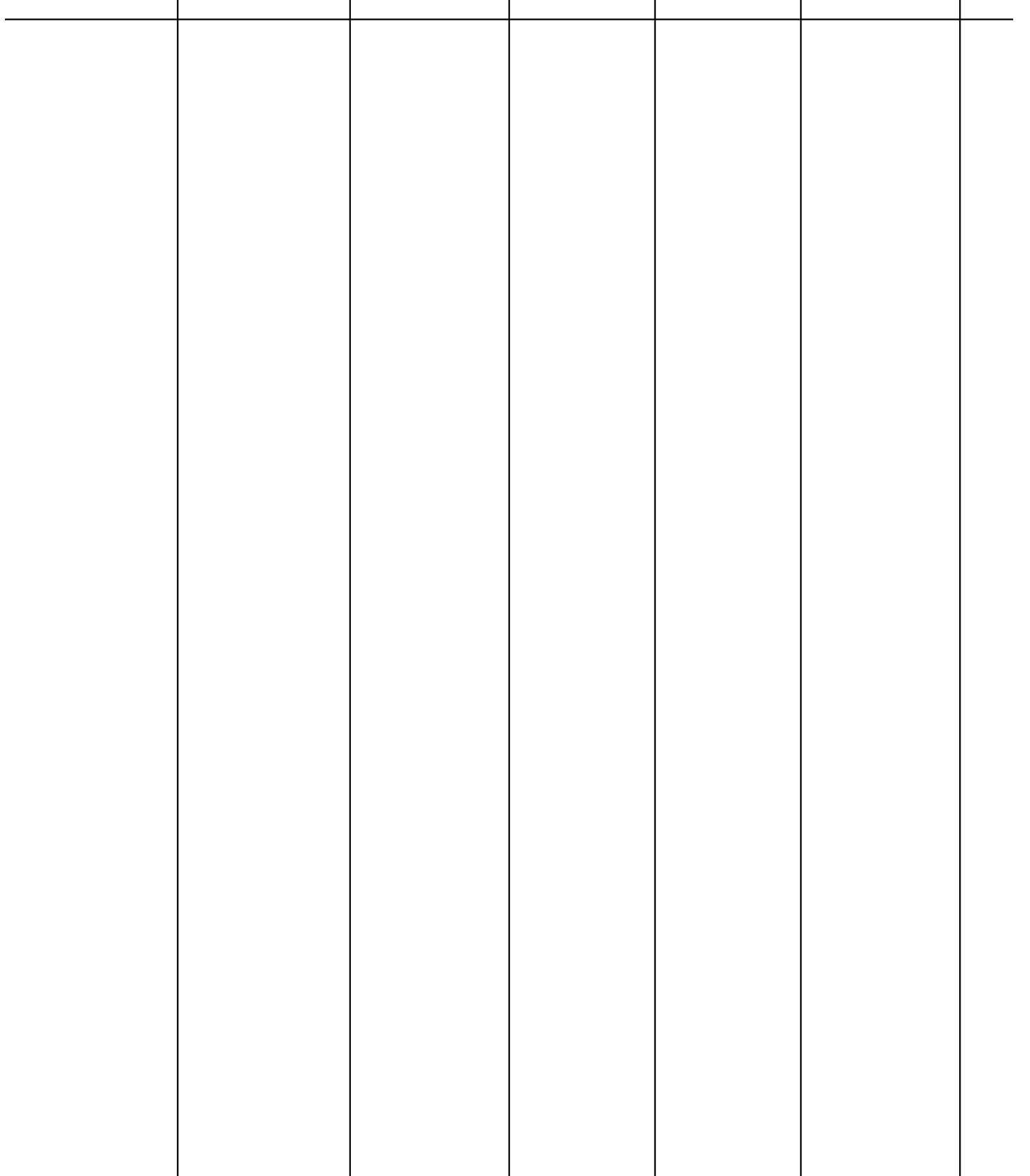
InTimer(1.0000)



ss ol_3_5	process TrackControl_2_6	process TrackControl_1_7	process InSensor_3_8	process InSensor_2_9	process InSensor_1_10	process TrainSignal_3_1
--------------	-----------------------------	-----------------------------	-------------------------	-------------------------	--------------------------	----------------------------

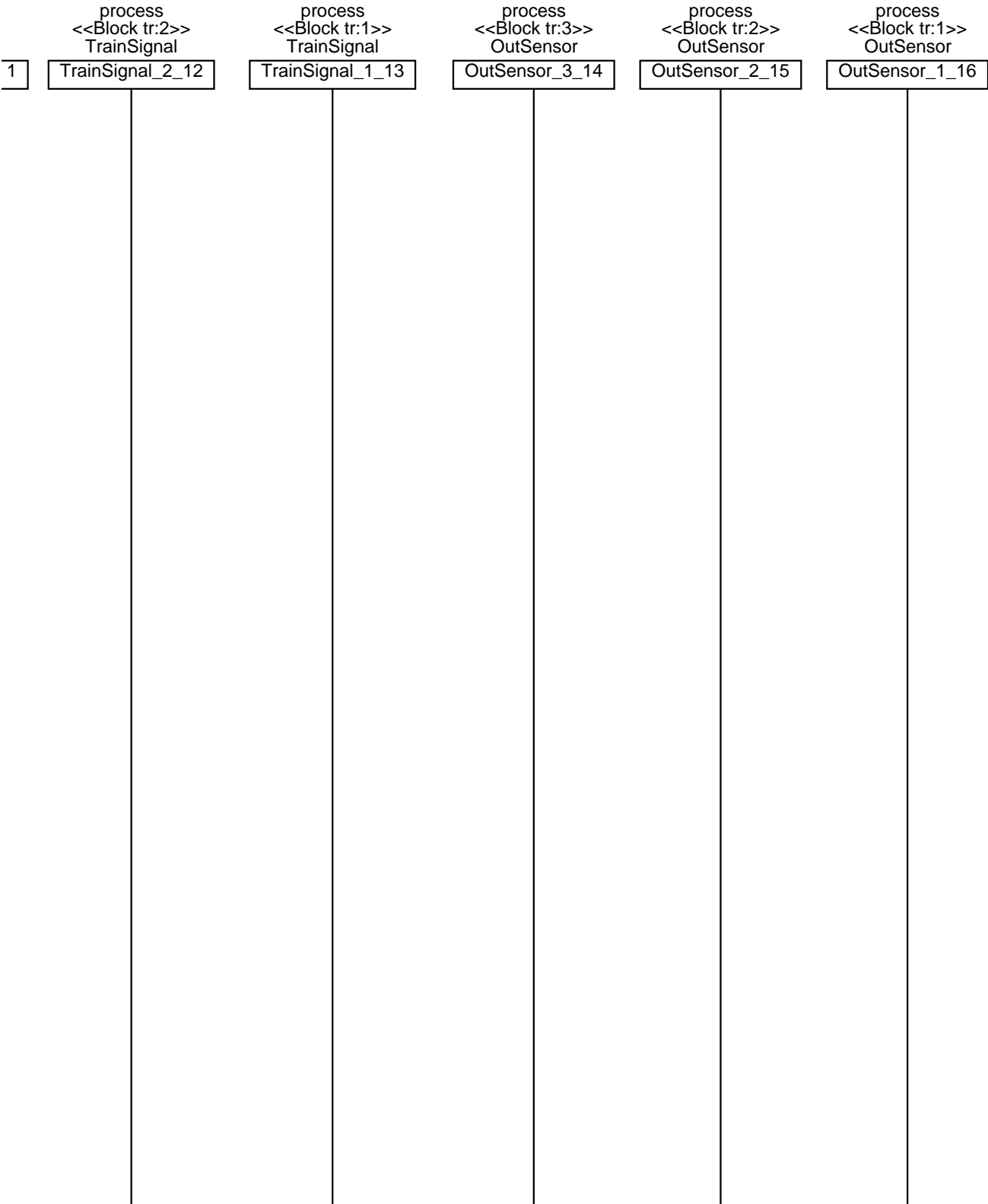


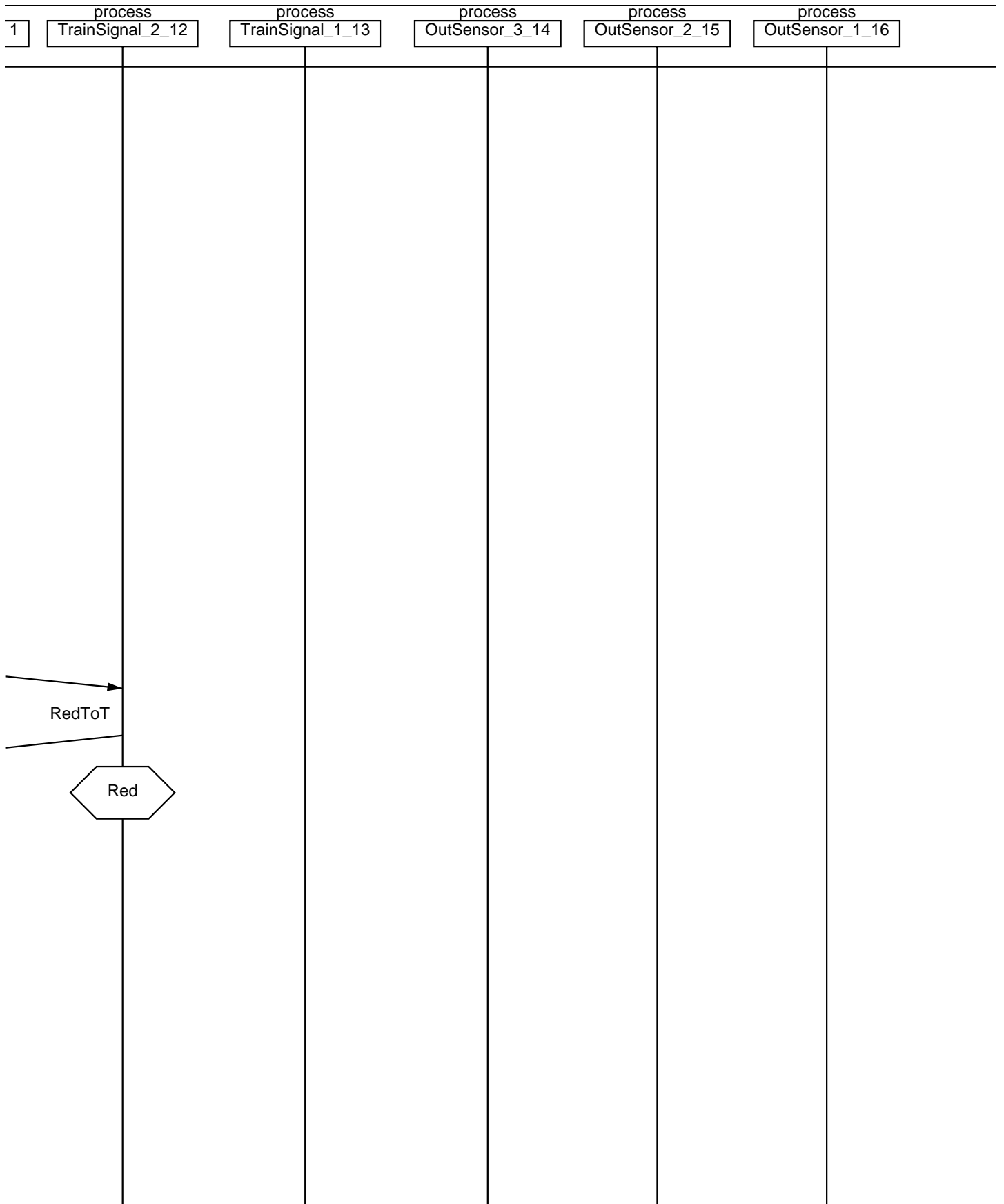
ss ol_3_5	process TrackControl_2_6	process TrackControl_1_7	process InSensor_3_8	process InSensor_2_9	process InSensor_1_10	process TrainSignal_3_1
--------------	-----------------------------	-----------------------------	-------------------------	-------------------------	--------------------------	----------------------------



ss	process	process	process	process	process	process
ol_3_5	TrackControl_2_6	TrackControl_1_7	InSensor_3_8	InSensor_2_9	InSensor_1_10	TrainSignal_3_1

--	--	--	--	--	--	--





process process process process process

1

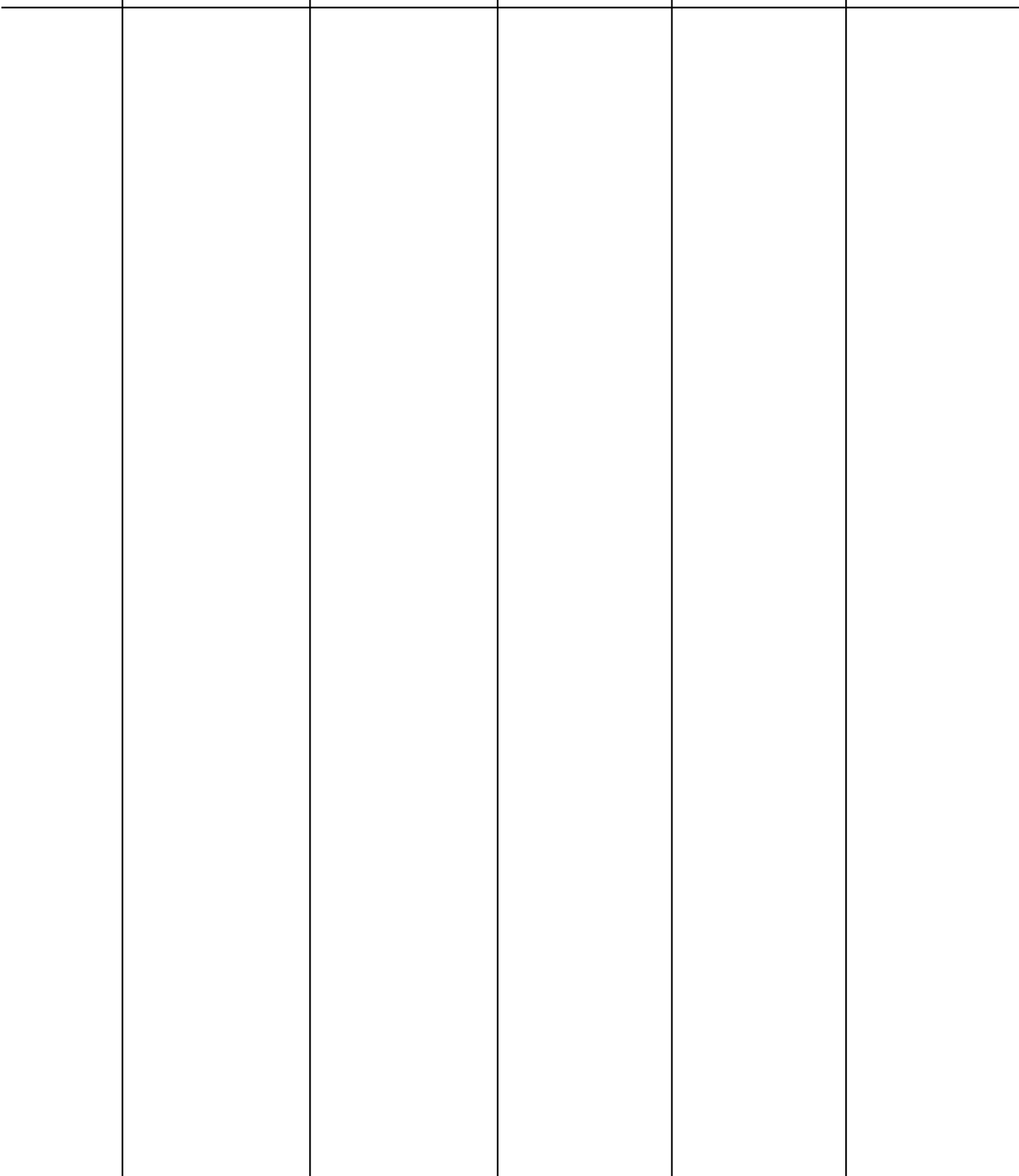
TrainSignal_2_12

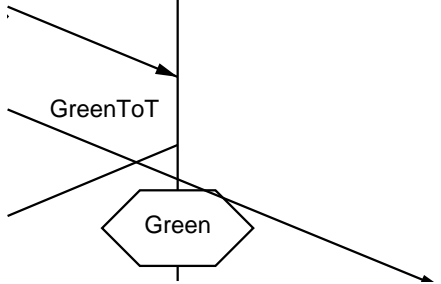
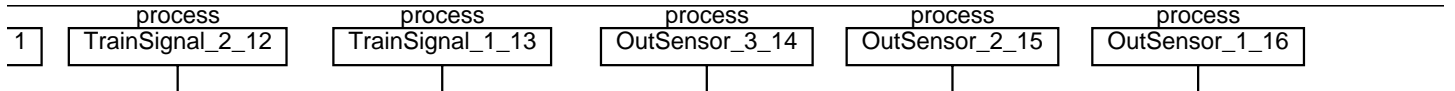
TrainSignal_1_13

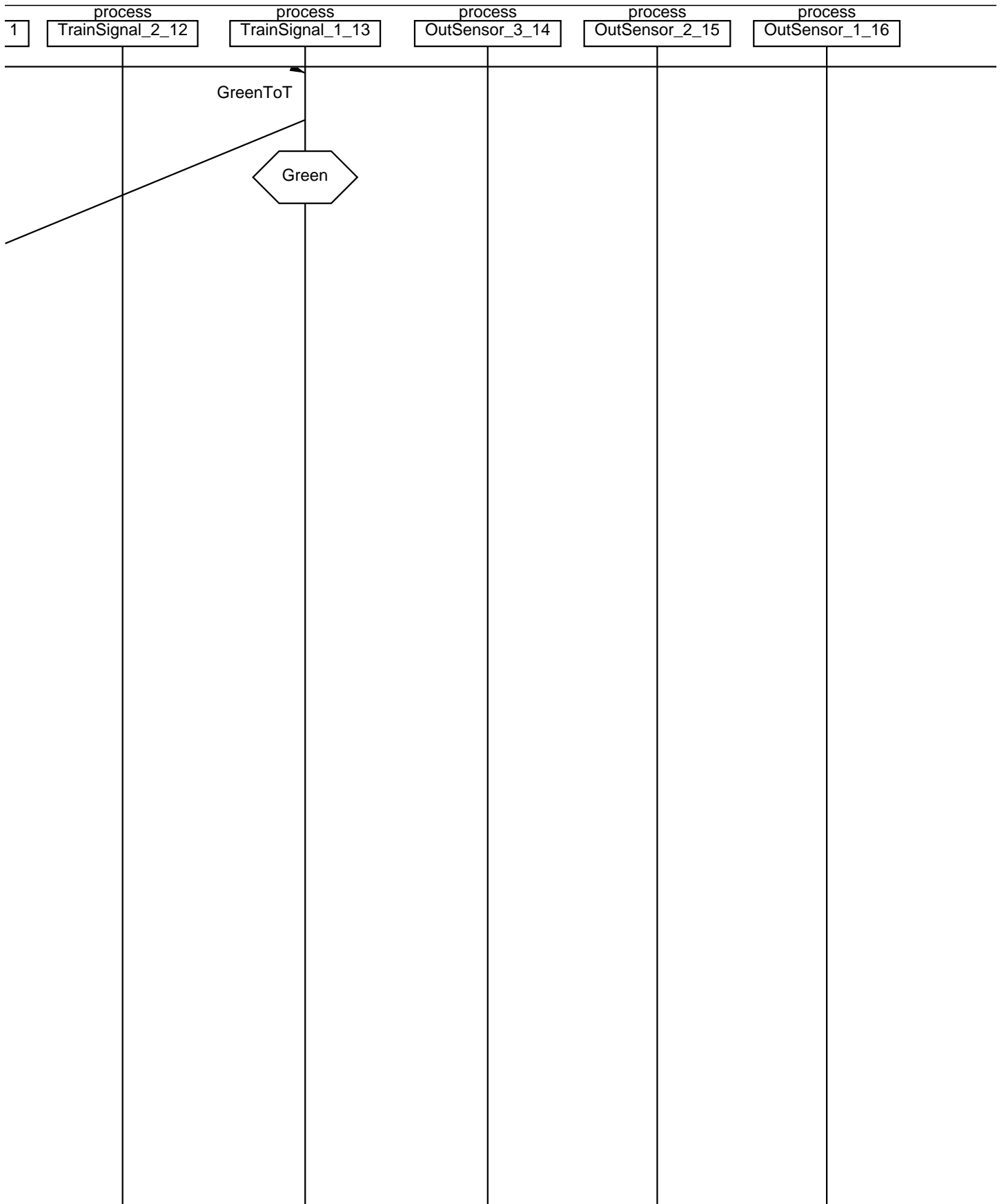
OutSensor_3_14

OutSensor_2_15

OutSensor_1_16







process process process process process

1

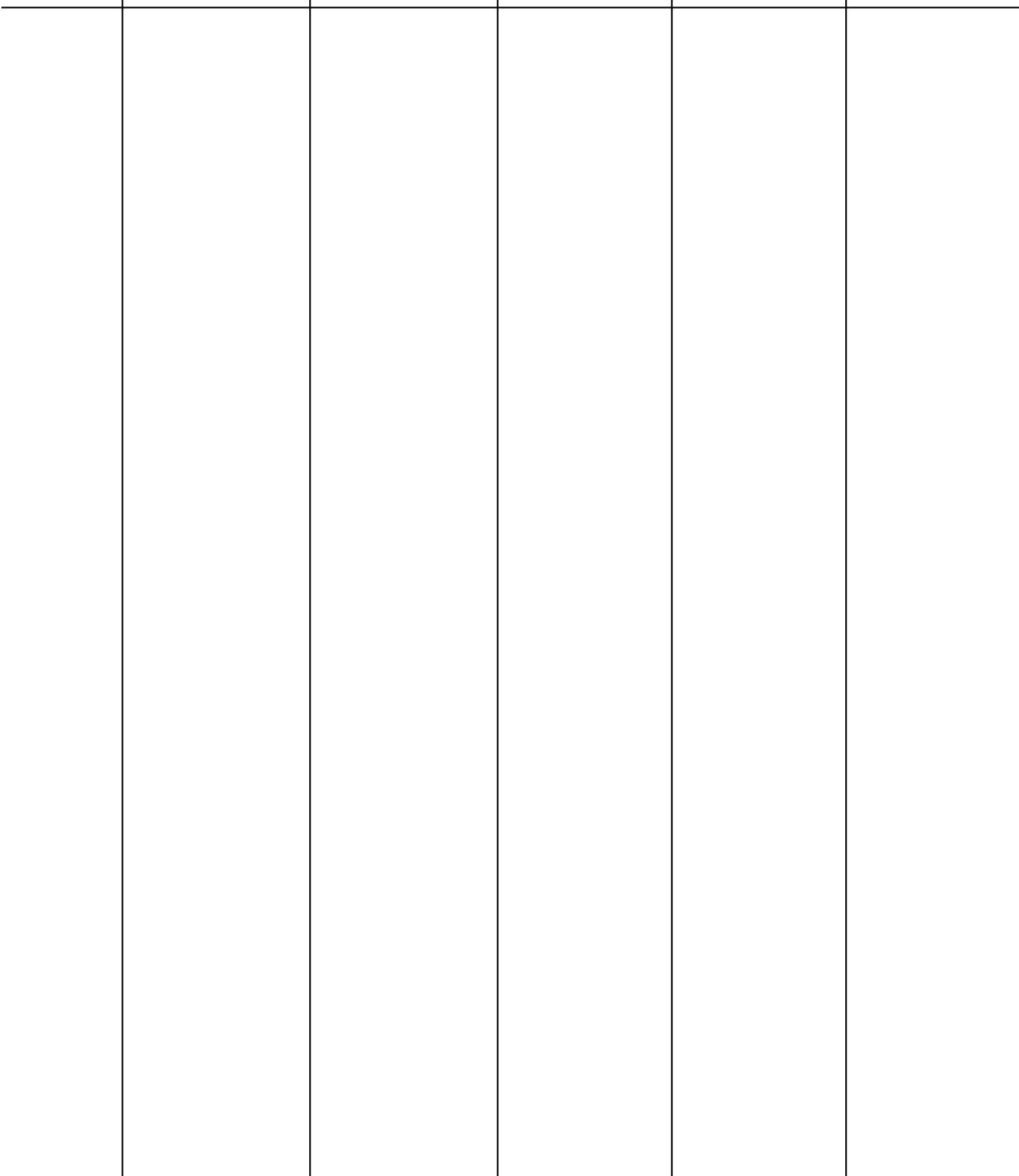
TrainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16



process process process process process

1

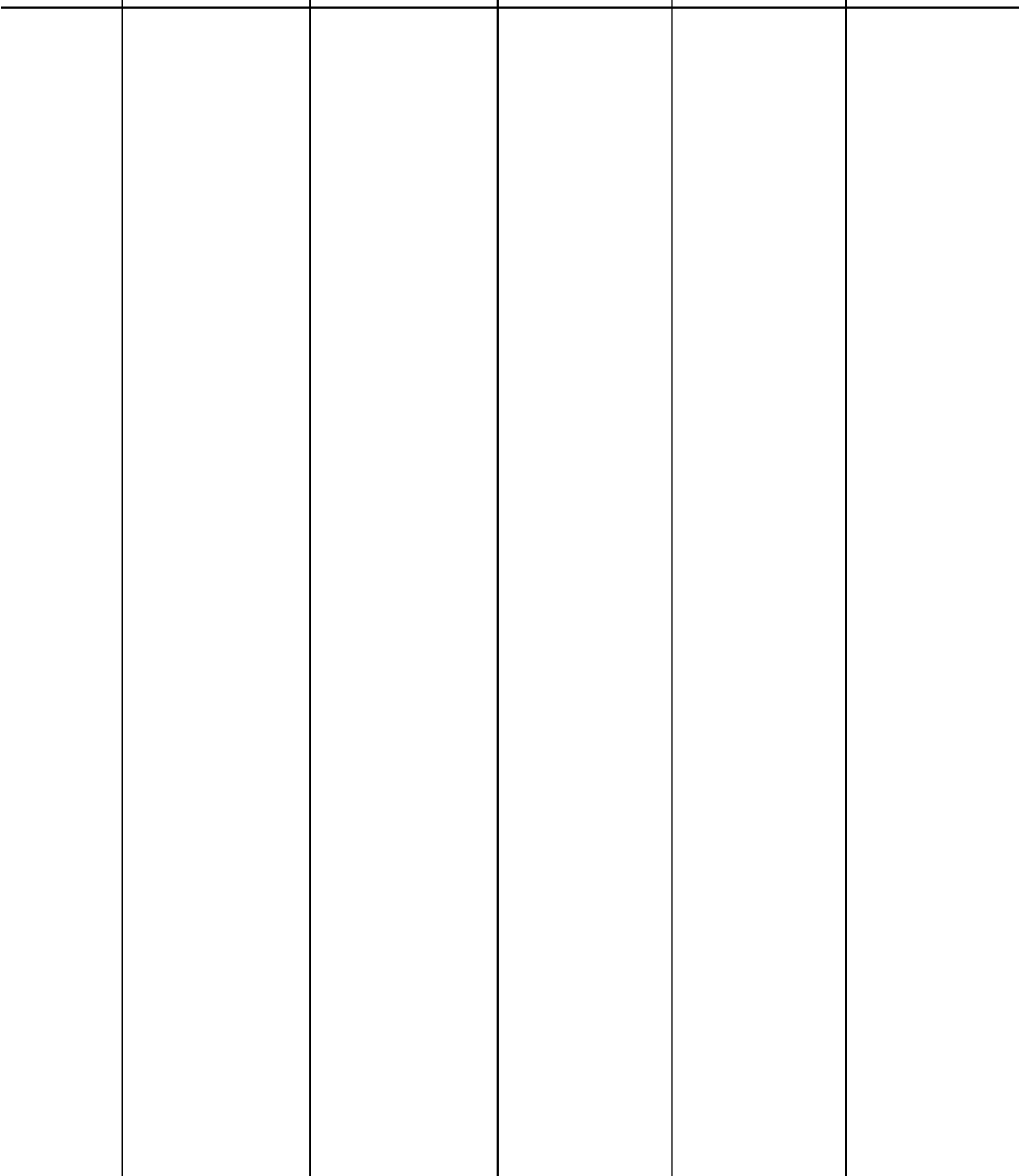
TrainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16



process process process process process

1

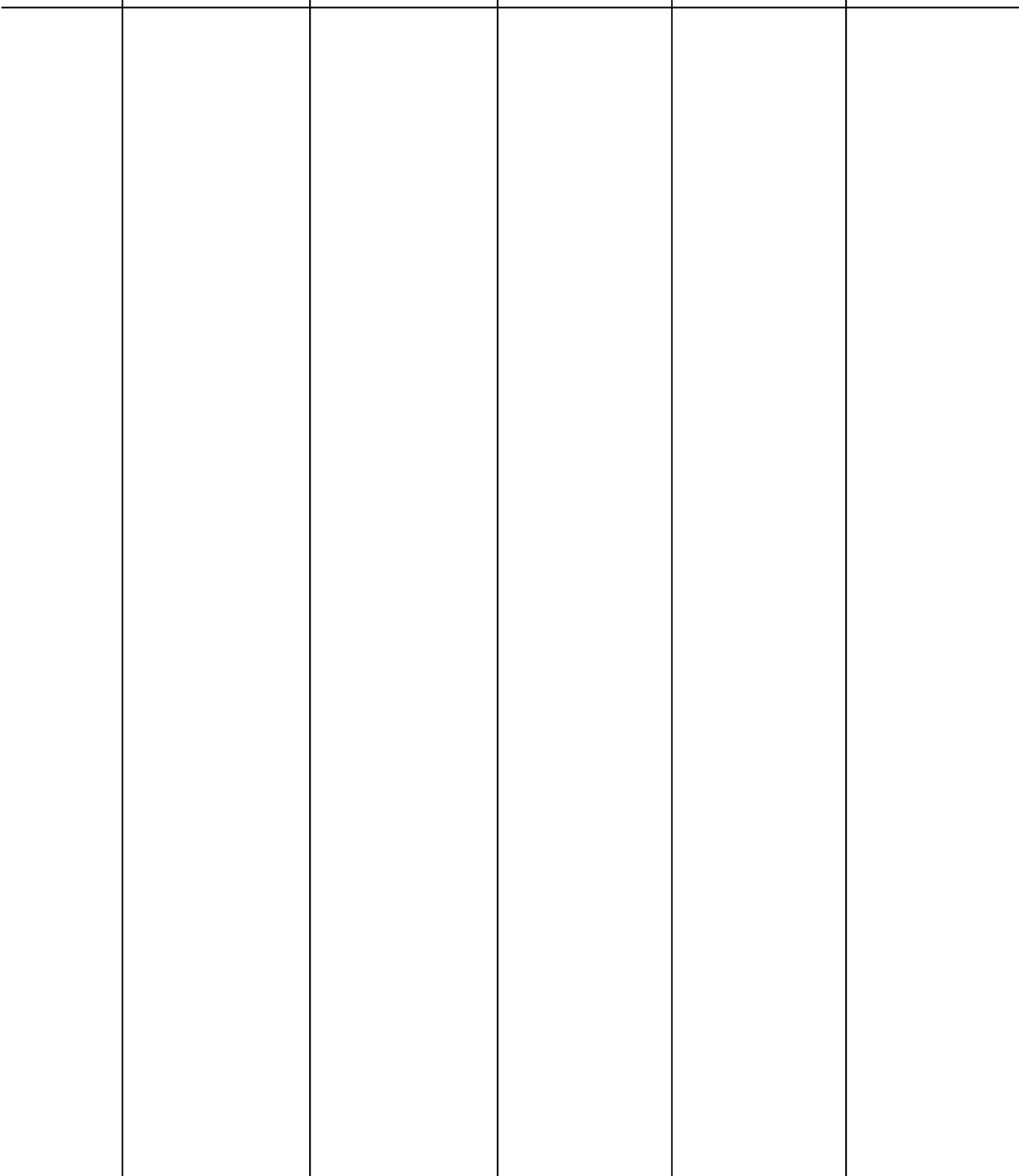
TrainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

OutSensor_1_16



process process process process process

1

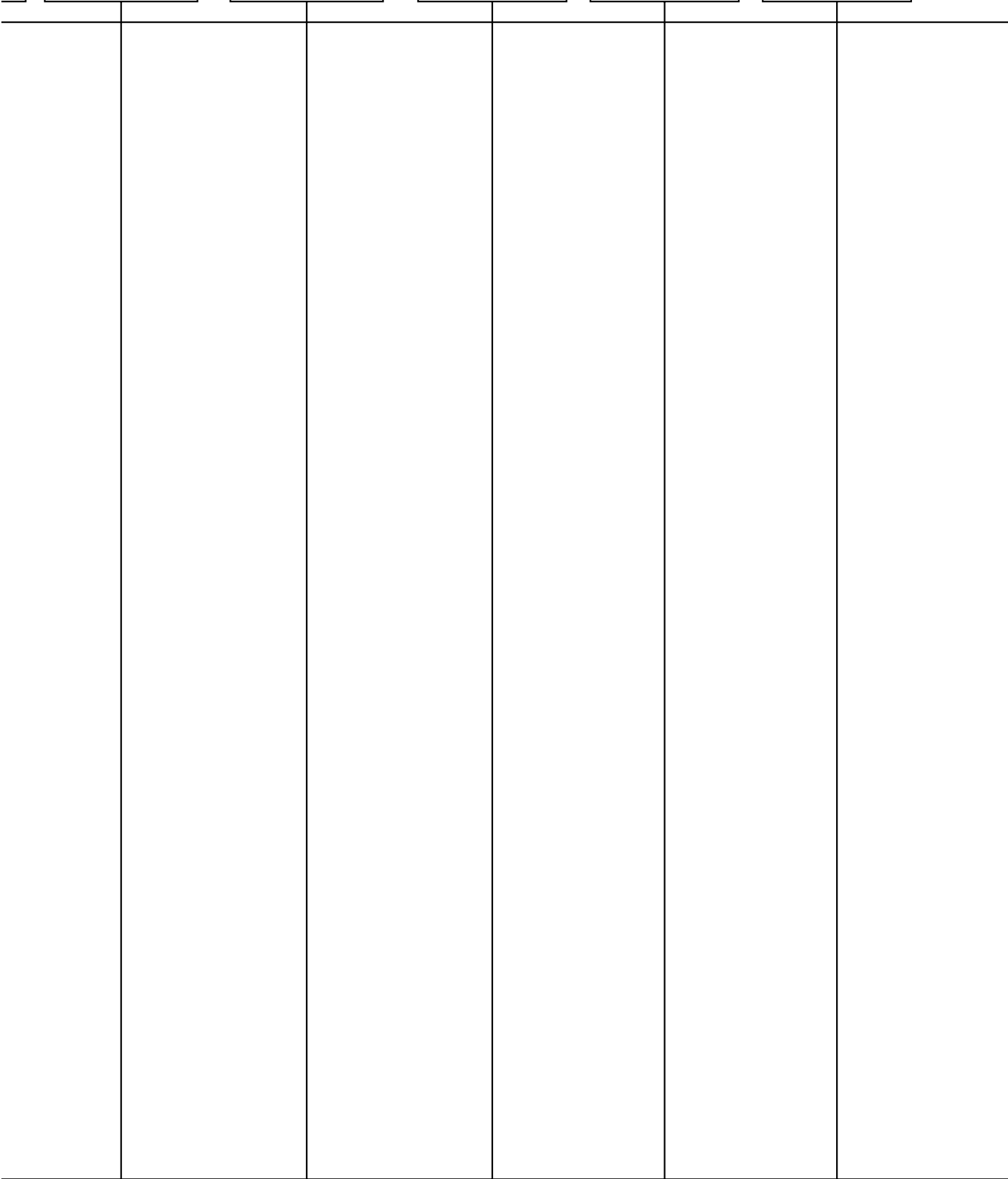
TrainSignal_2_12

TrainSignal_1_13

OutSensor_3_14

OutSensor_2_15

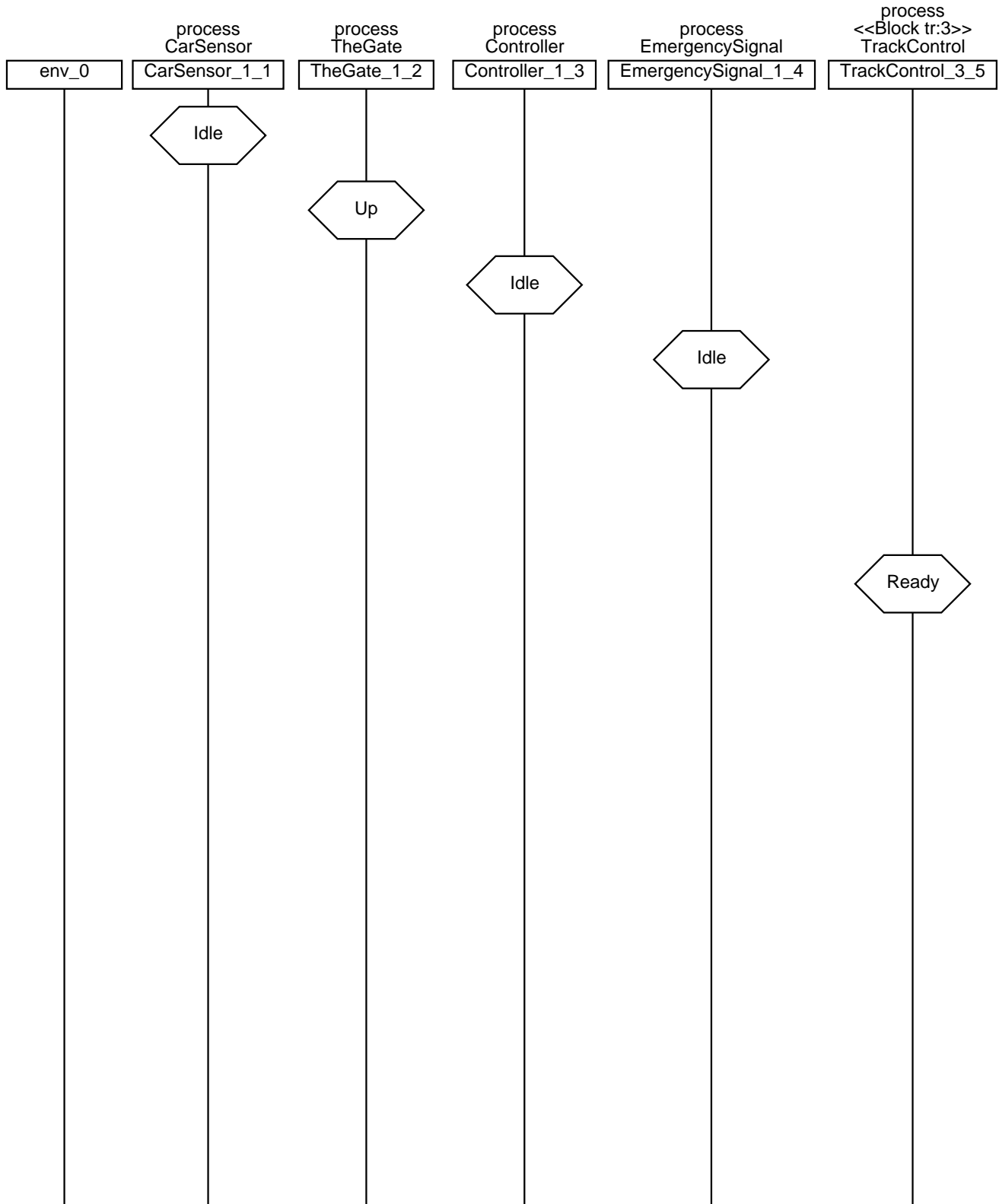
OutSensor_1_16

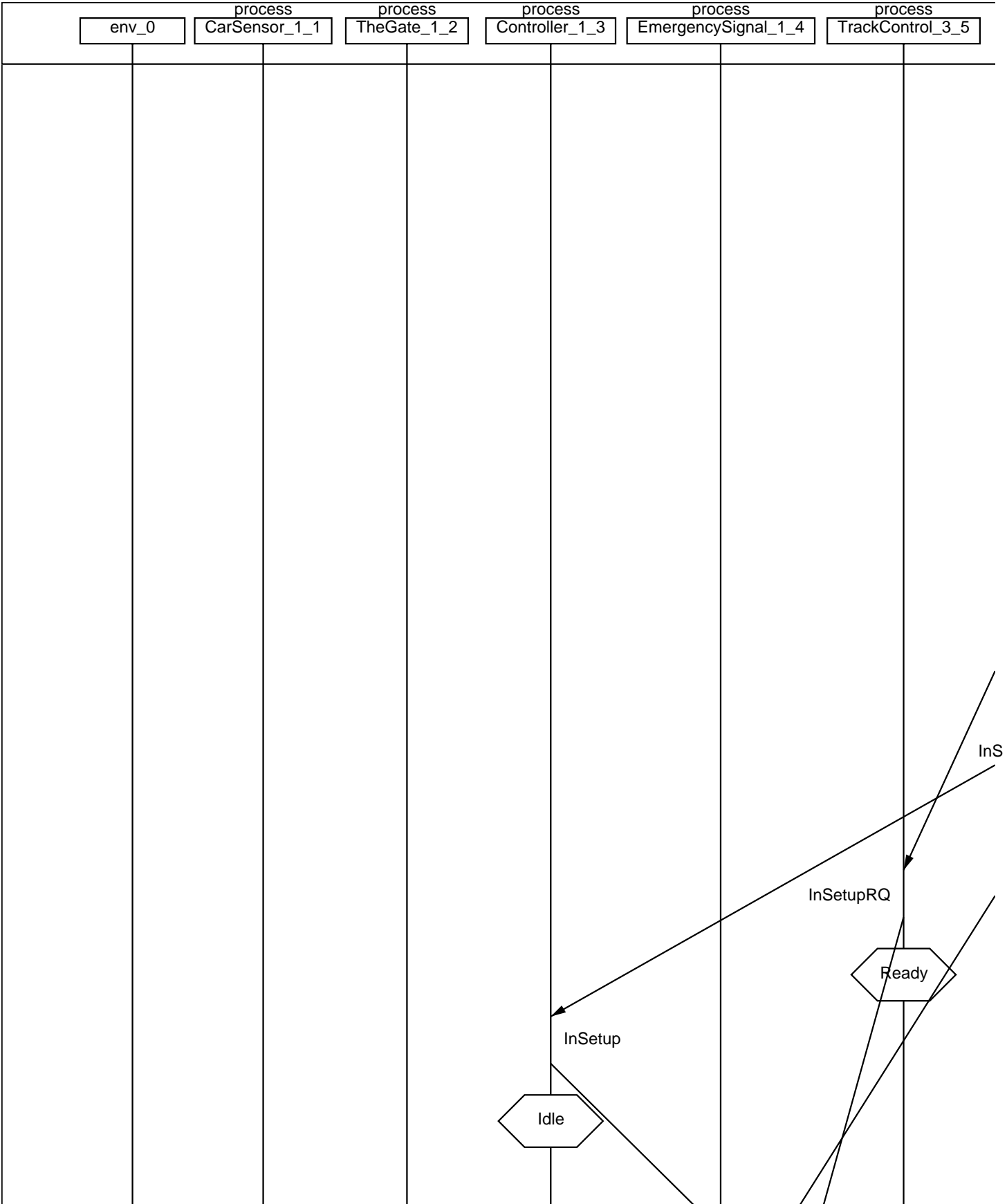


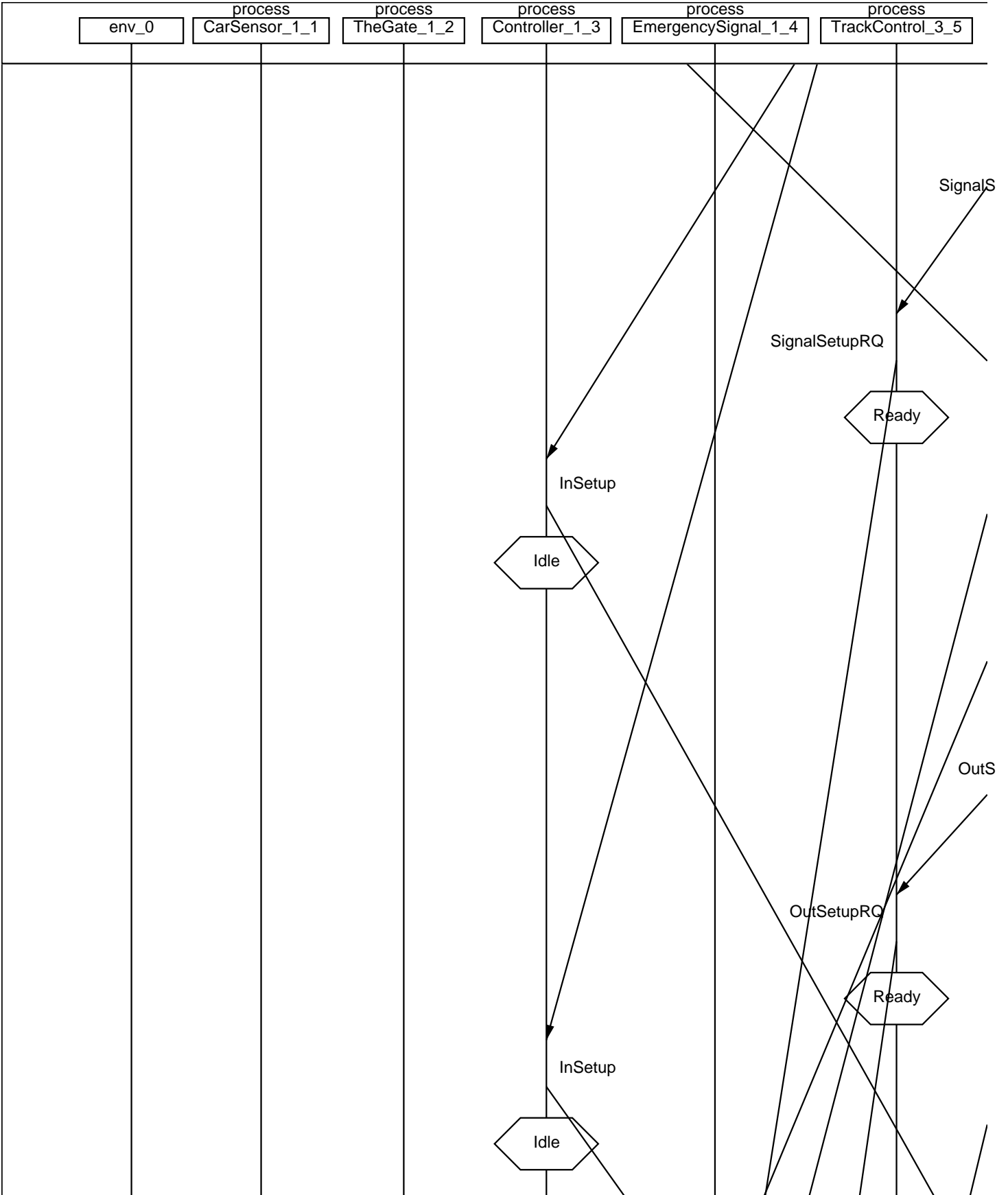
--

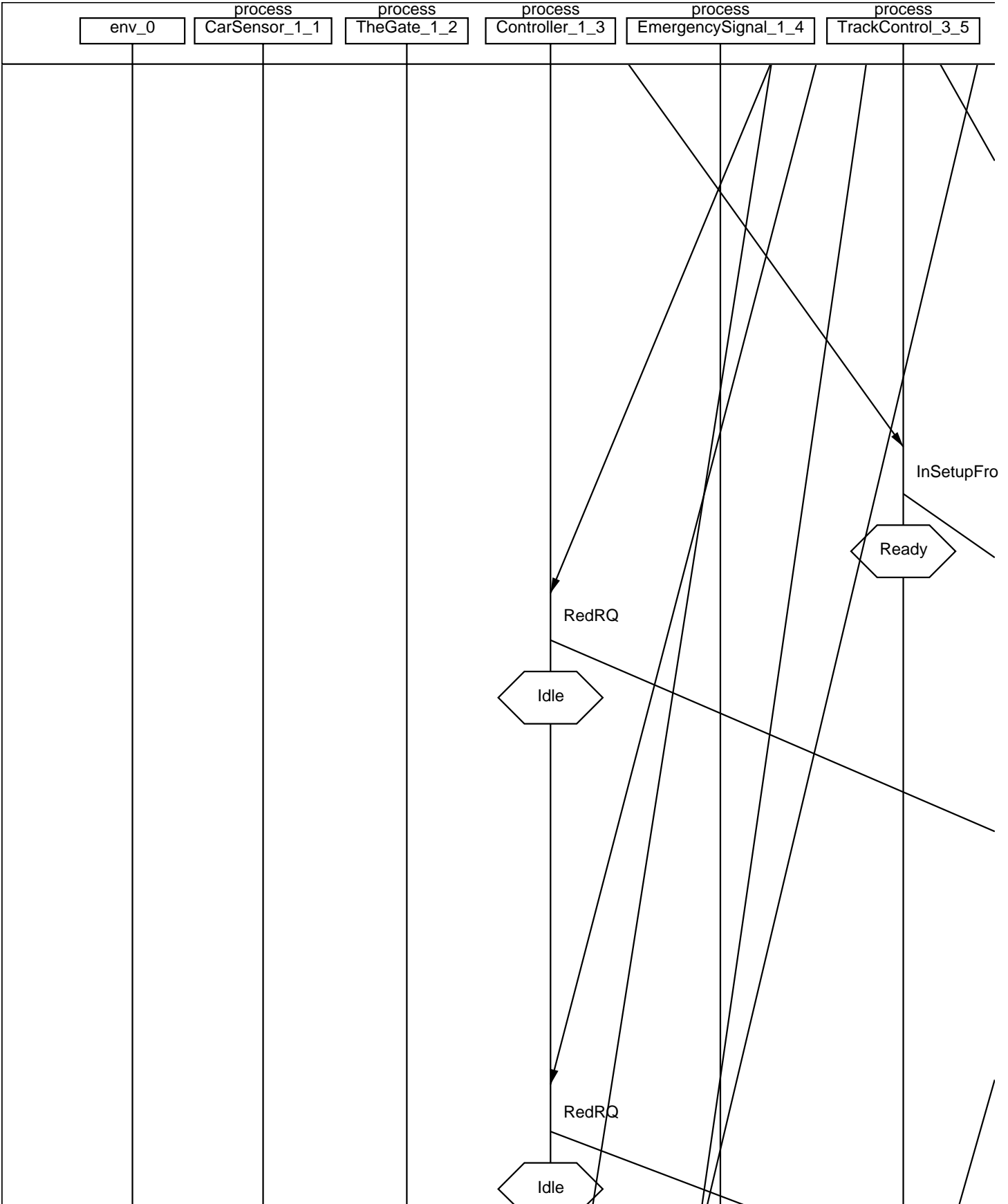
MSC CompleteMSC_TestCaseF_Strategy3

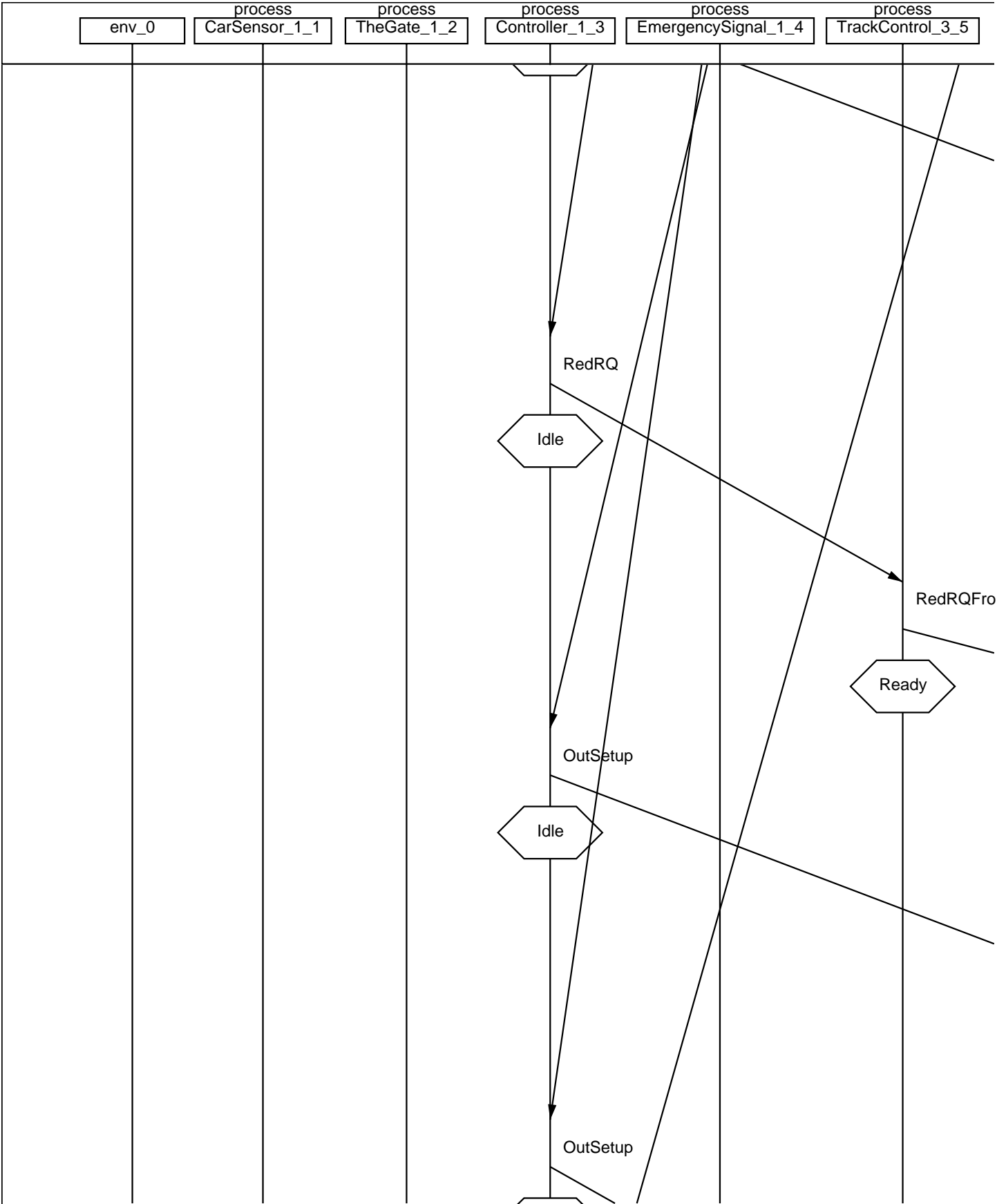
Simulation trace
generated by
SDL Simulator 4.3

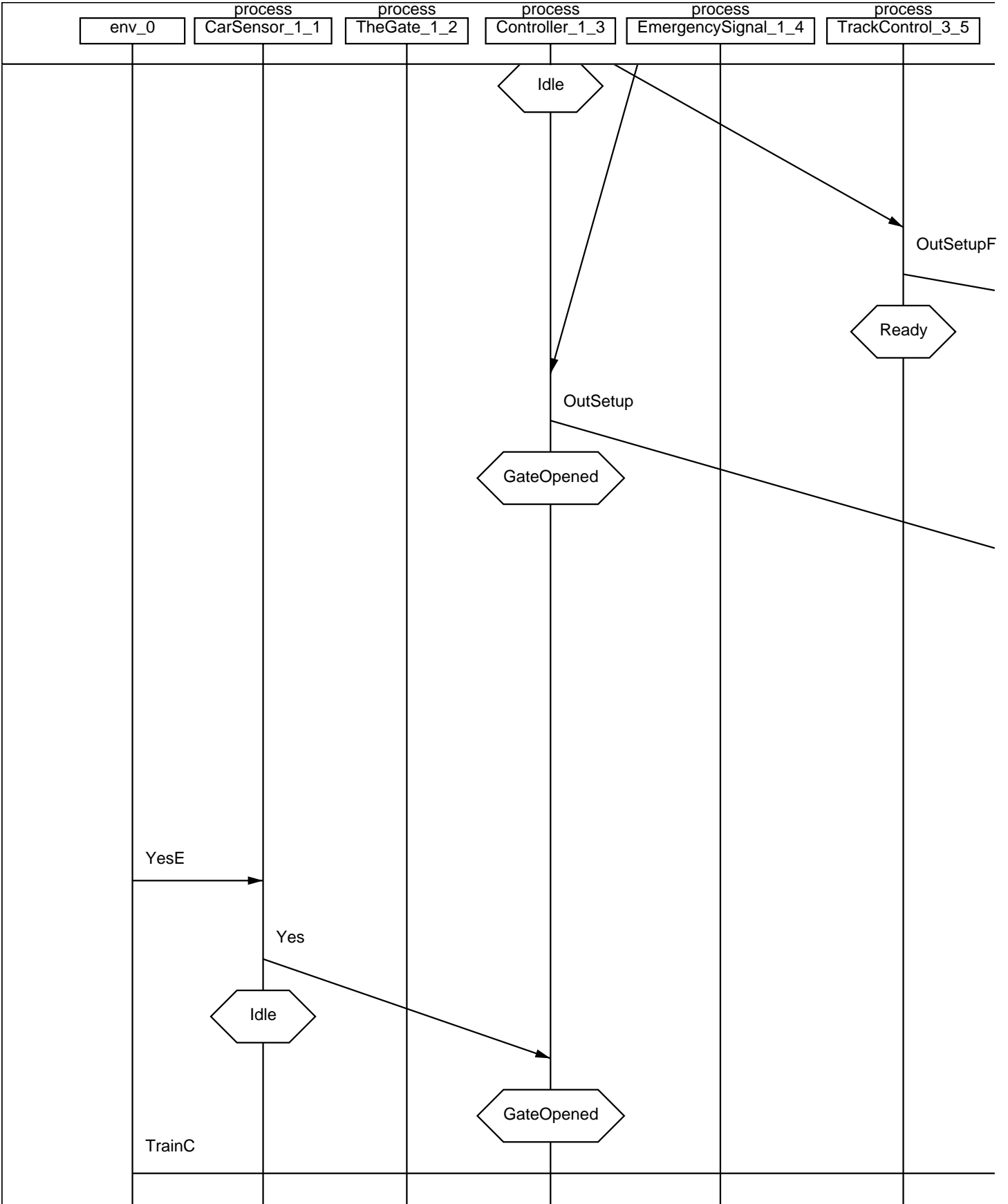


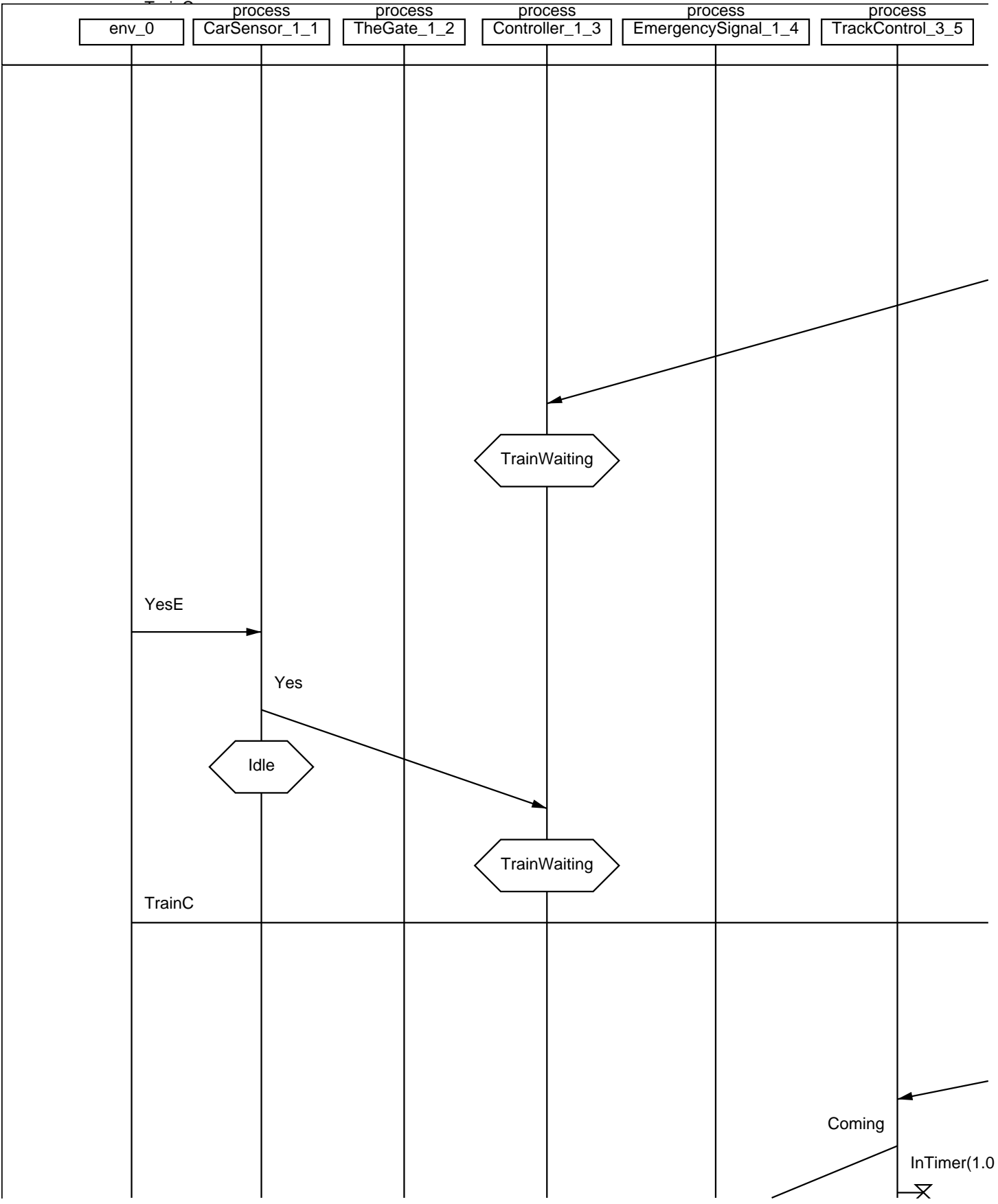


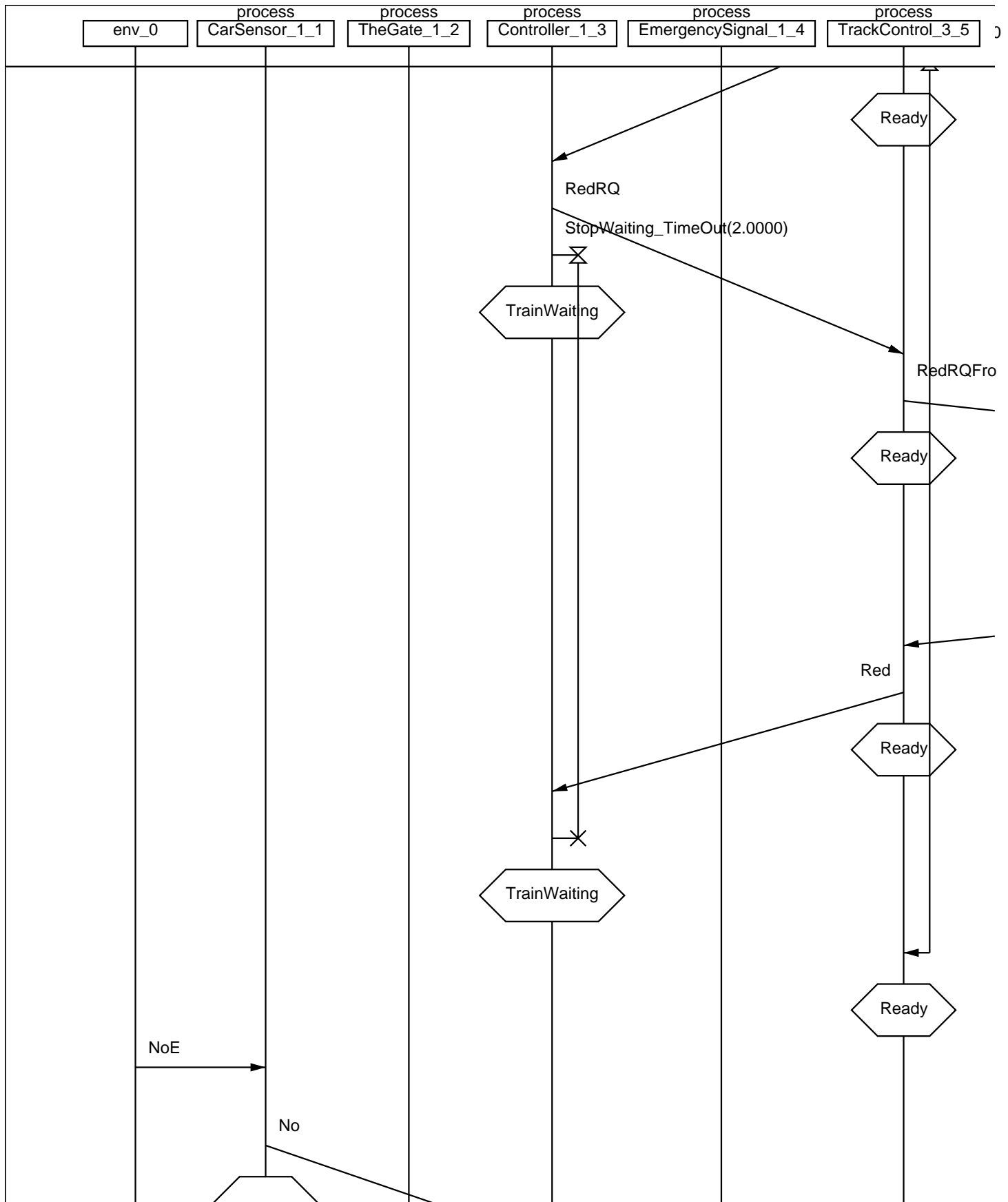


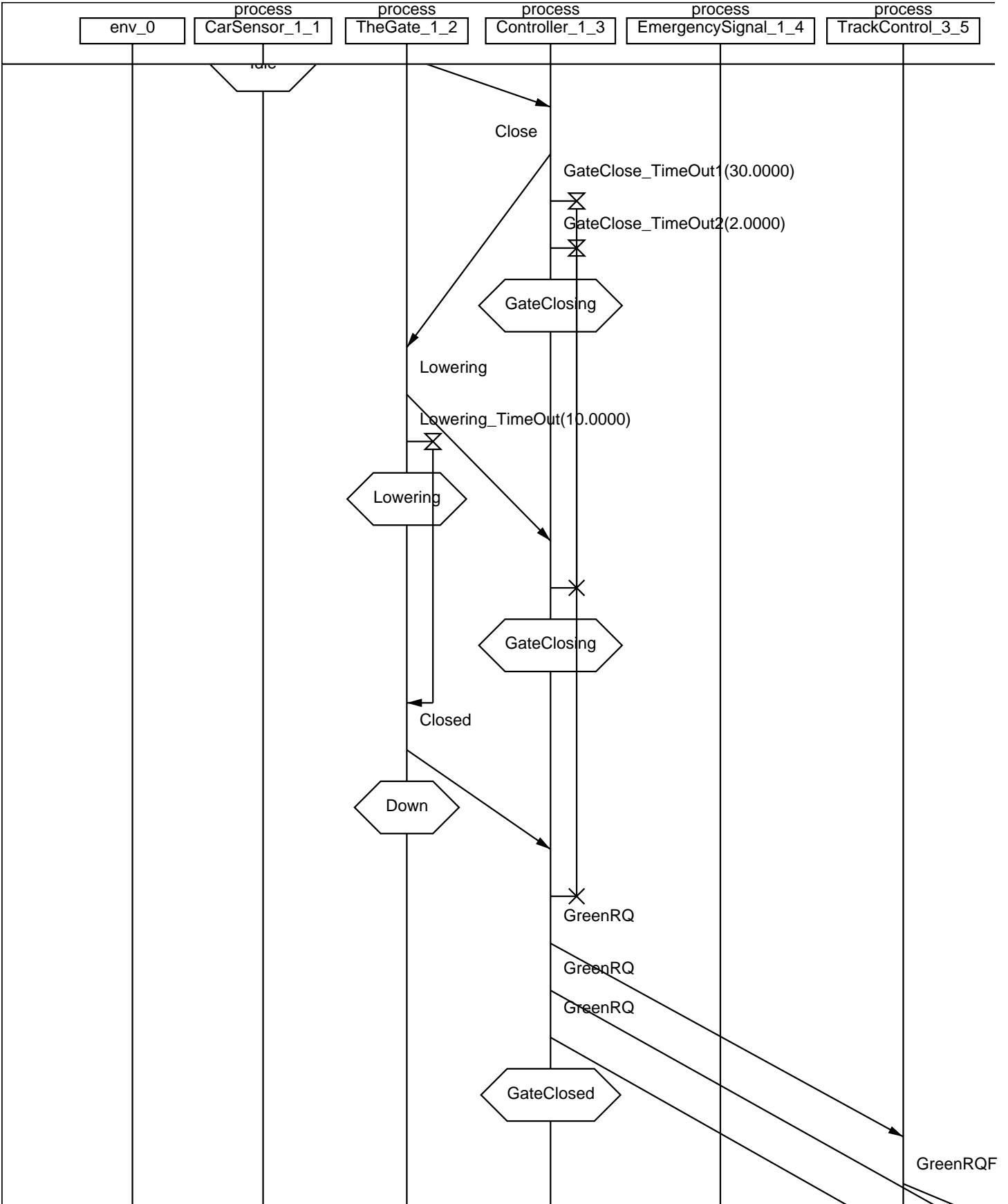


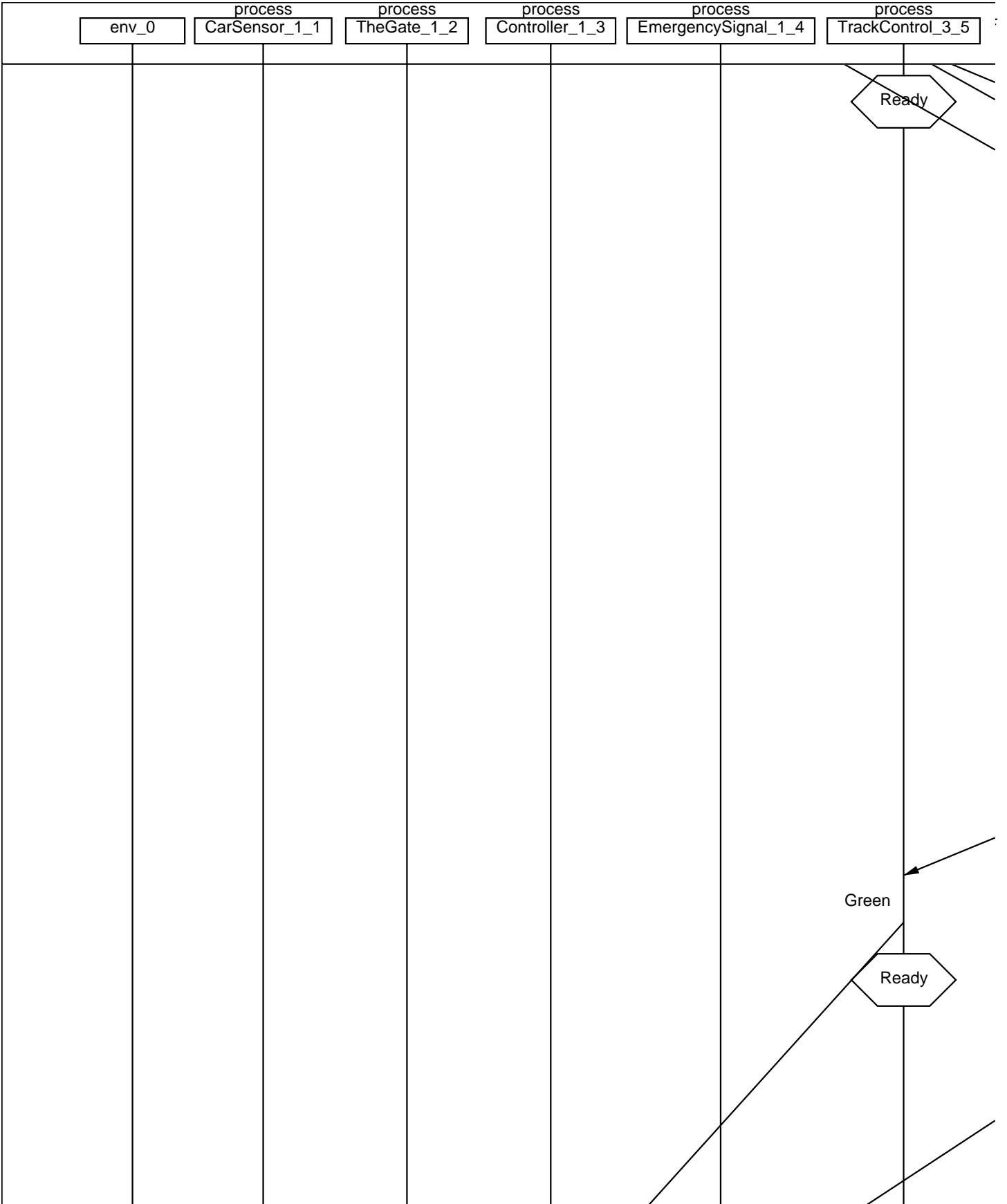


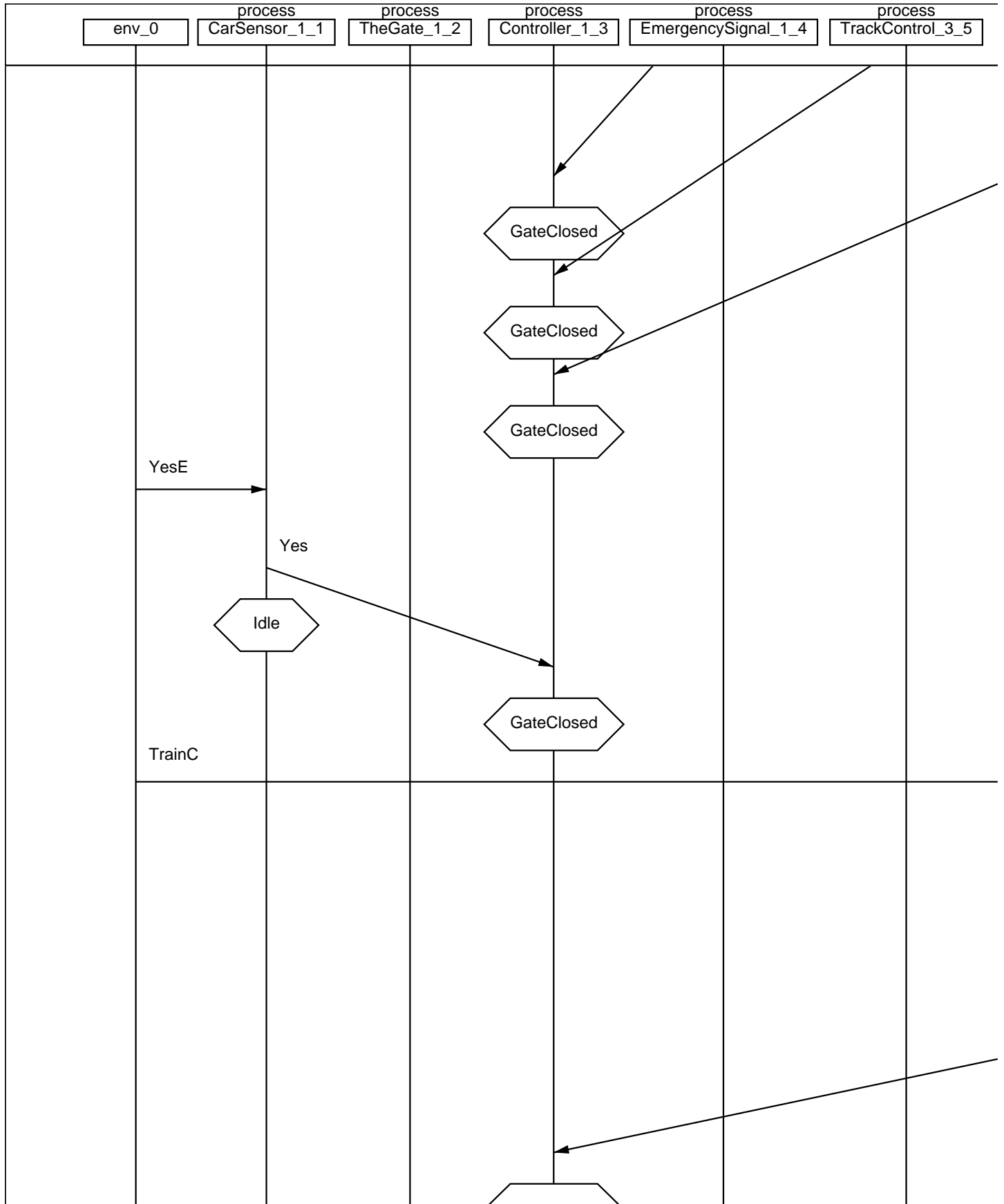


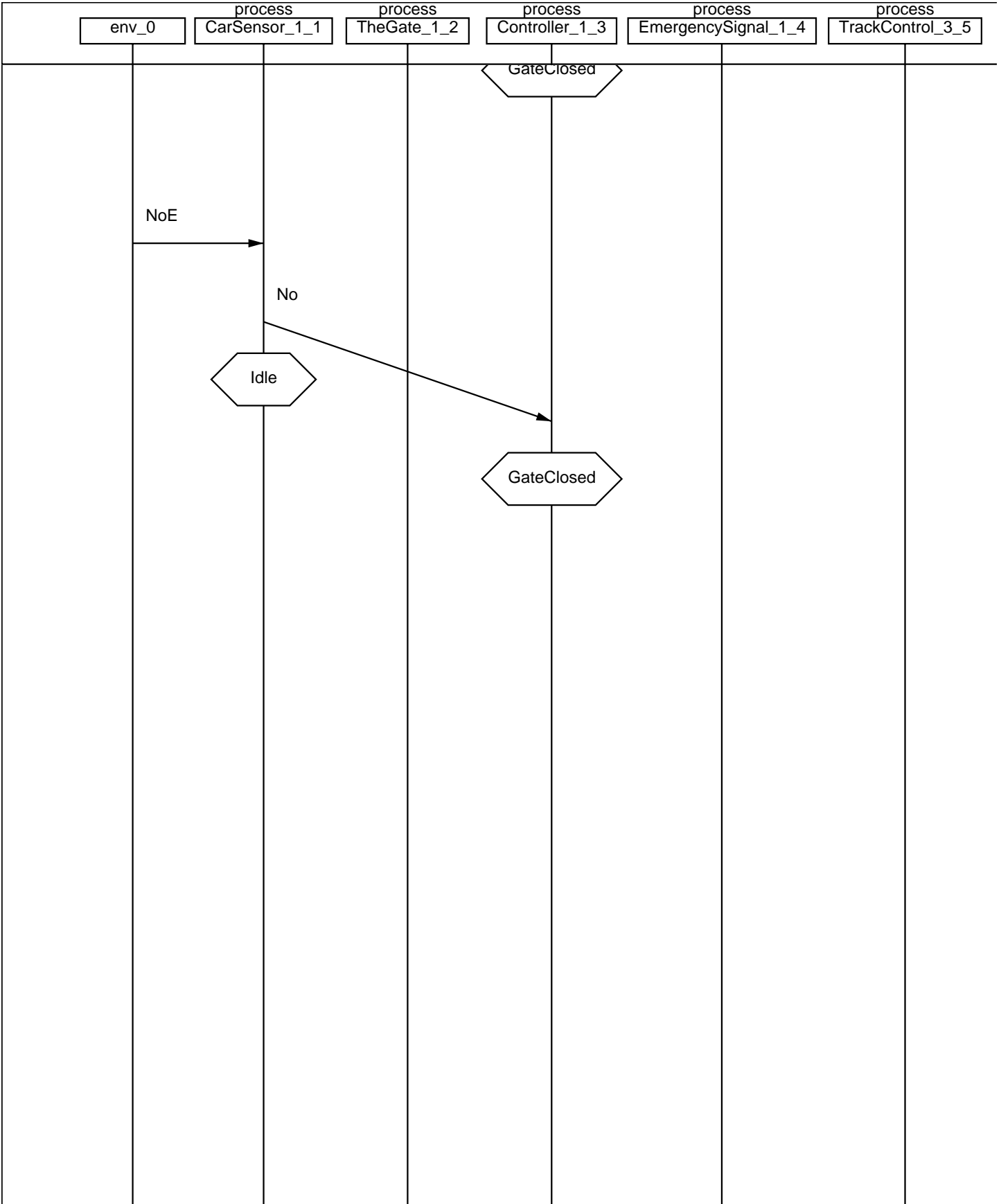


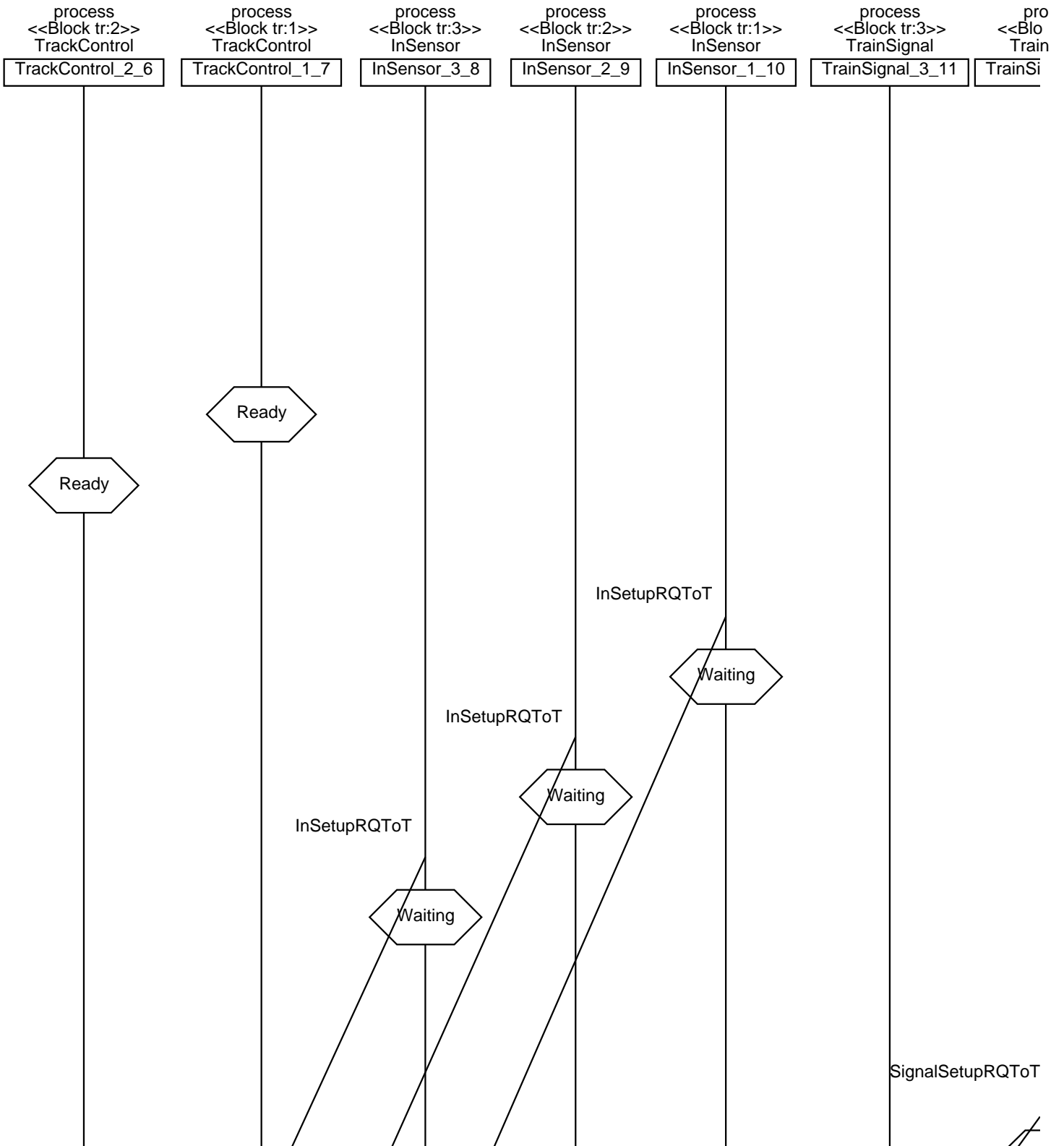


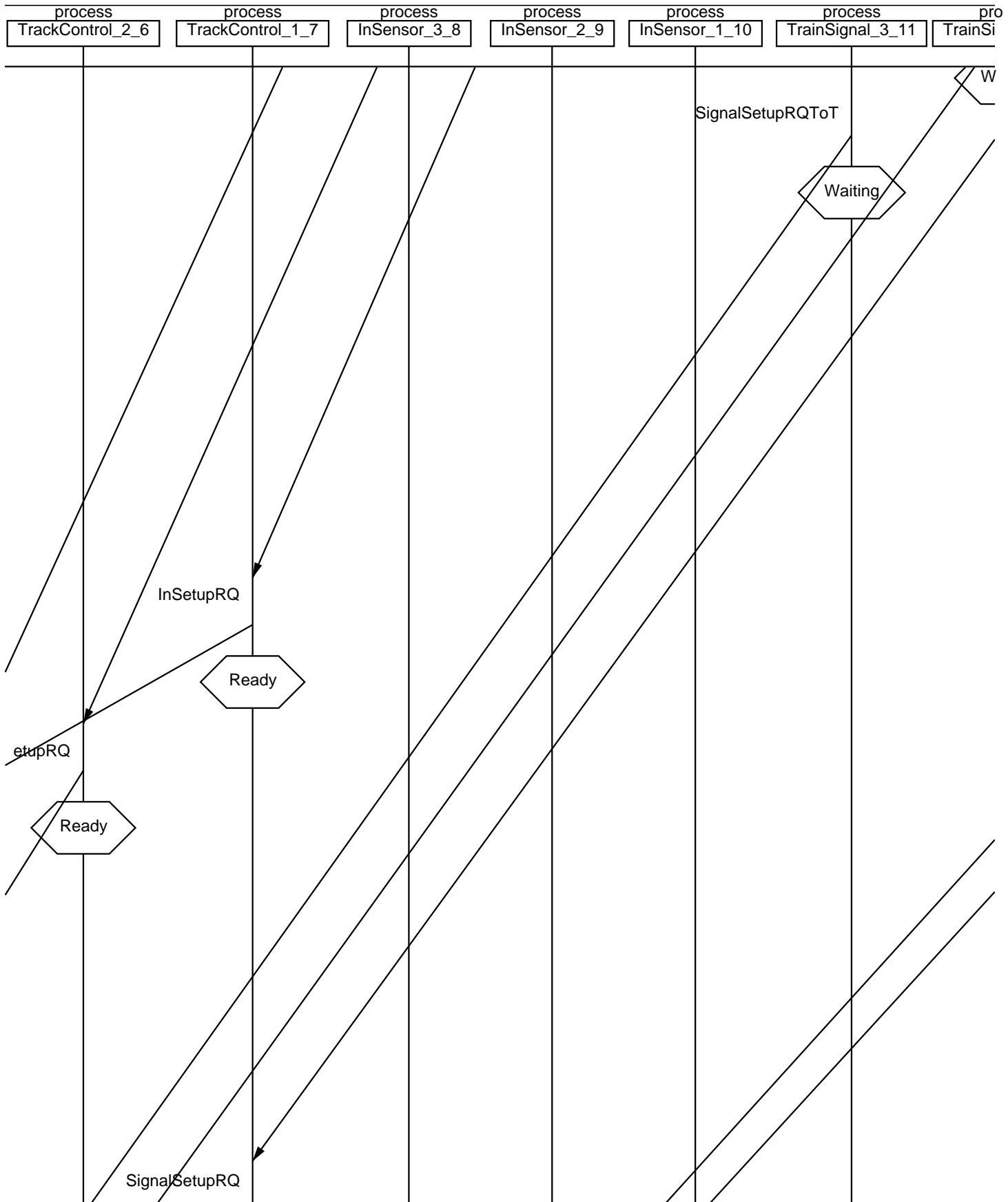


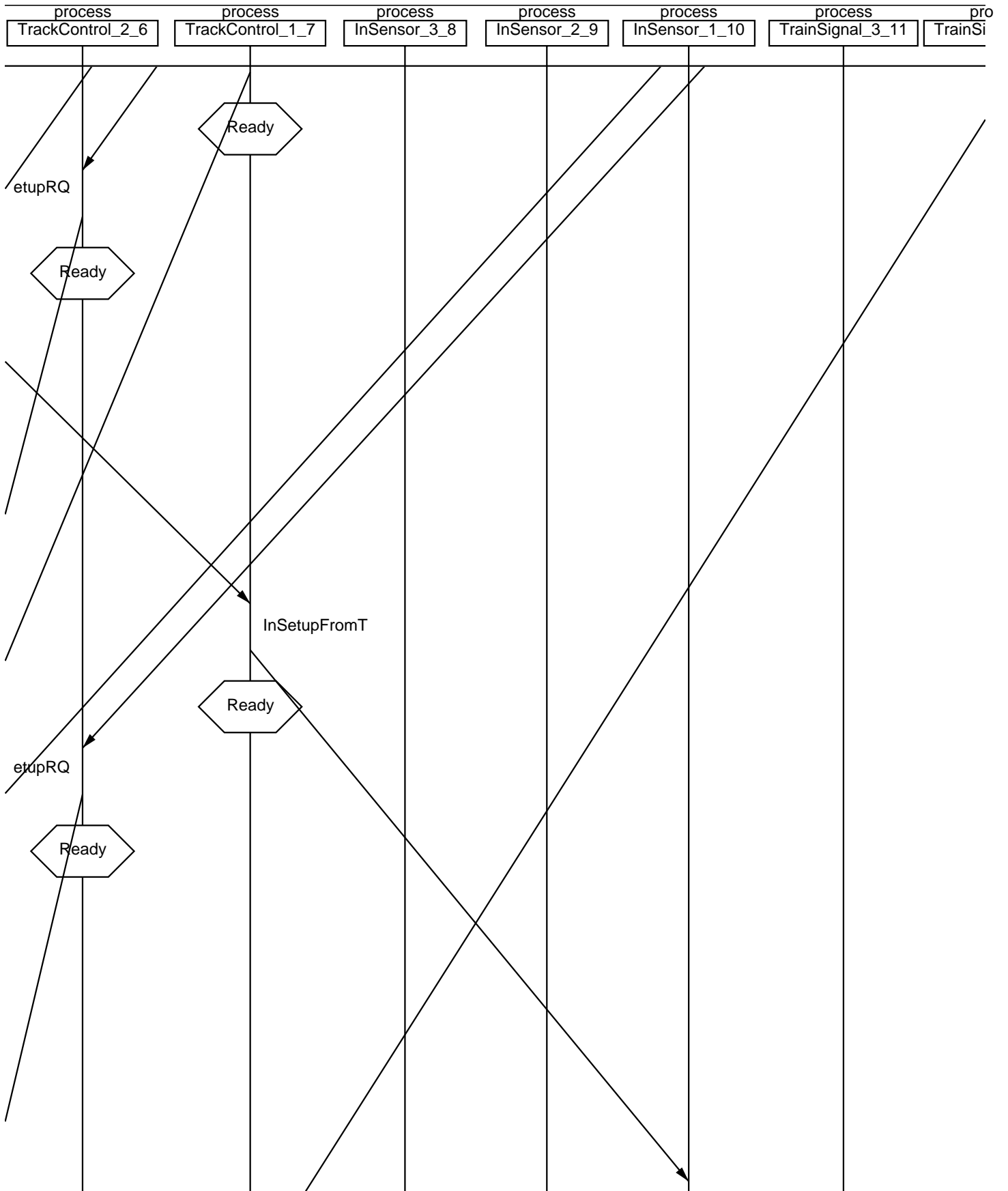


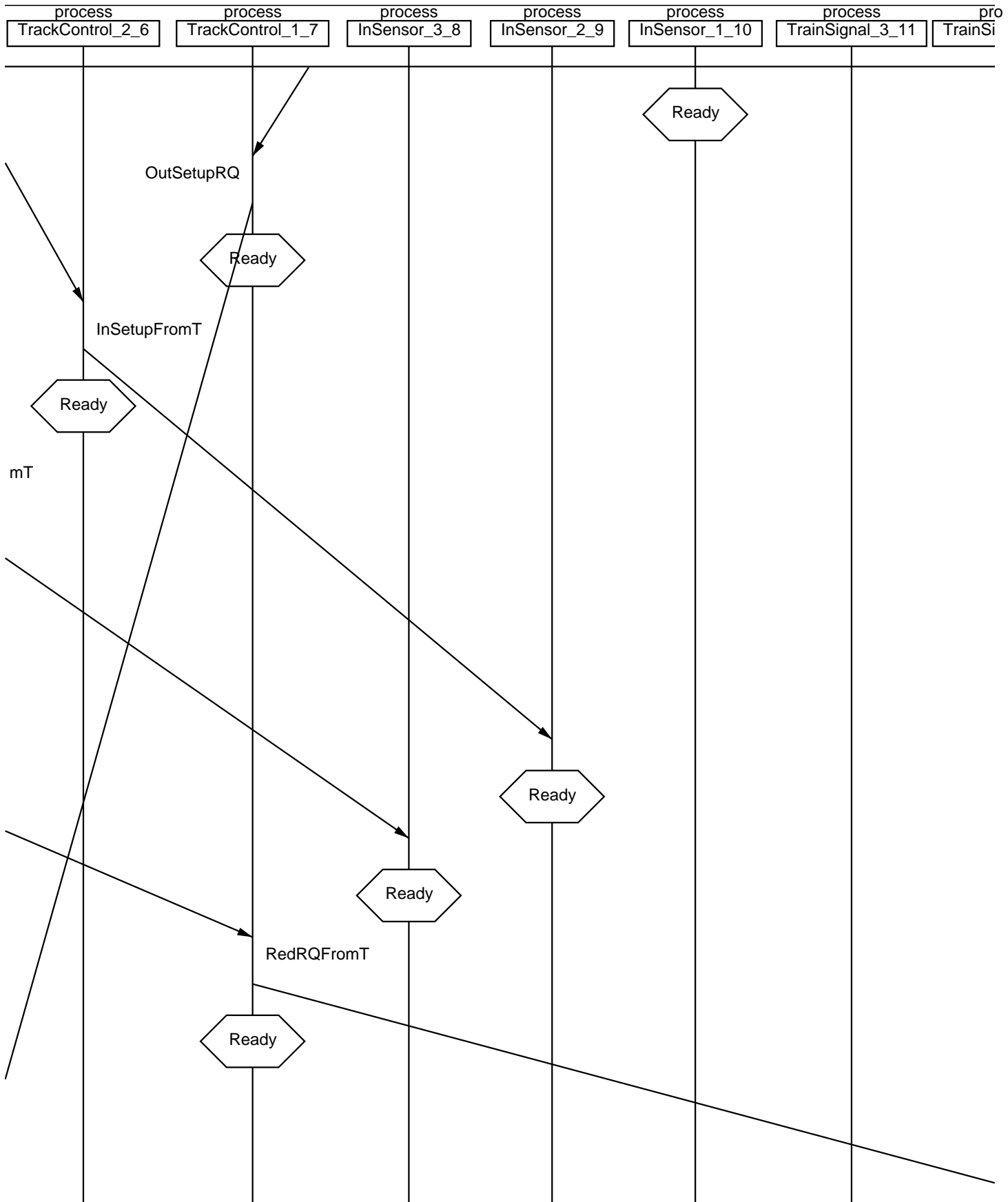




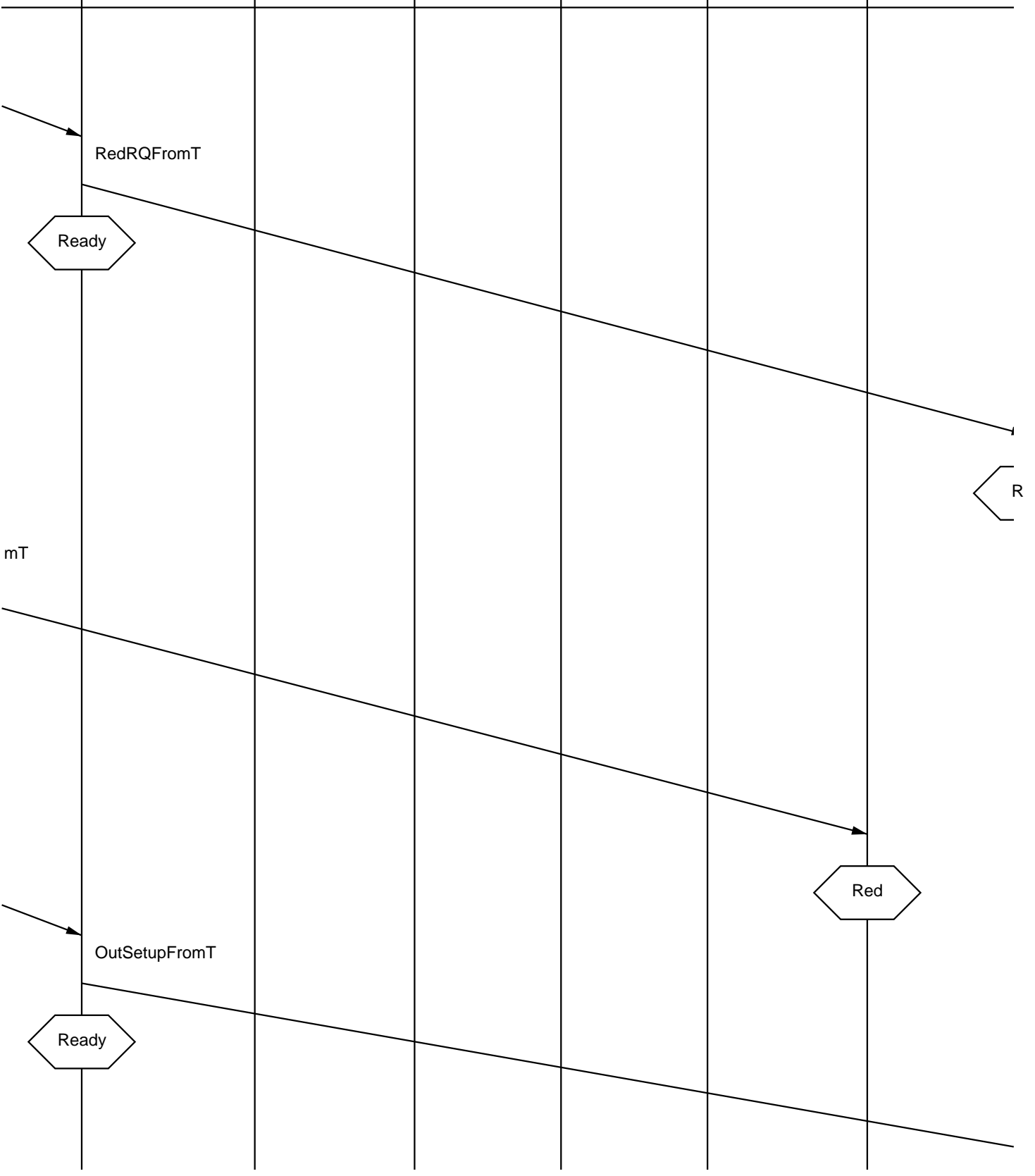




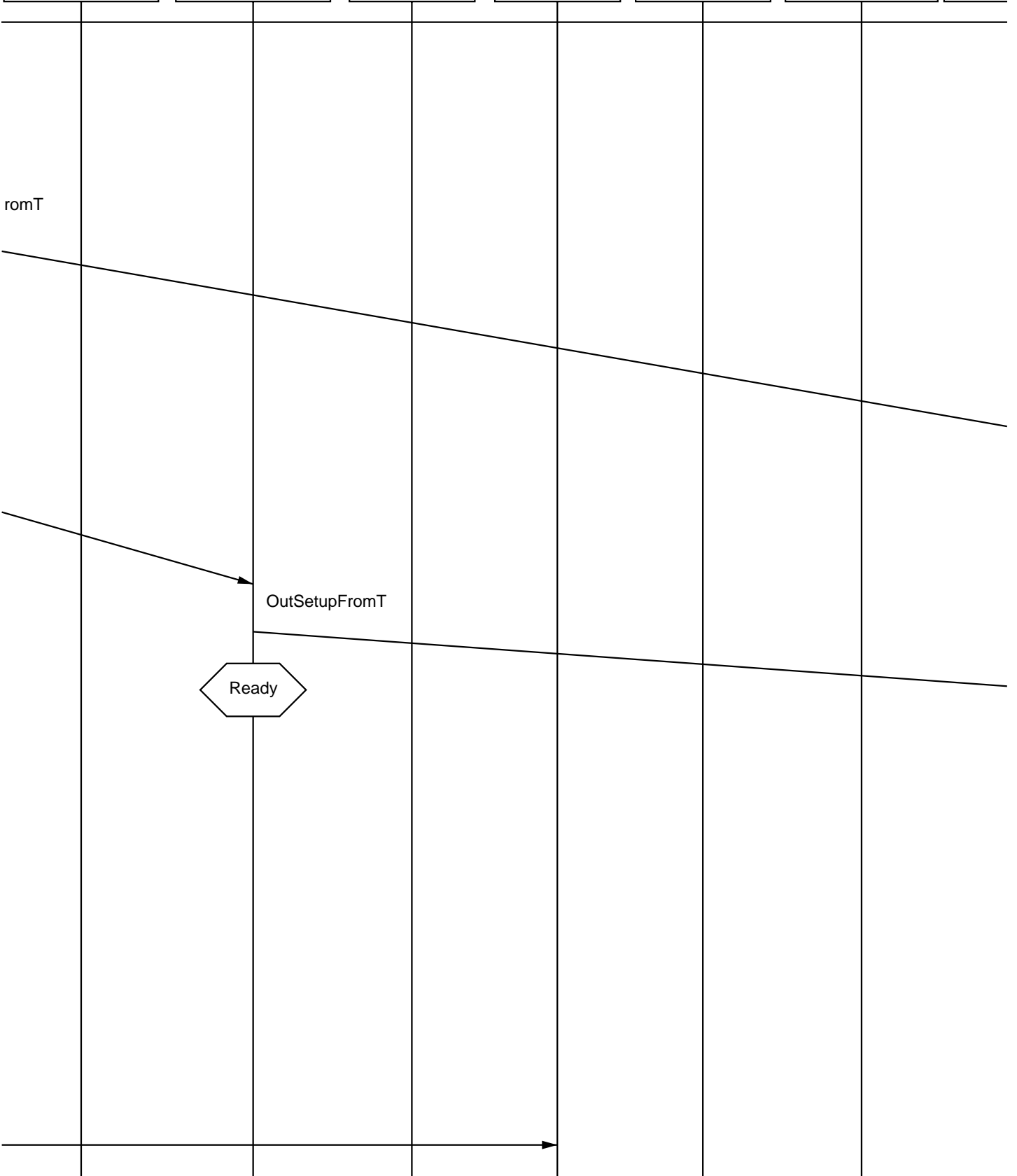


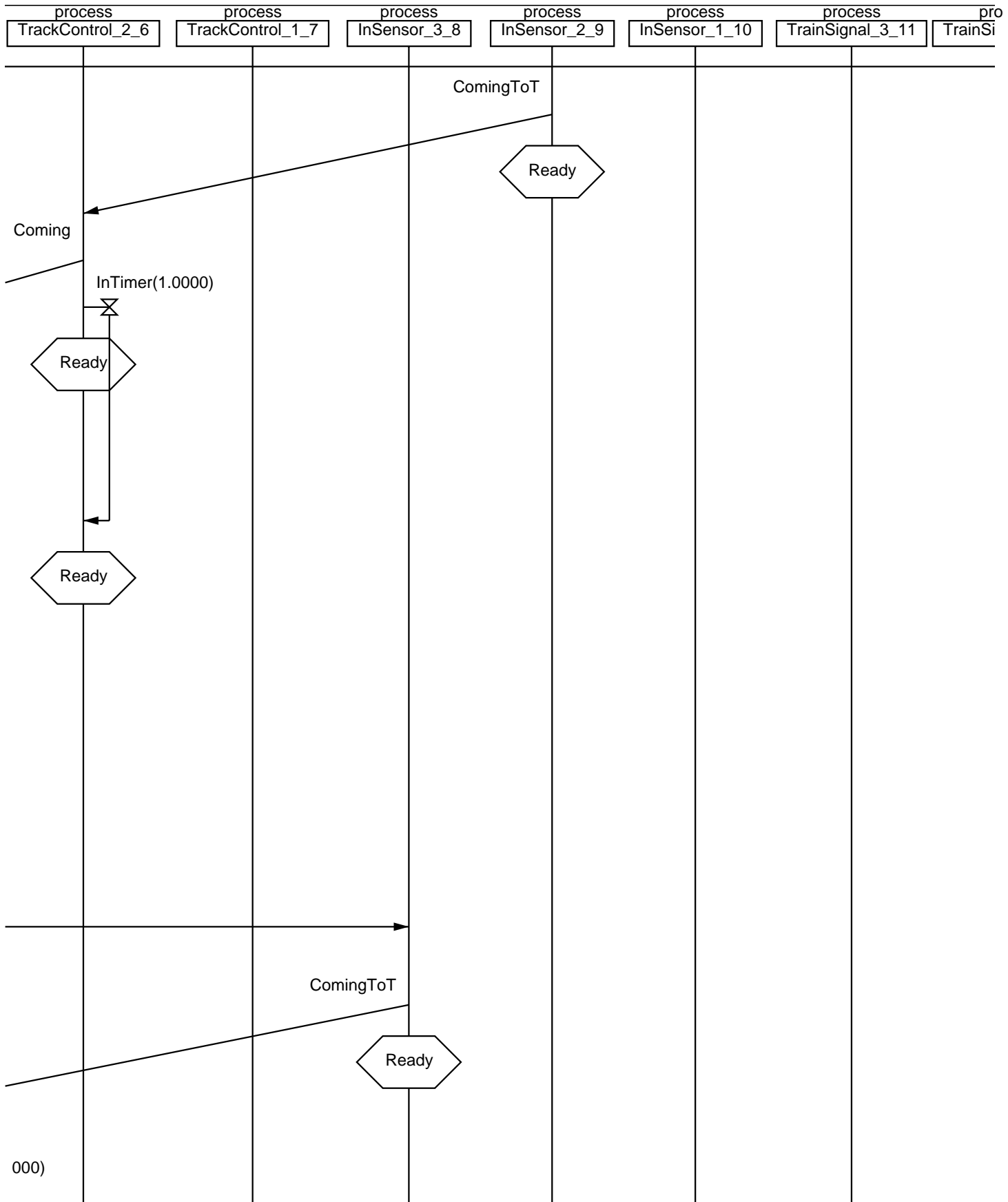


process TrackControl_2_6 process TrackControl_1_7 process InSensor_3_8 process InSensor_2_9 process InSensor_1_10 process TrainSignal_3_11 pro TrainSi



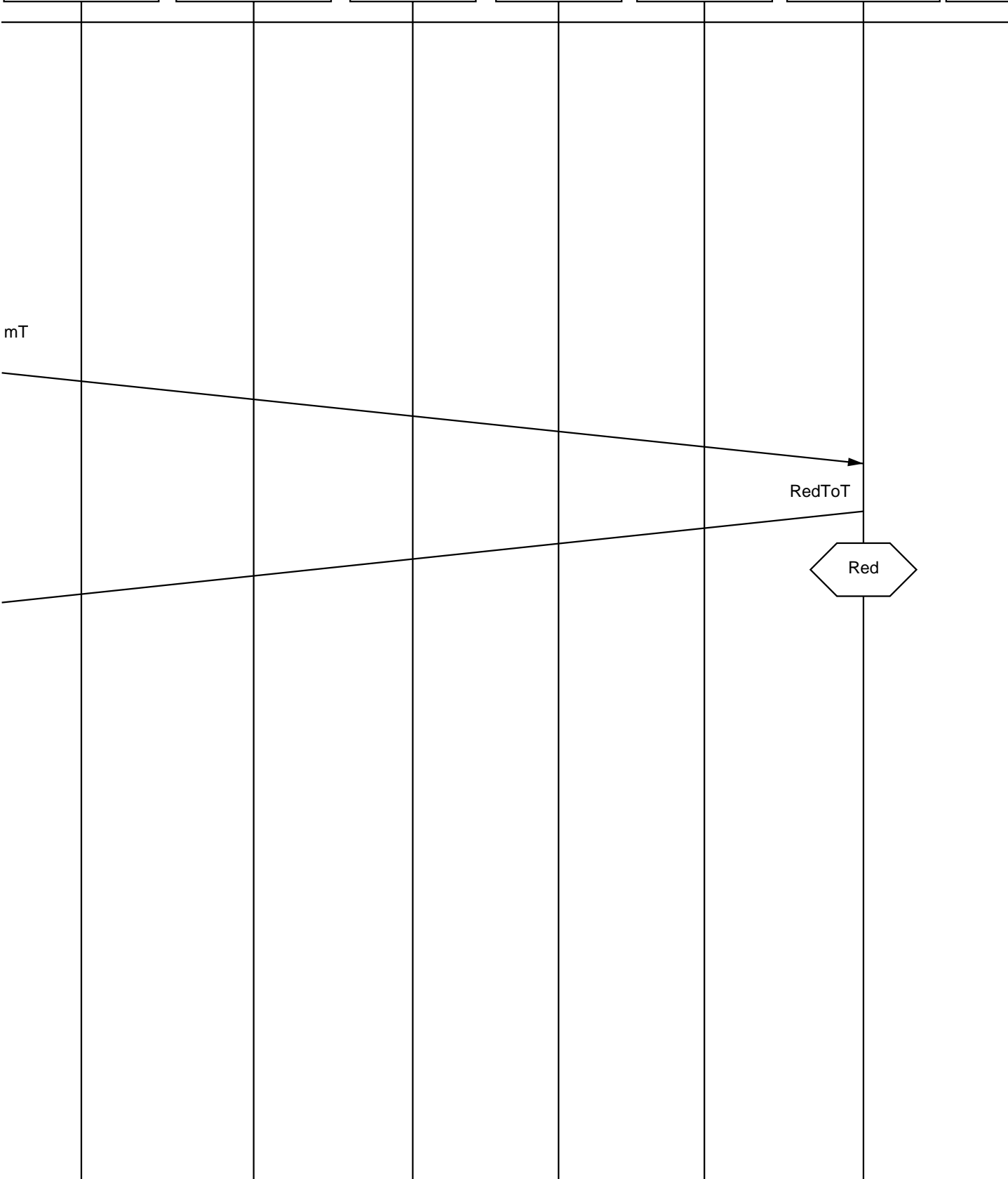
process TrackControl_2_6 process TrackControl_1_7 process InSensor_3_8 process InSensor_2_9 process InSensor_1_10 process TrainSignal_3_11 process TrainSi





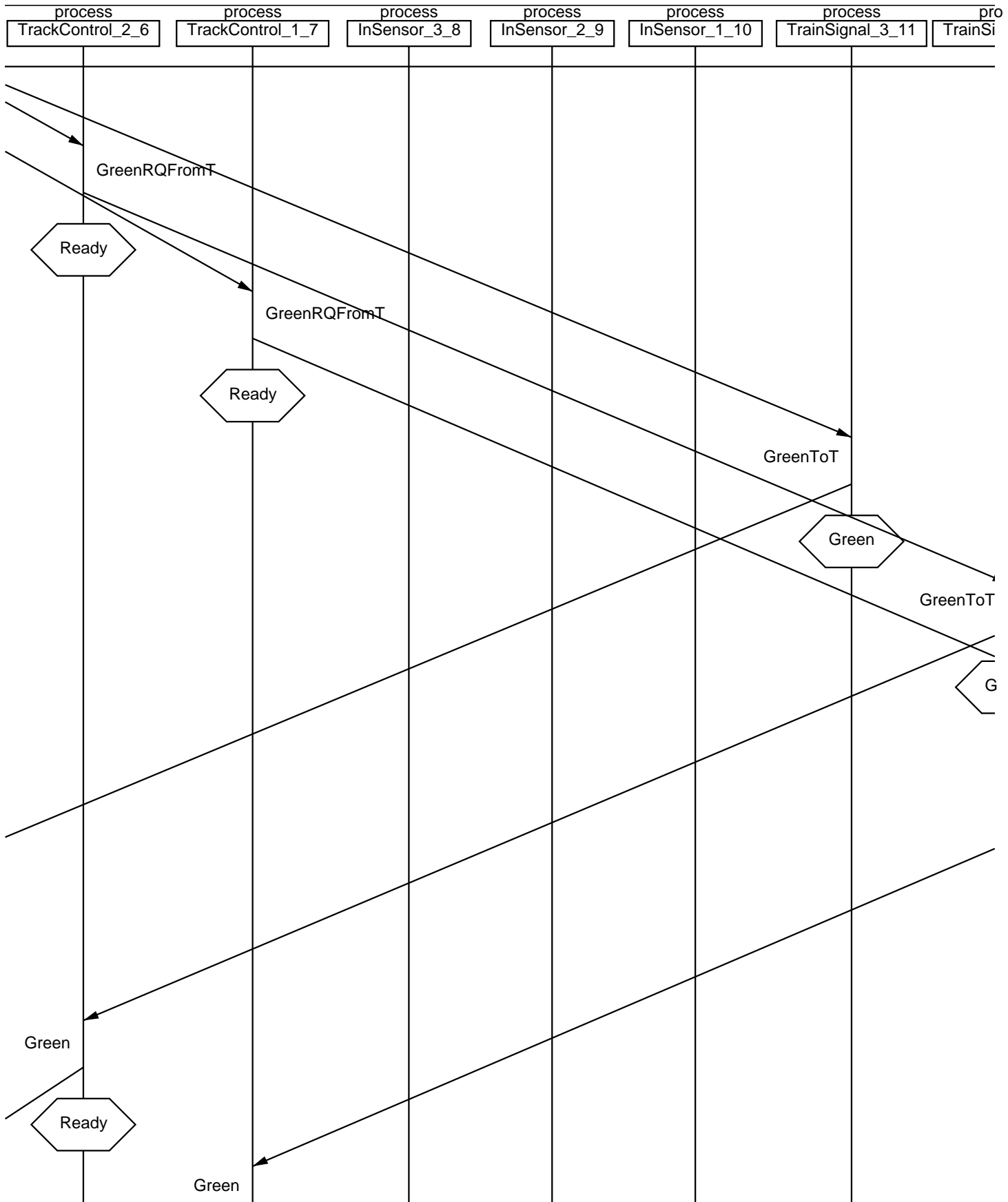
000)

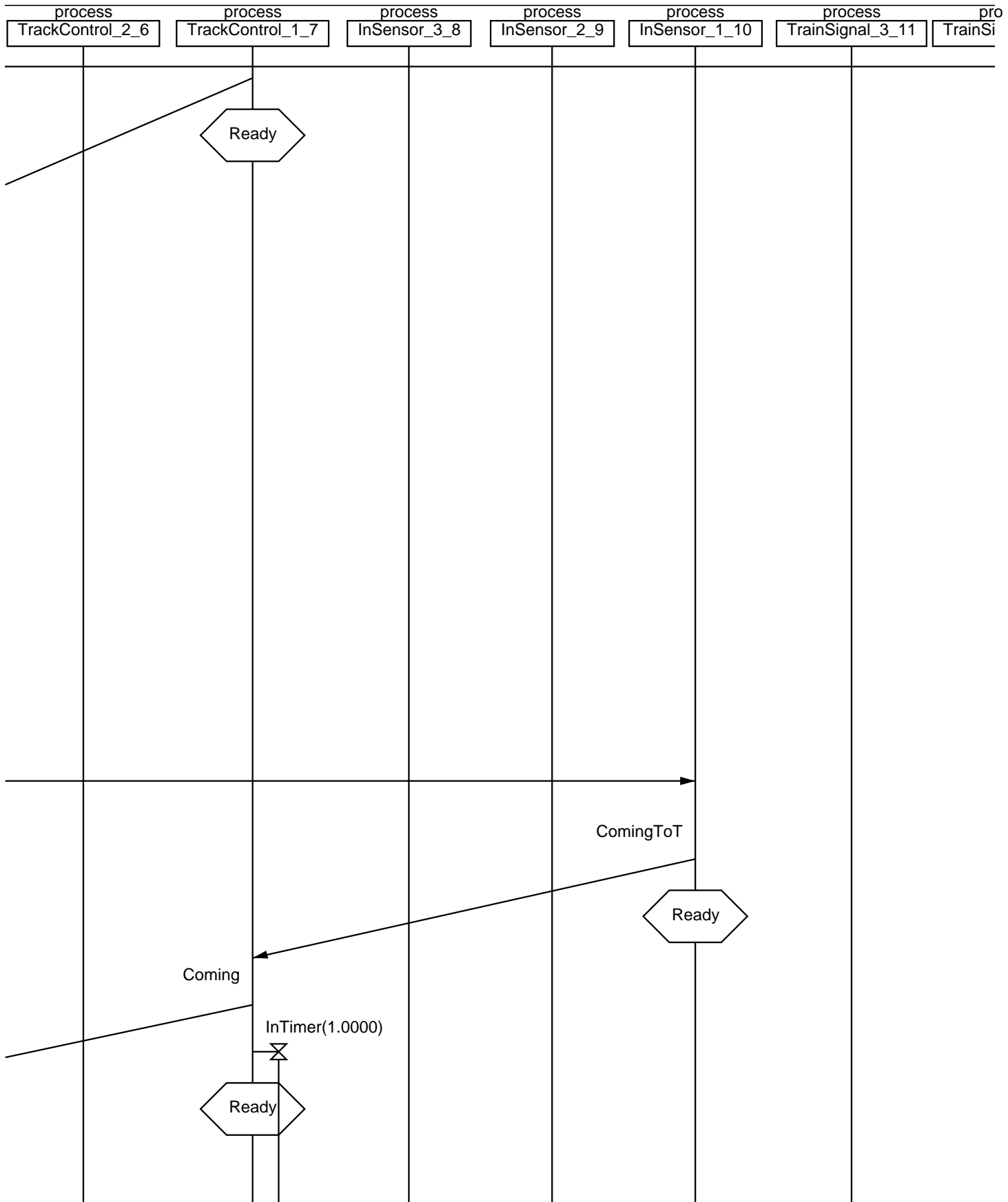
process process process process process process pro
TrackControl_2_6 TrackControl_1_7 InSensor_3_8 InSensor_2_9 InSensor_1_10 TrainSignal_3_11 TrainSi



process	process	process	process	process	process	pro
TrackControl_2_6	TrackControl_1_7	InSensor_3_8	InSensor_2_9	InSensor_1_10	TrainSignal_3_11	TrainSi

romT





process process process process process process pro

TrackControl_2_6

TrackControl_1_7

InSensor_3_8

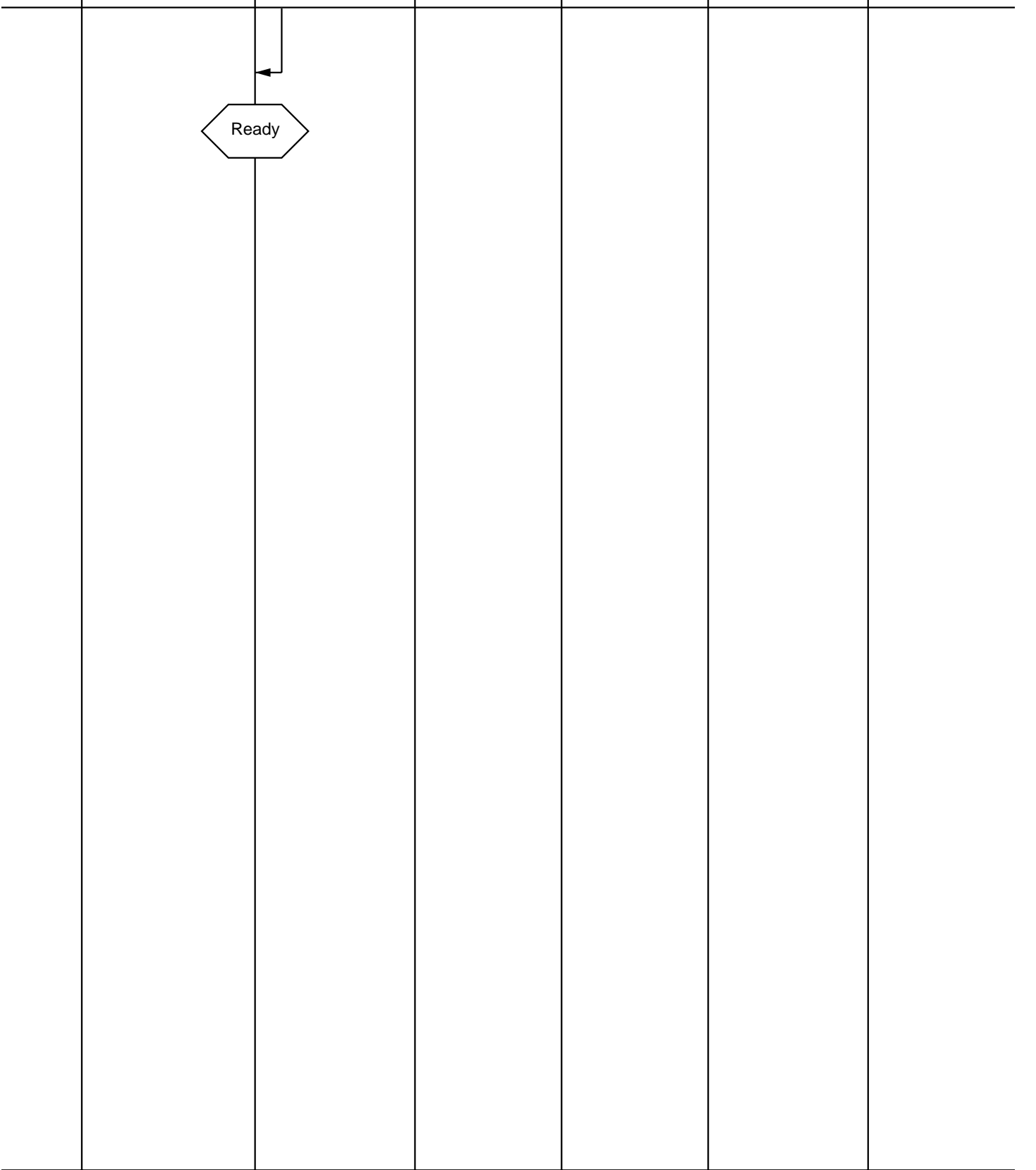
InSensor_2_9

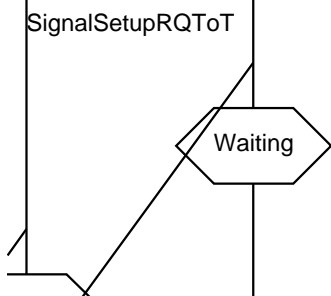
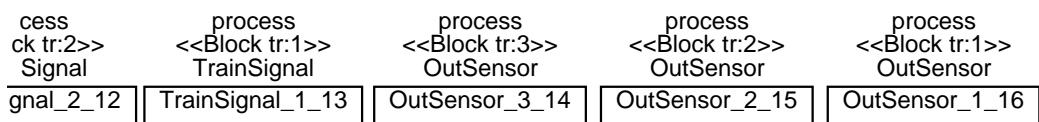
InSensor_1_10

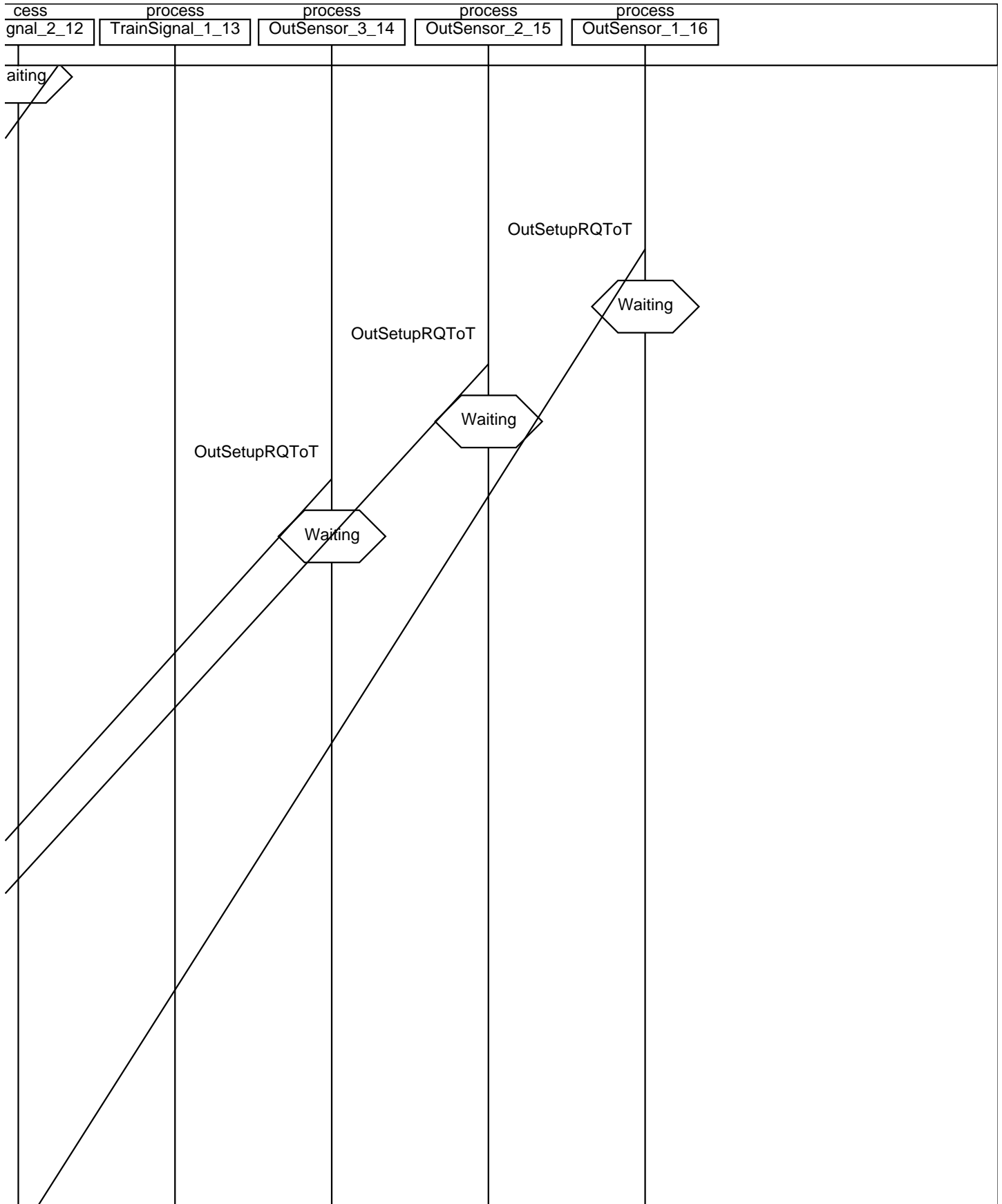
TrainSignal_3_11

TrainSi

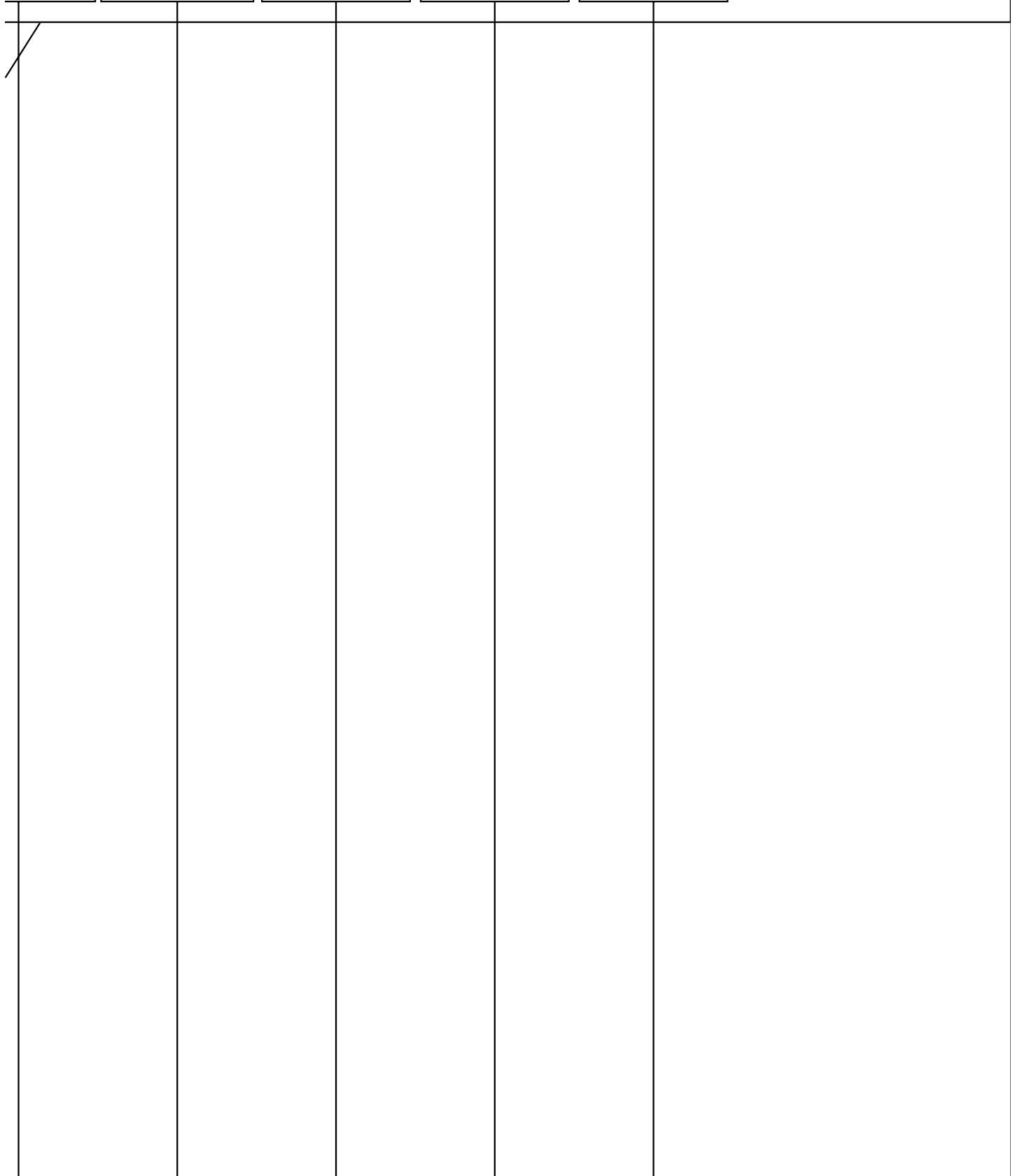
Ready





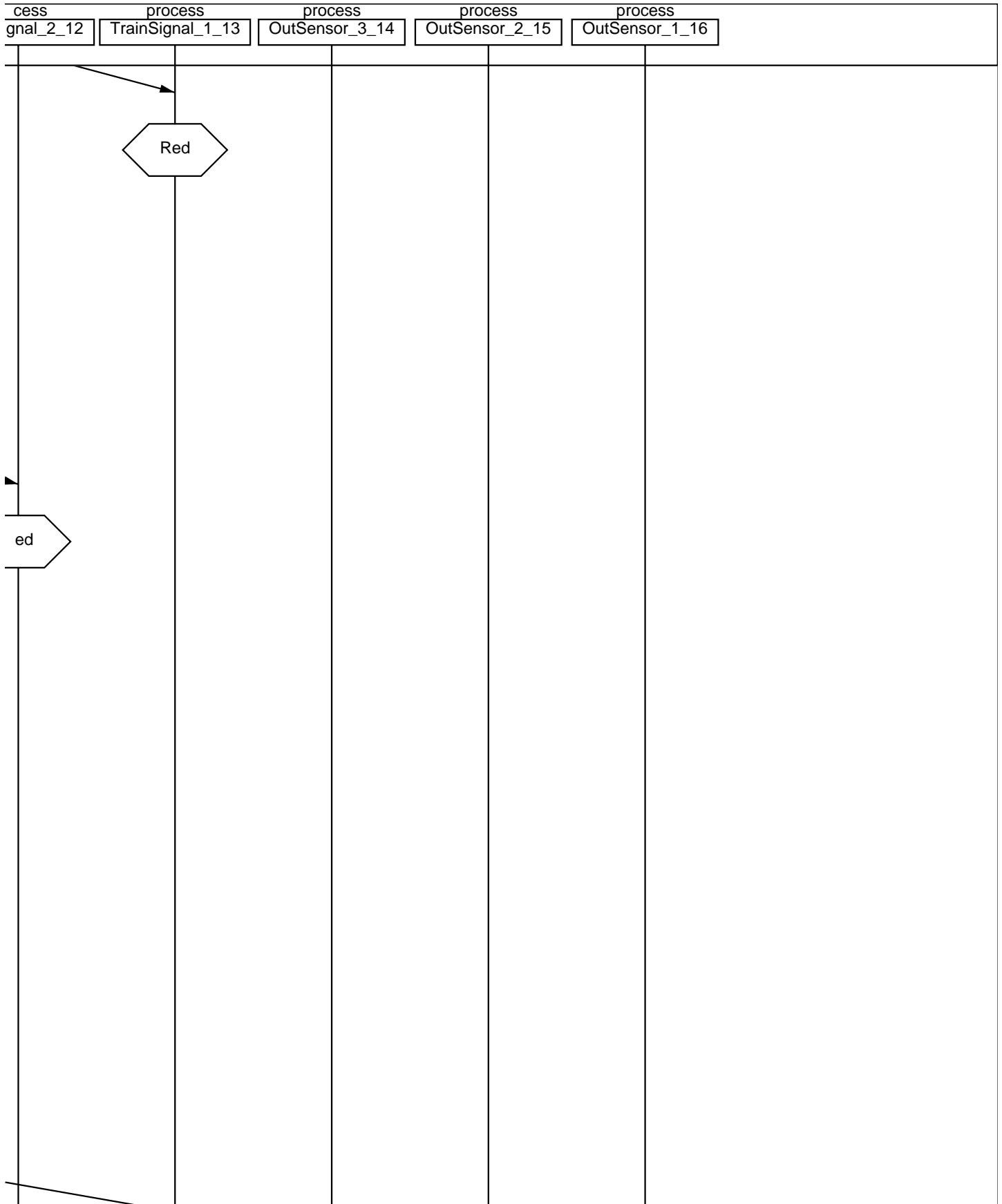


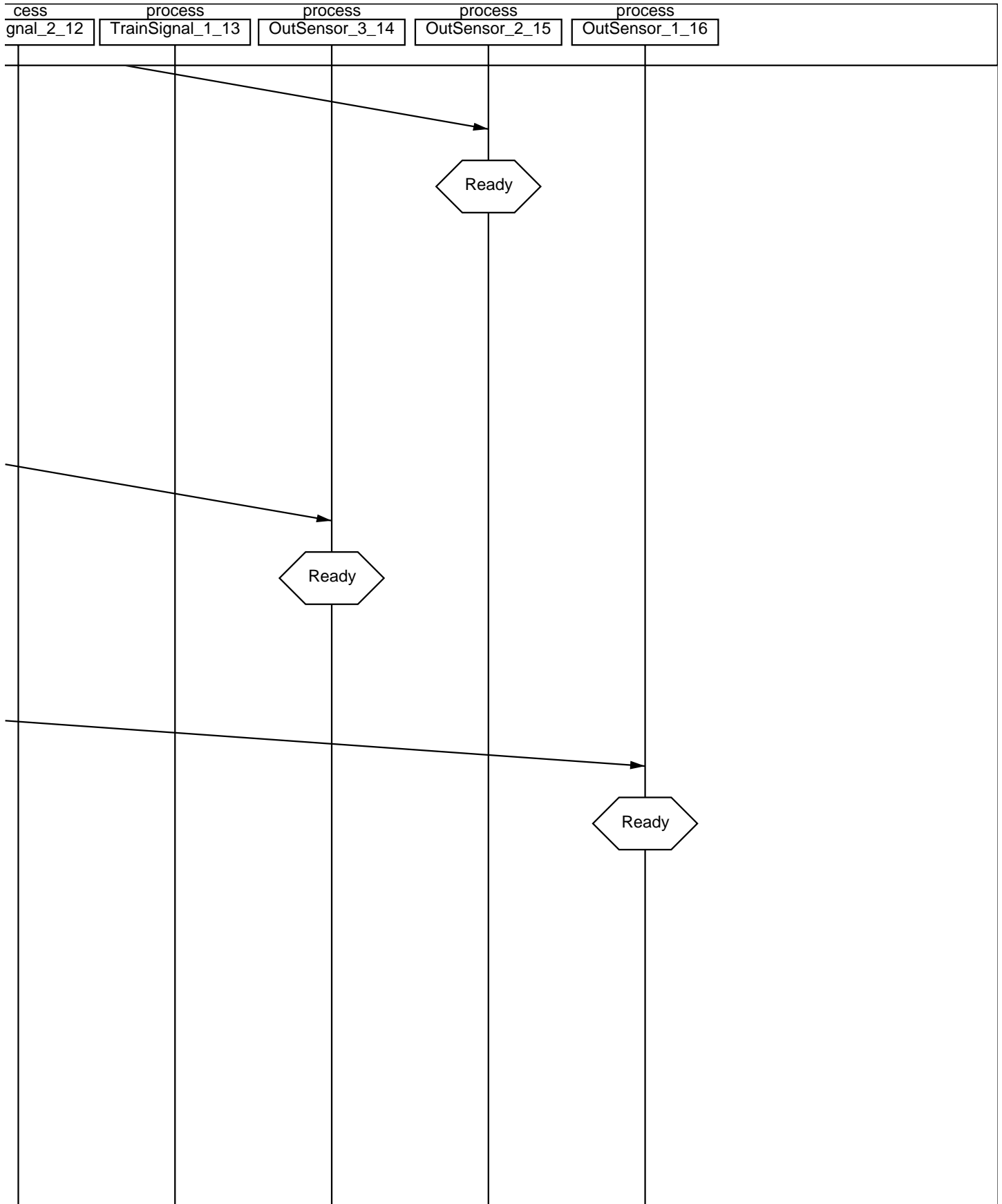
cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16



cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

--	--	--	--	--	--





cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

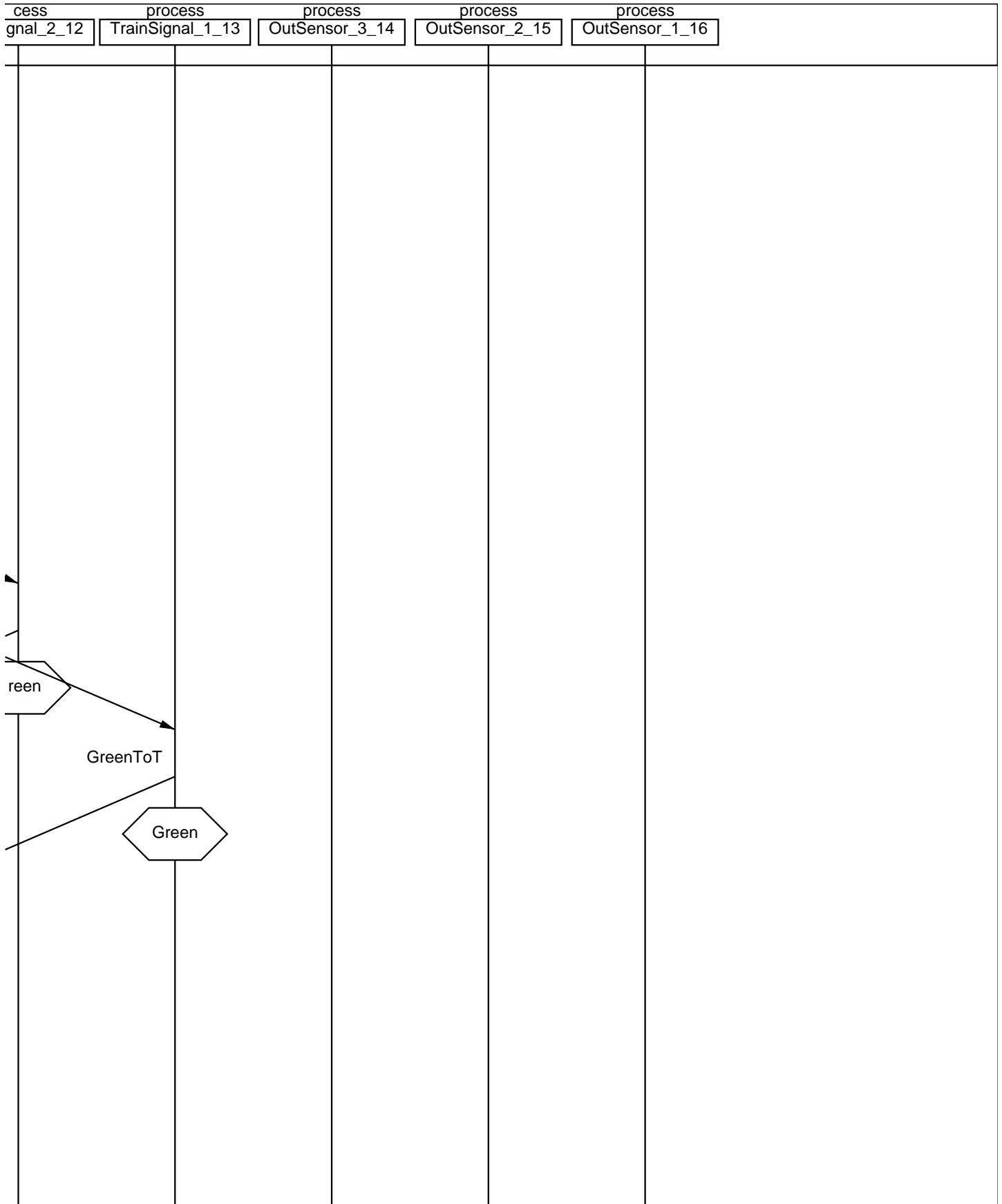
--	--	--	--	--	--

cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

--	--	--	--	--	--

cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

--	--	--	--	--	--



cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

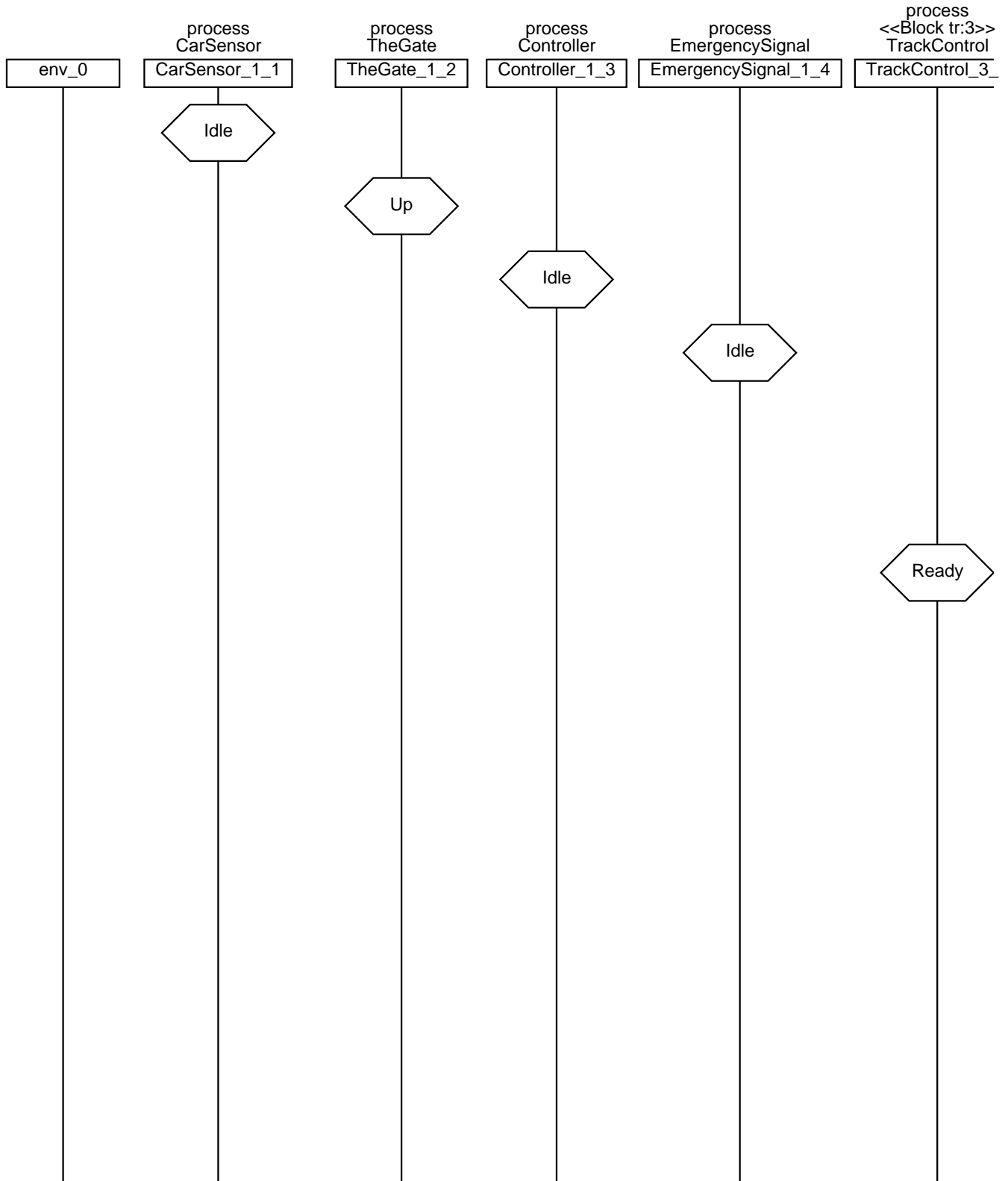
--	--	--	--	--	--

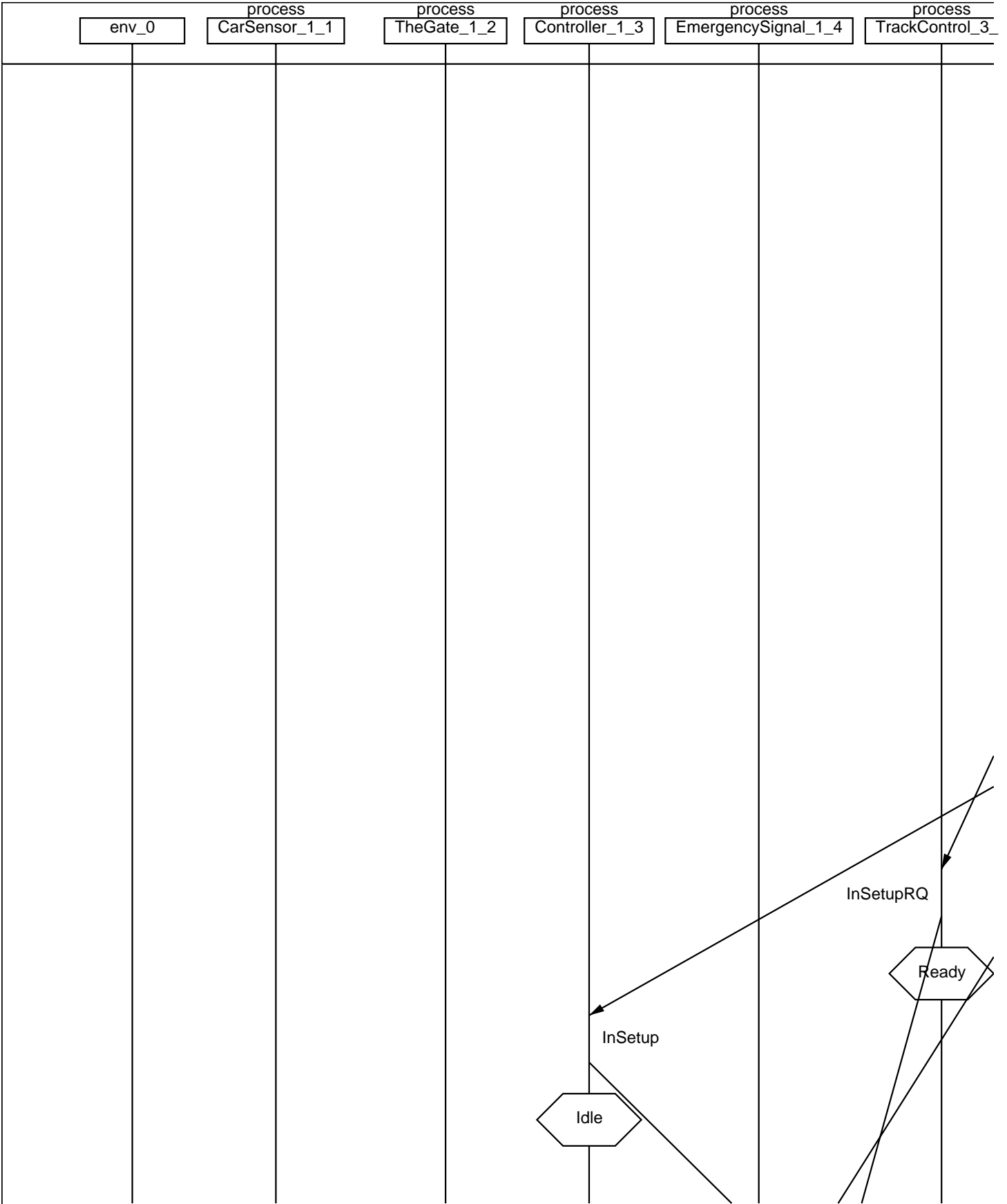
cess	process	process	process	process
gnal_2_12	TrainSignal_1_13	OutSensor_3_14	OutSensor_2_15	OutSensor_1_16

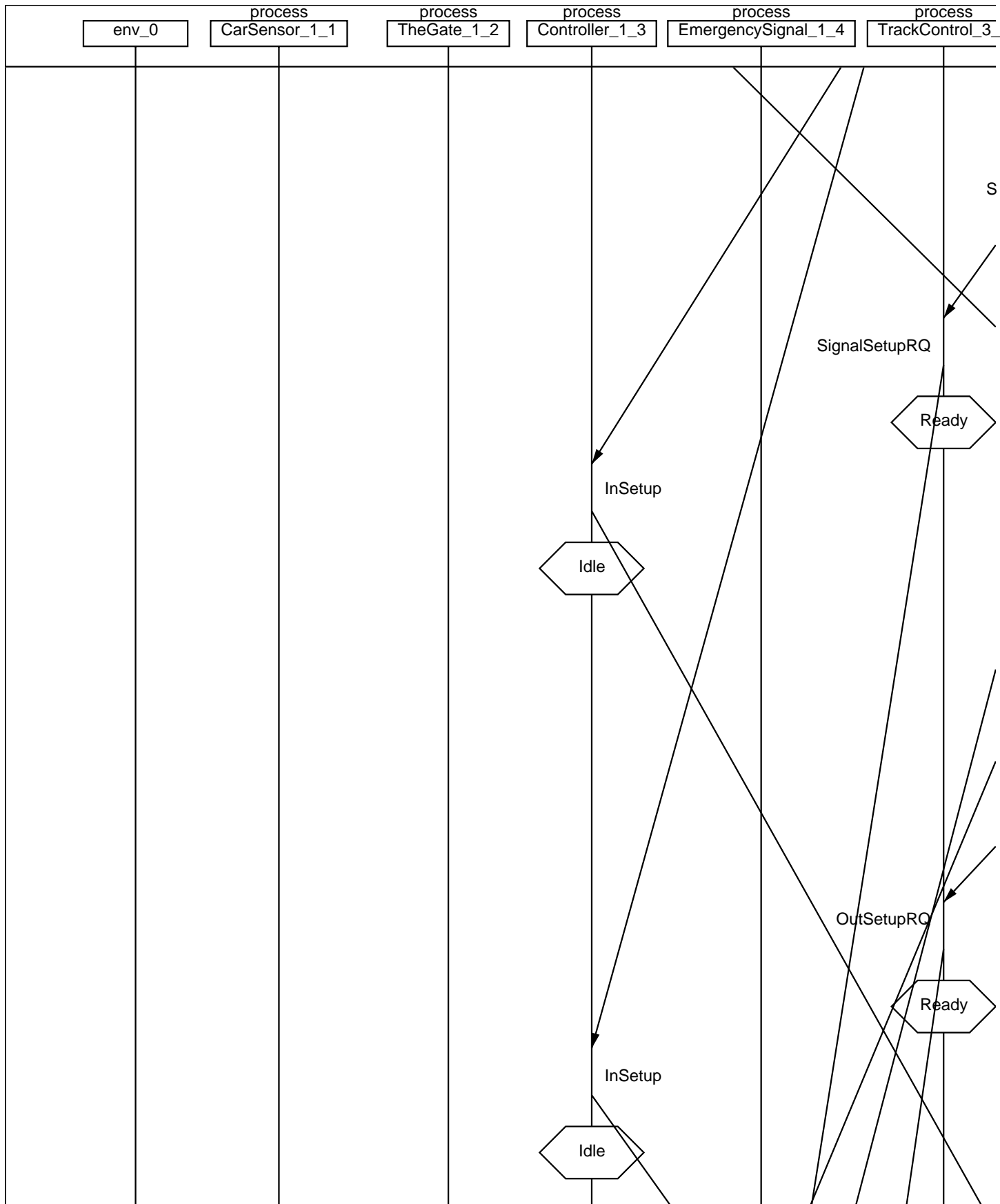
--	--	--	--	--

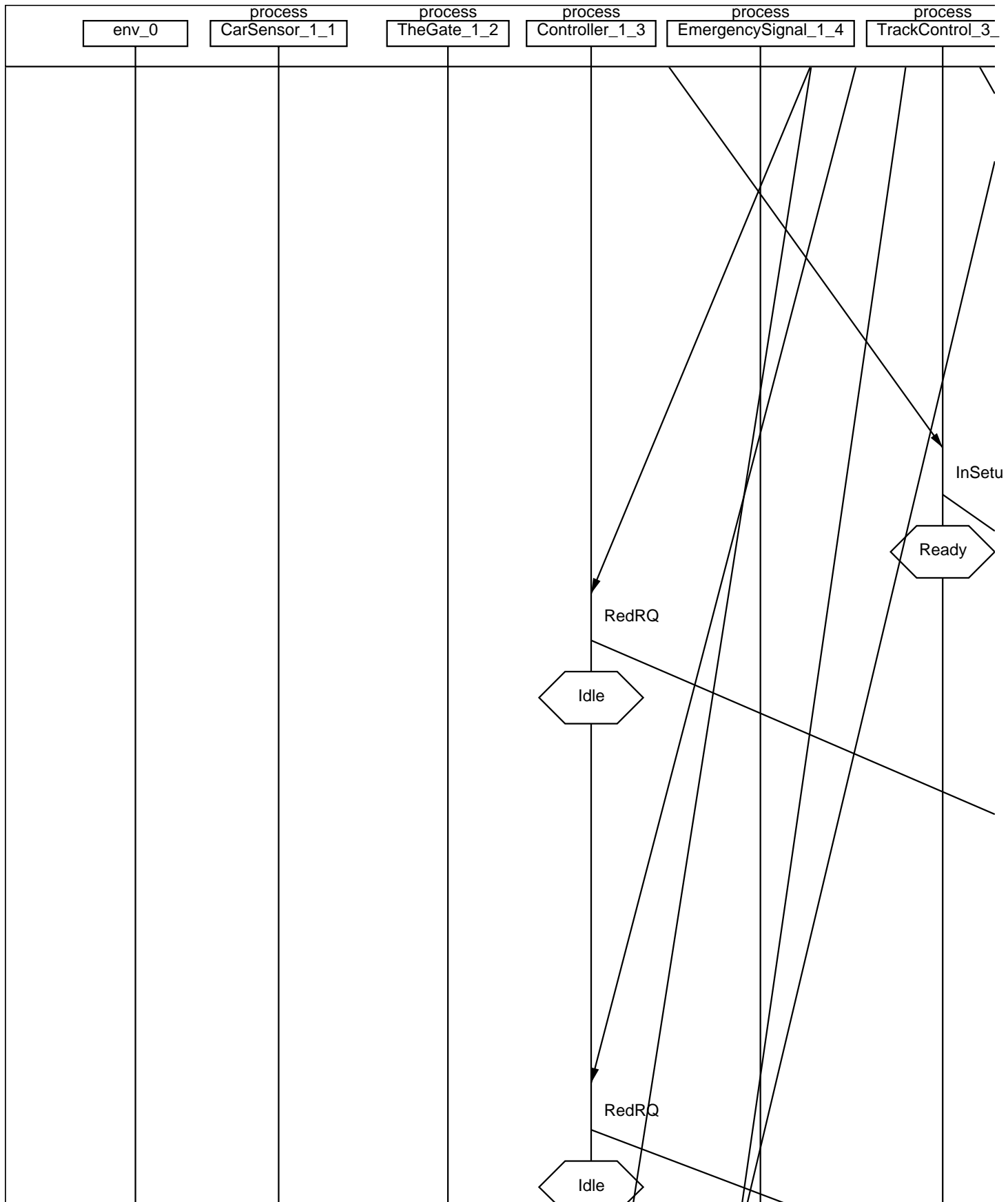
MSC CompleteMSC_TestCaseF_Strategy4

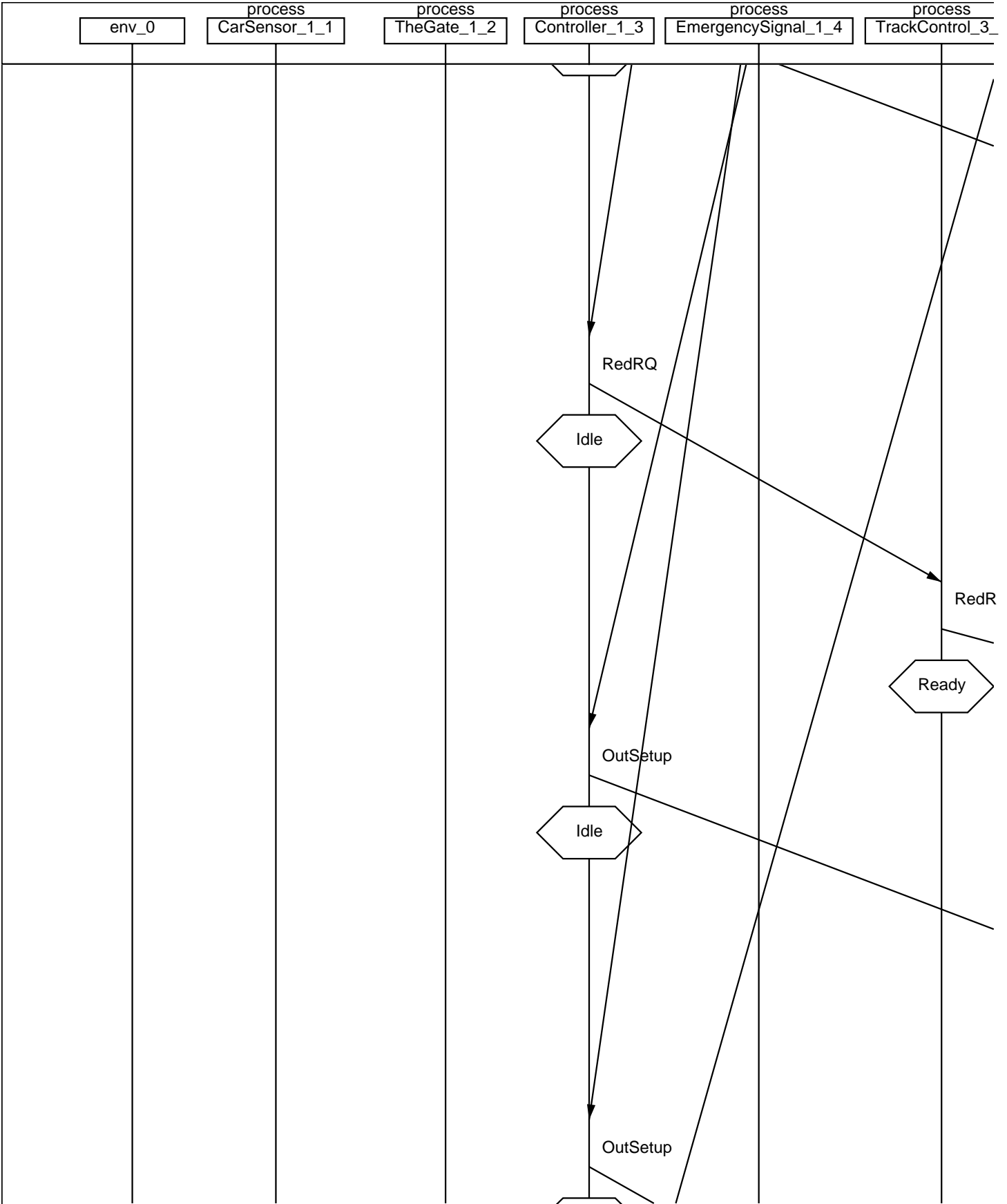
Simulation trace
generated by
SDL Simulator 4.3

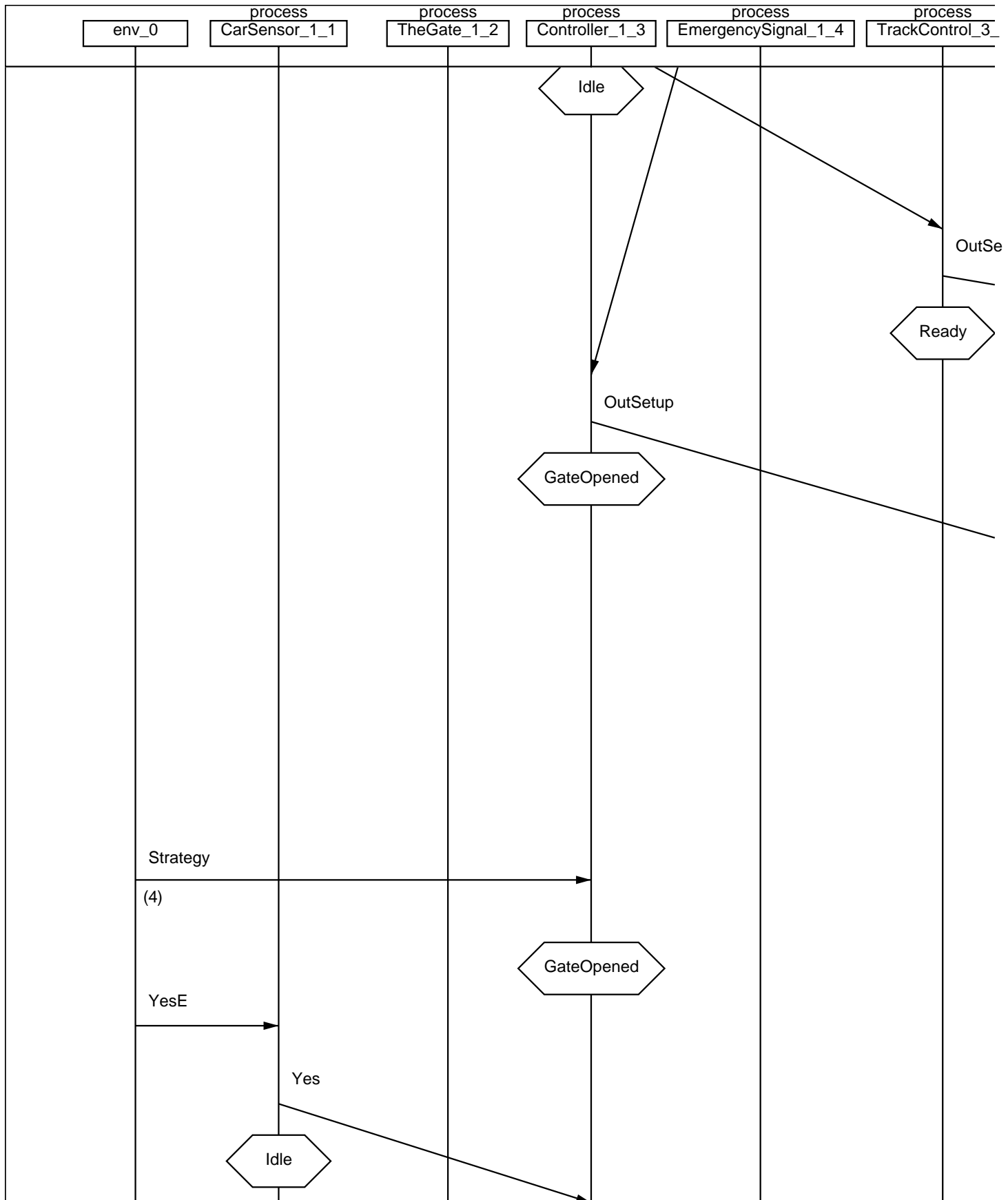


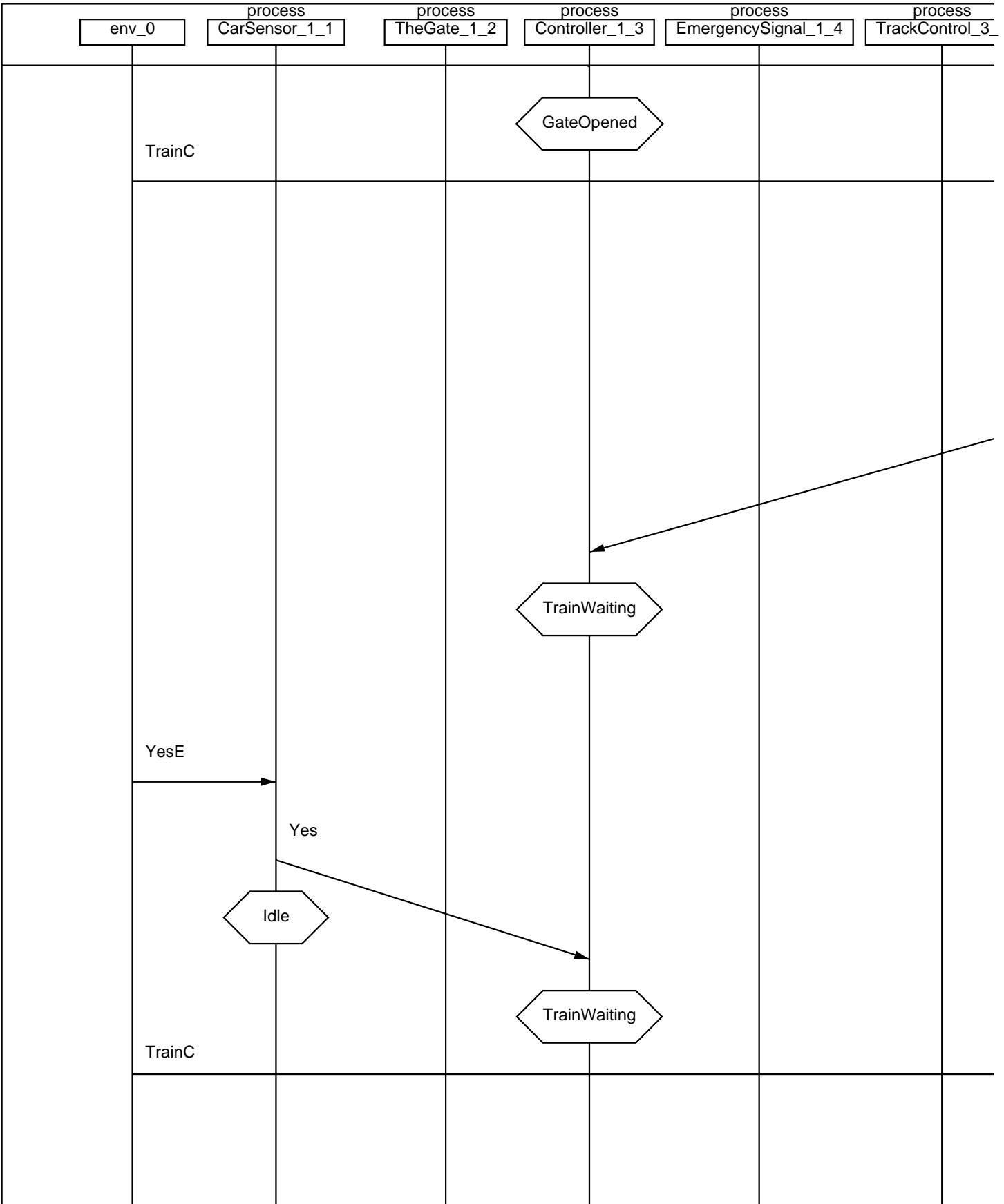


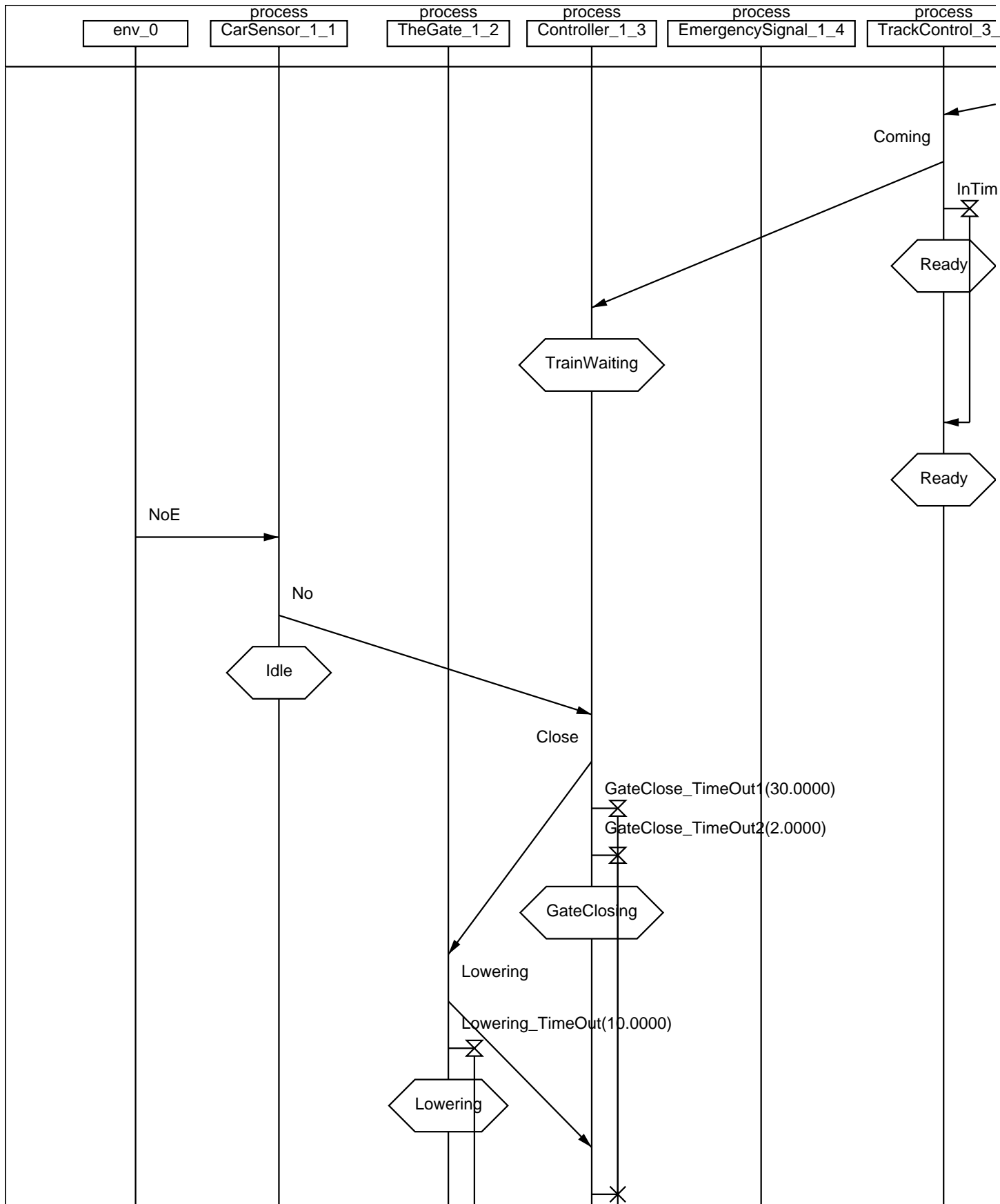


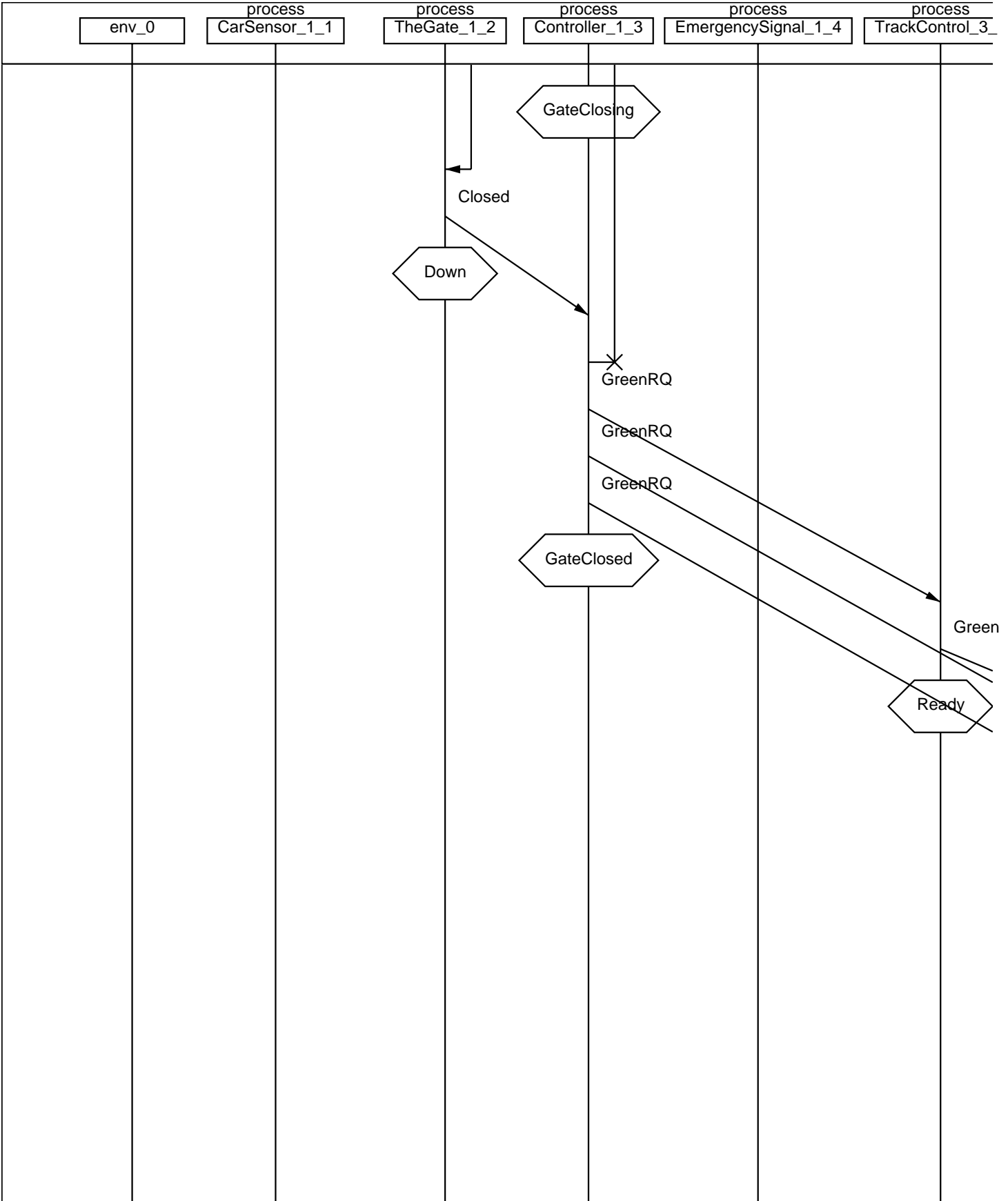


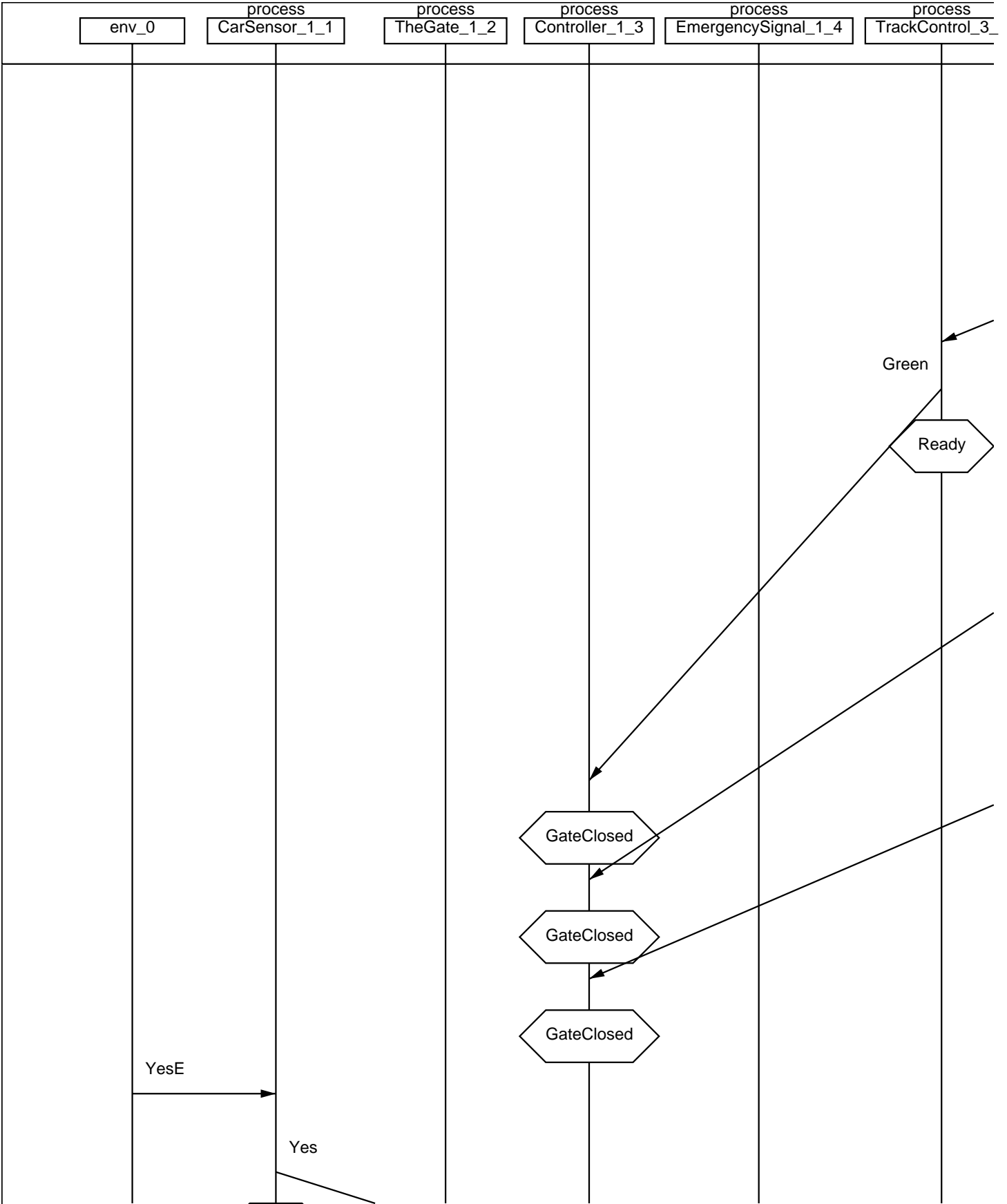


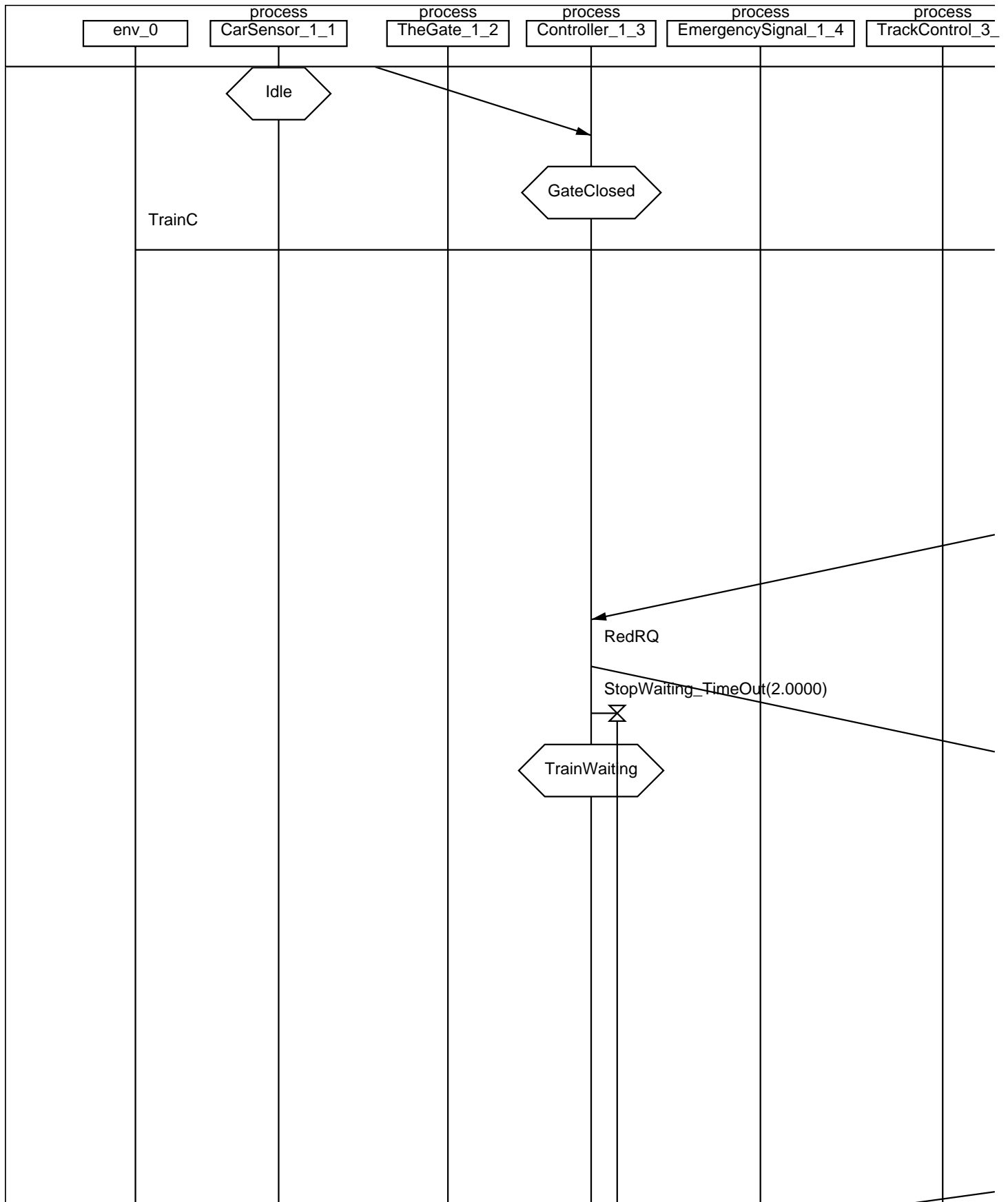


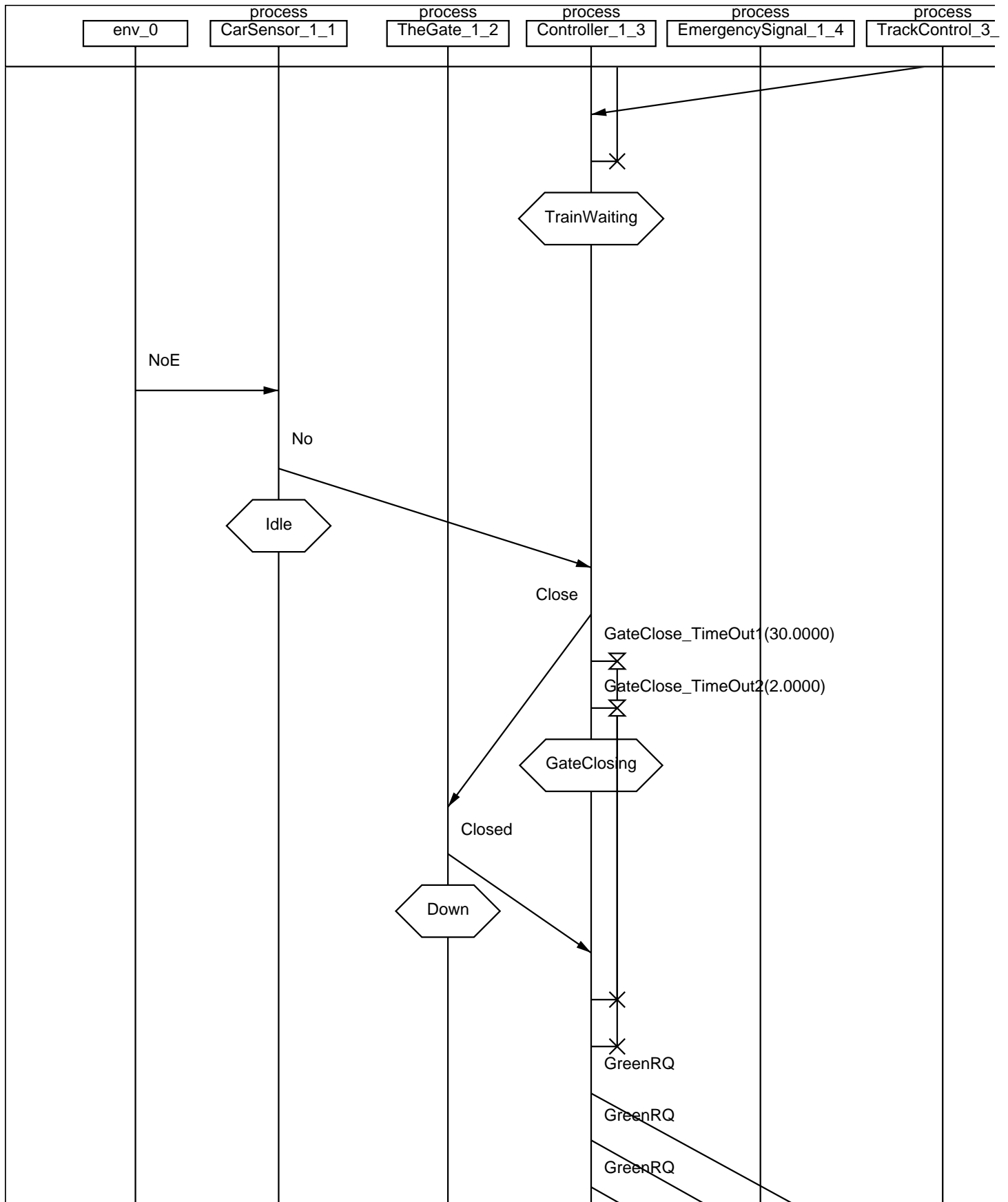


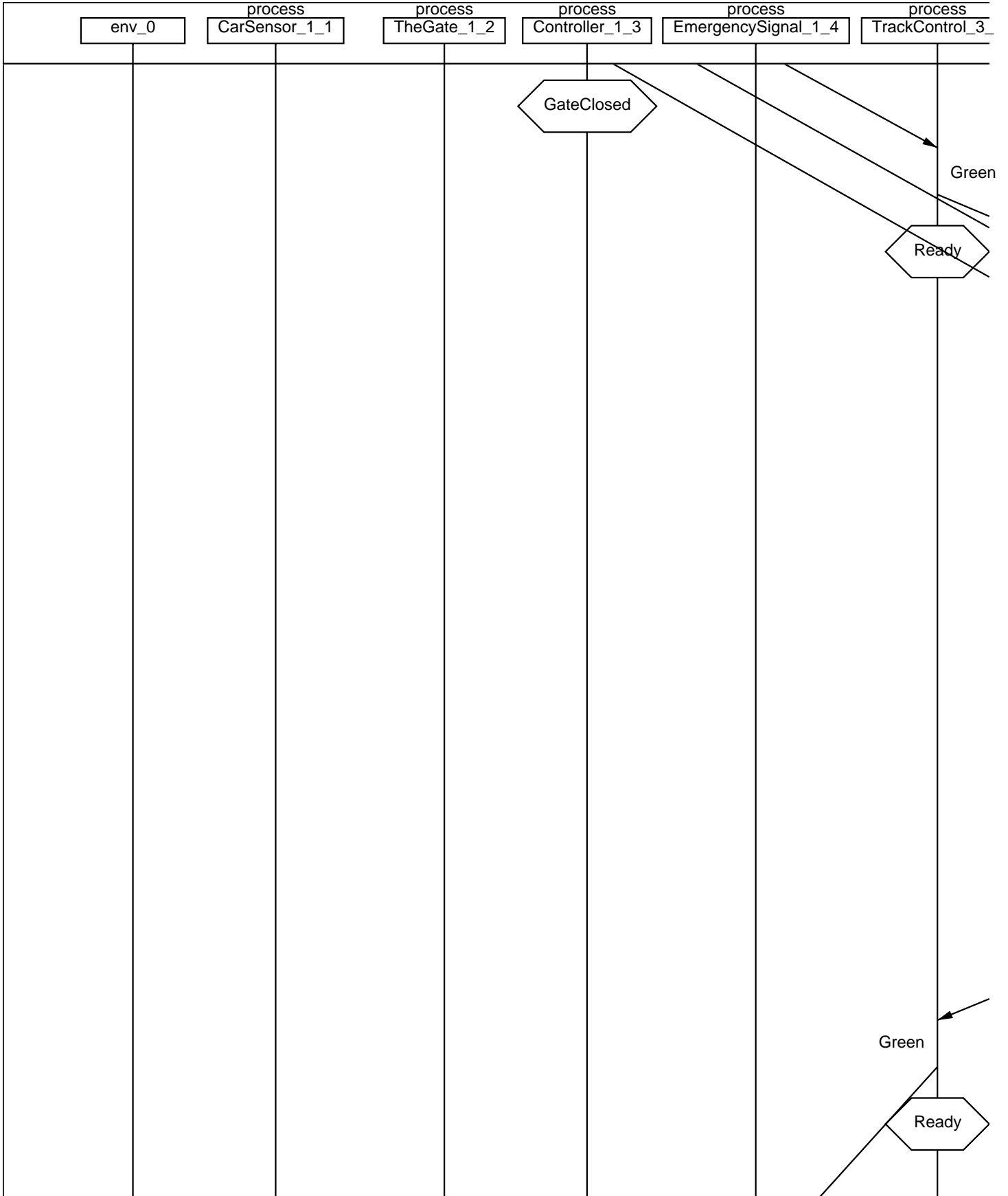


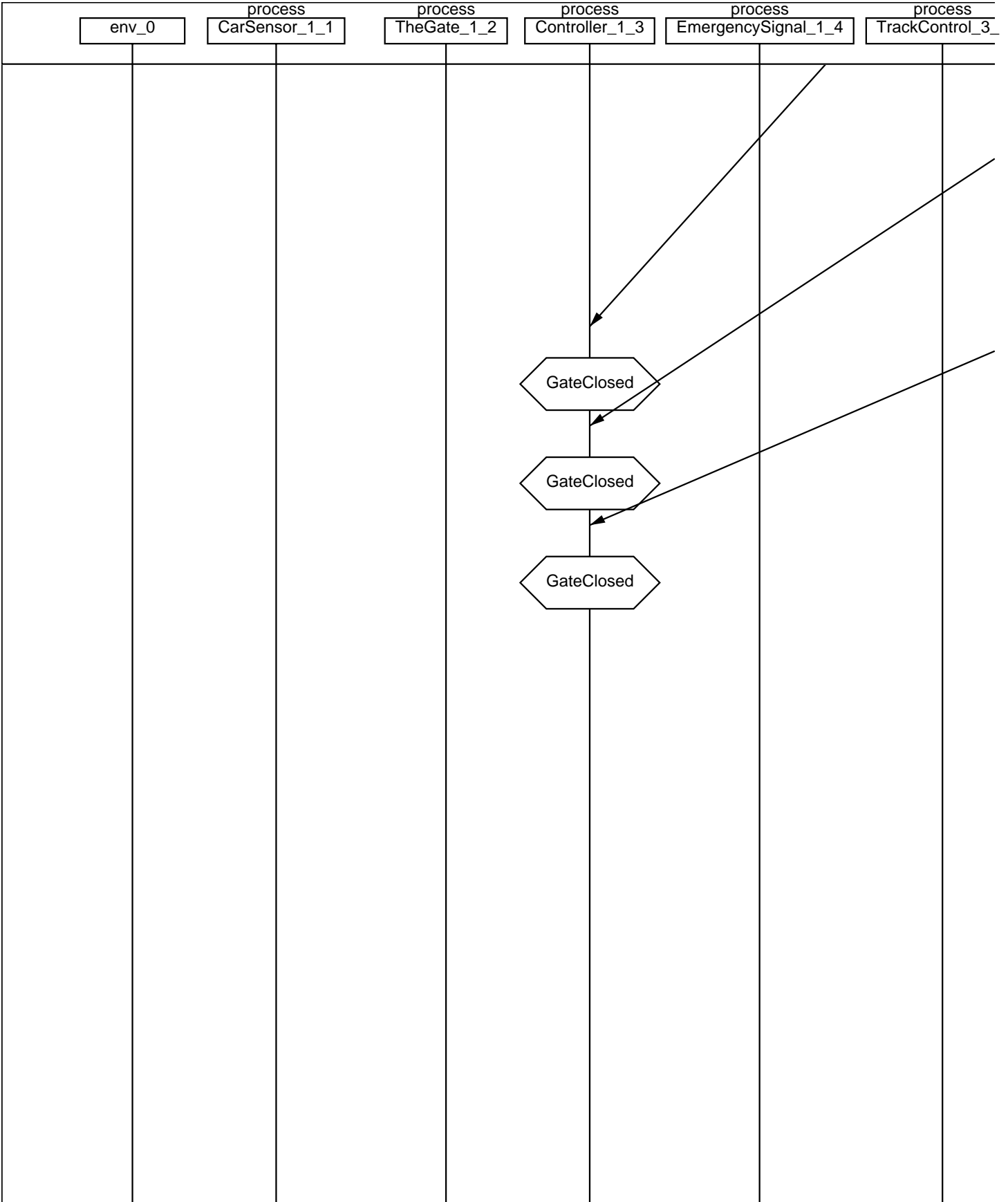


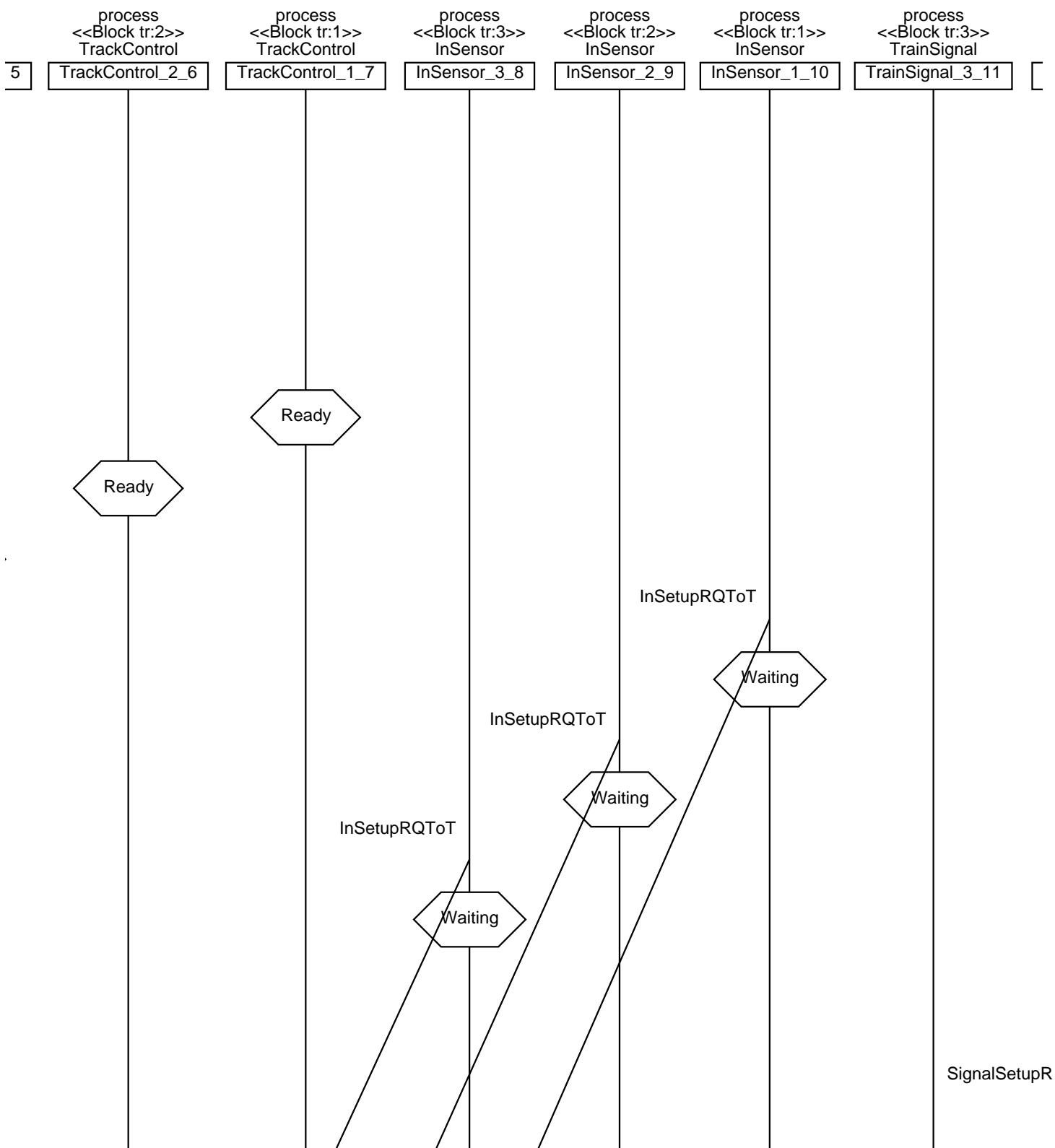


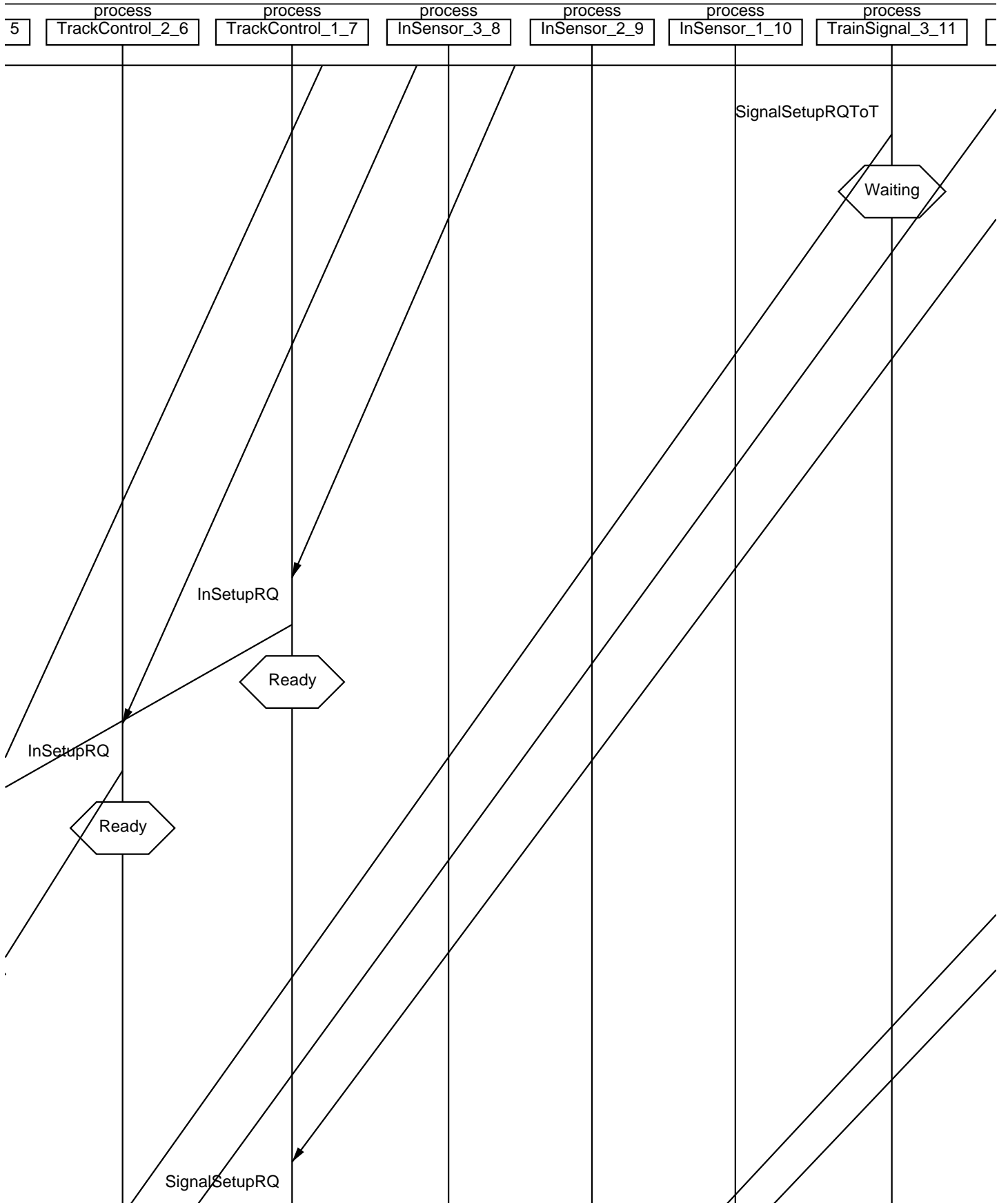


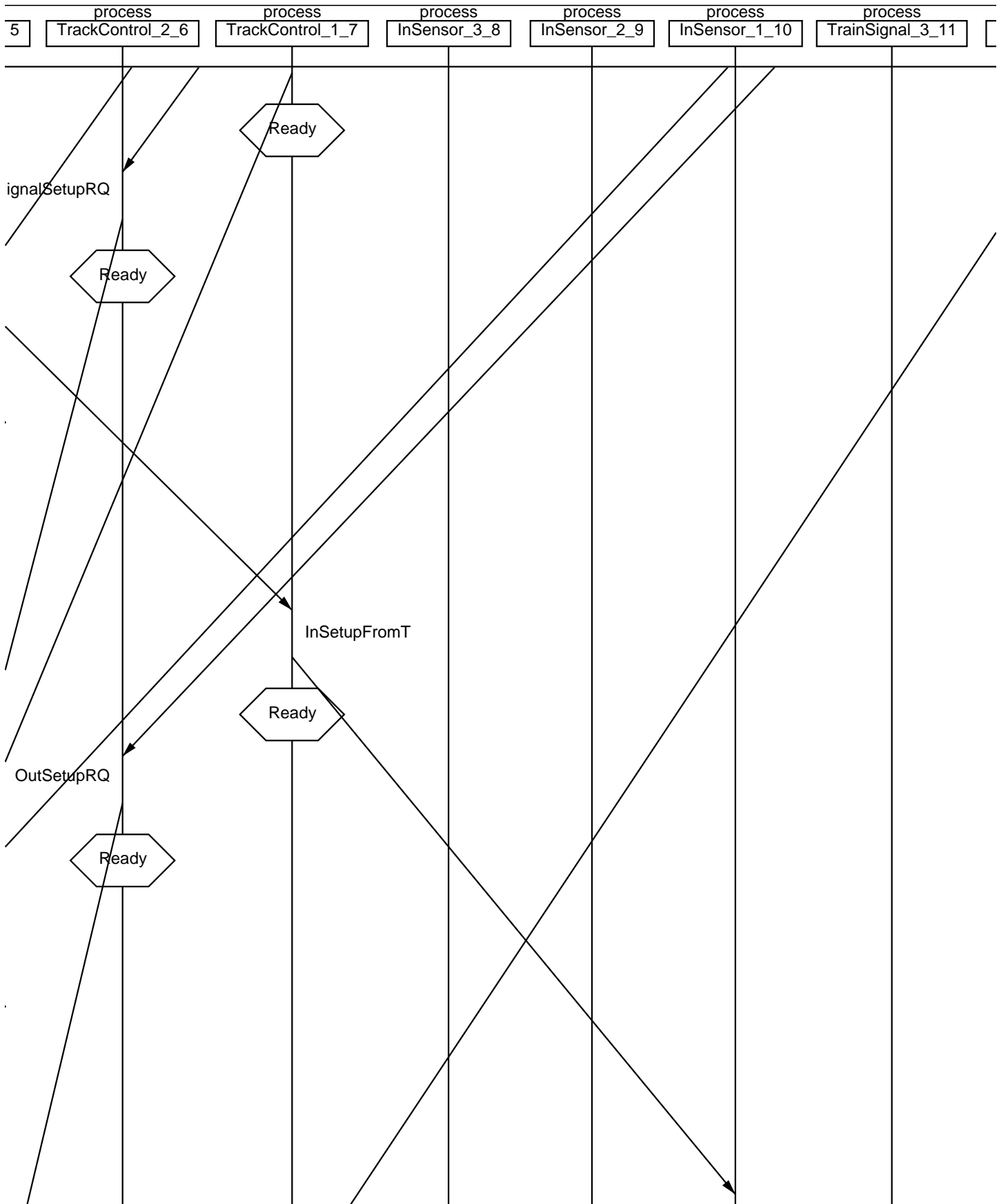


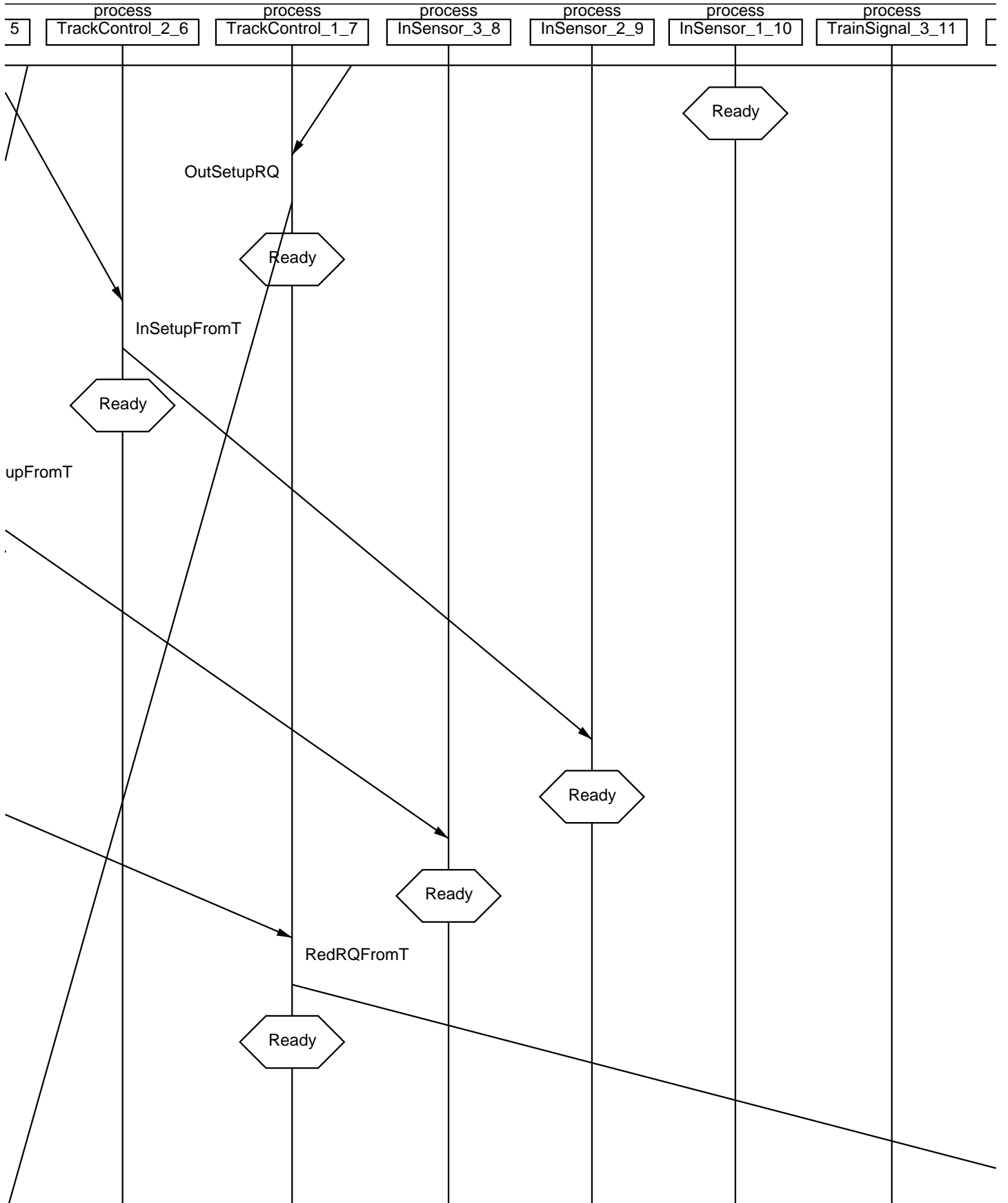


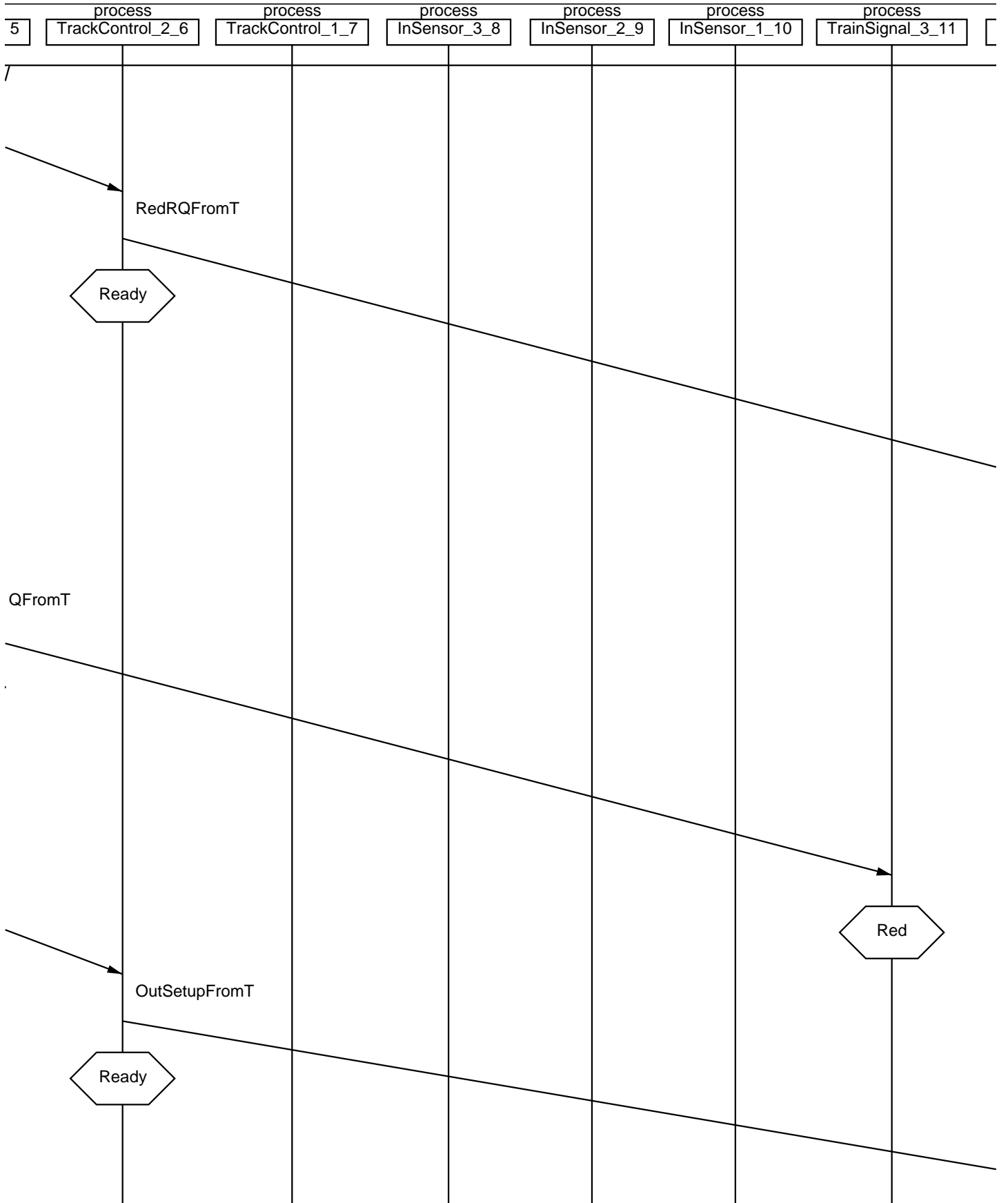


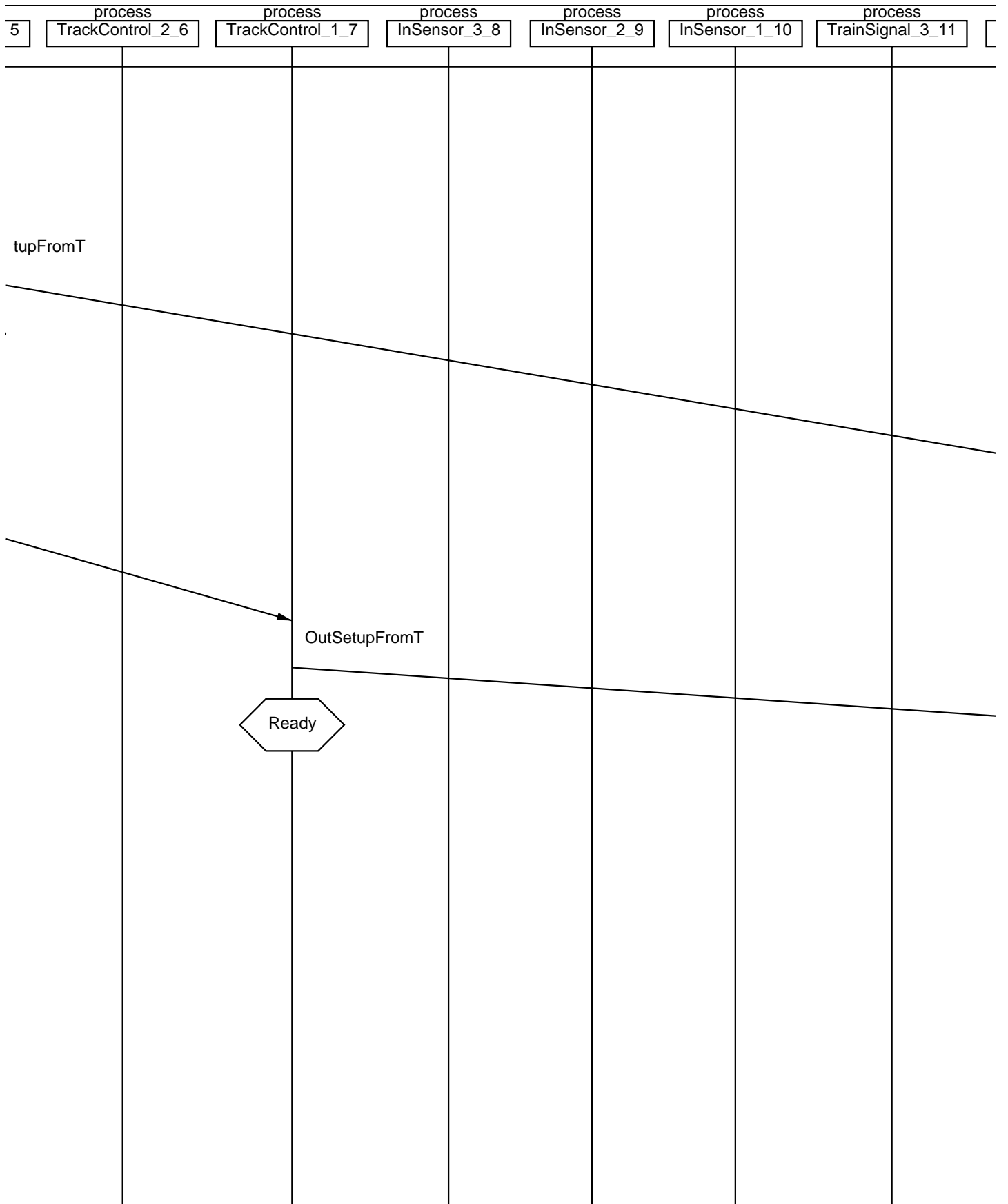


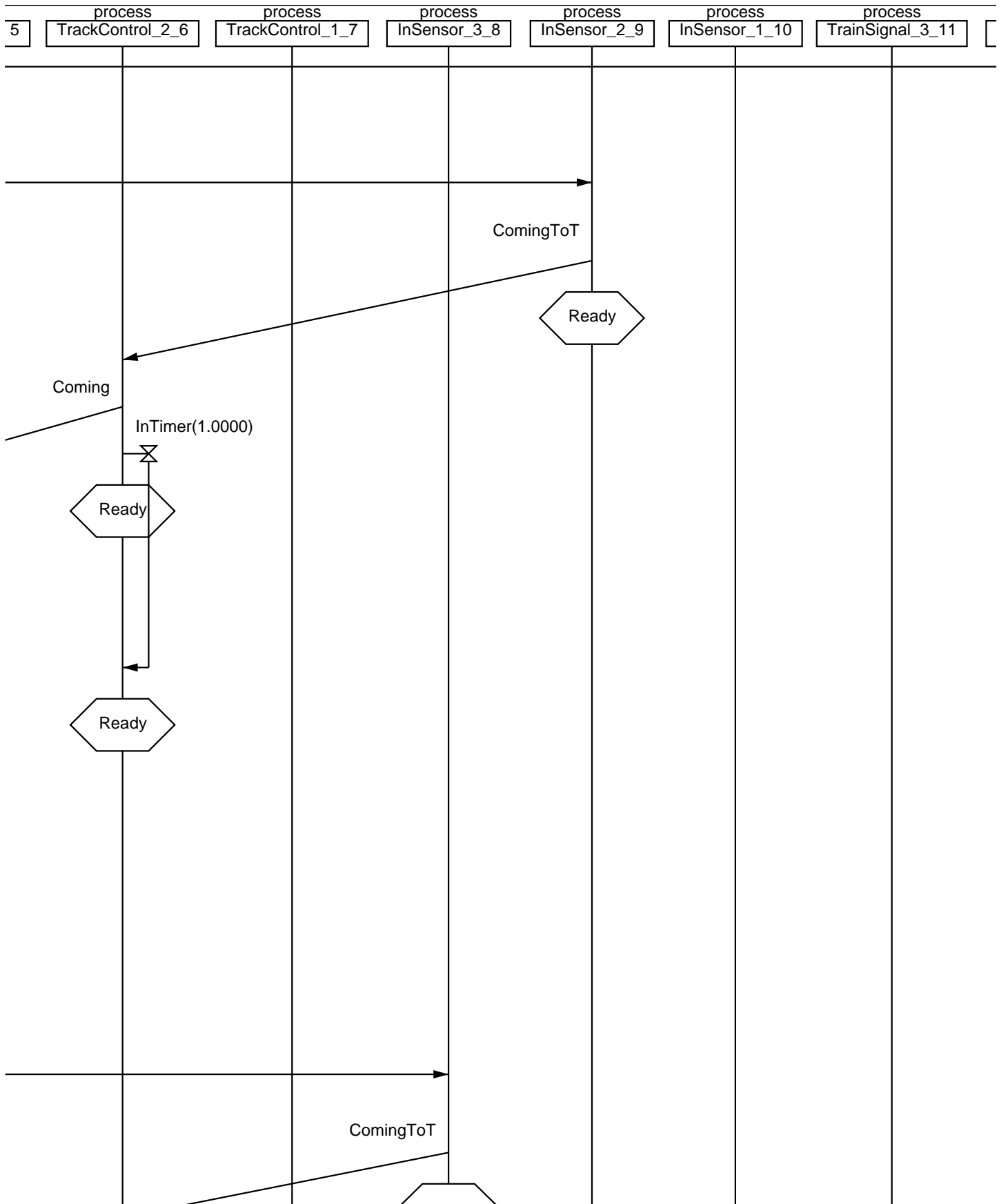


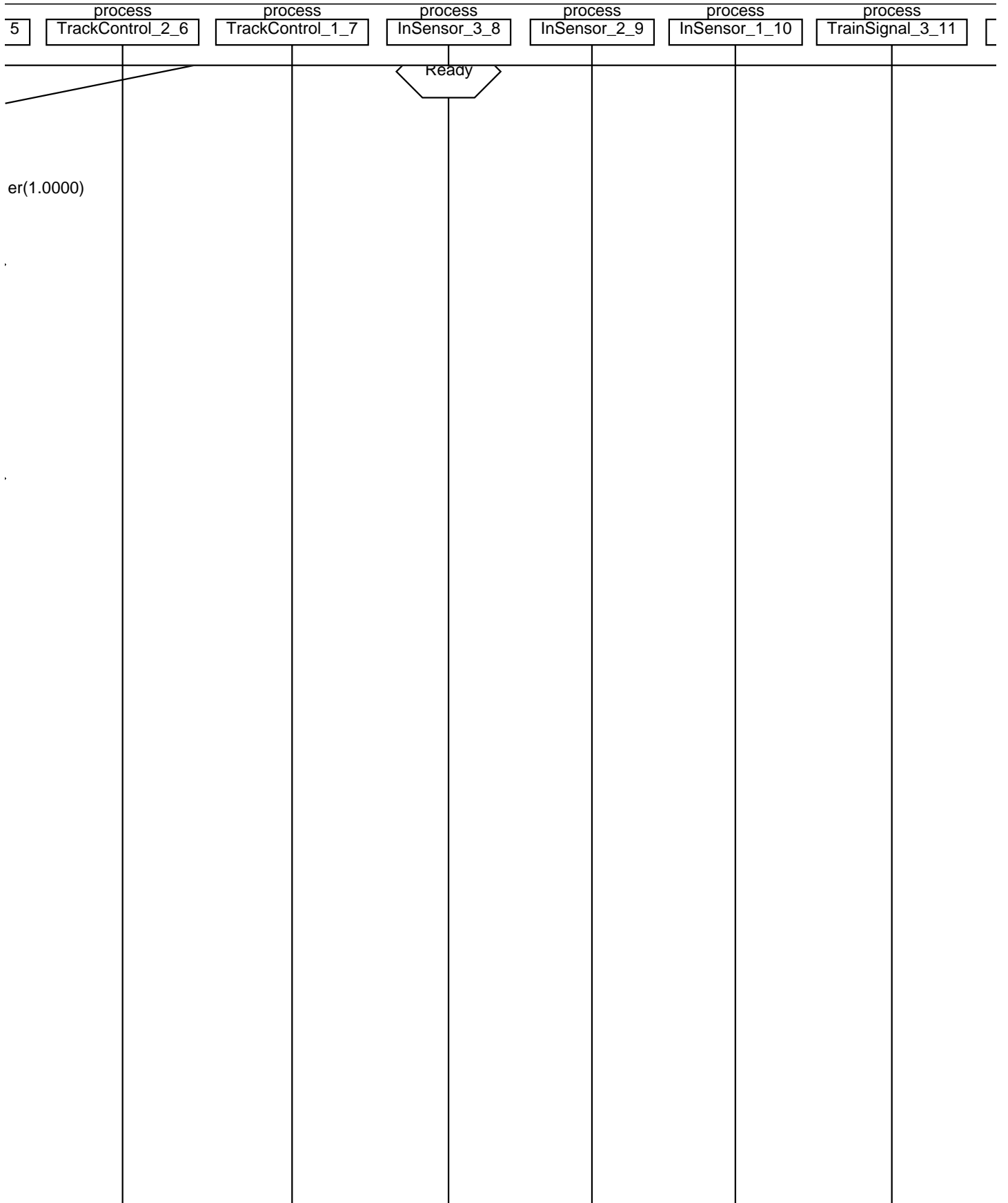


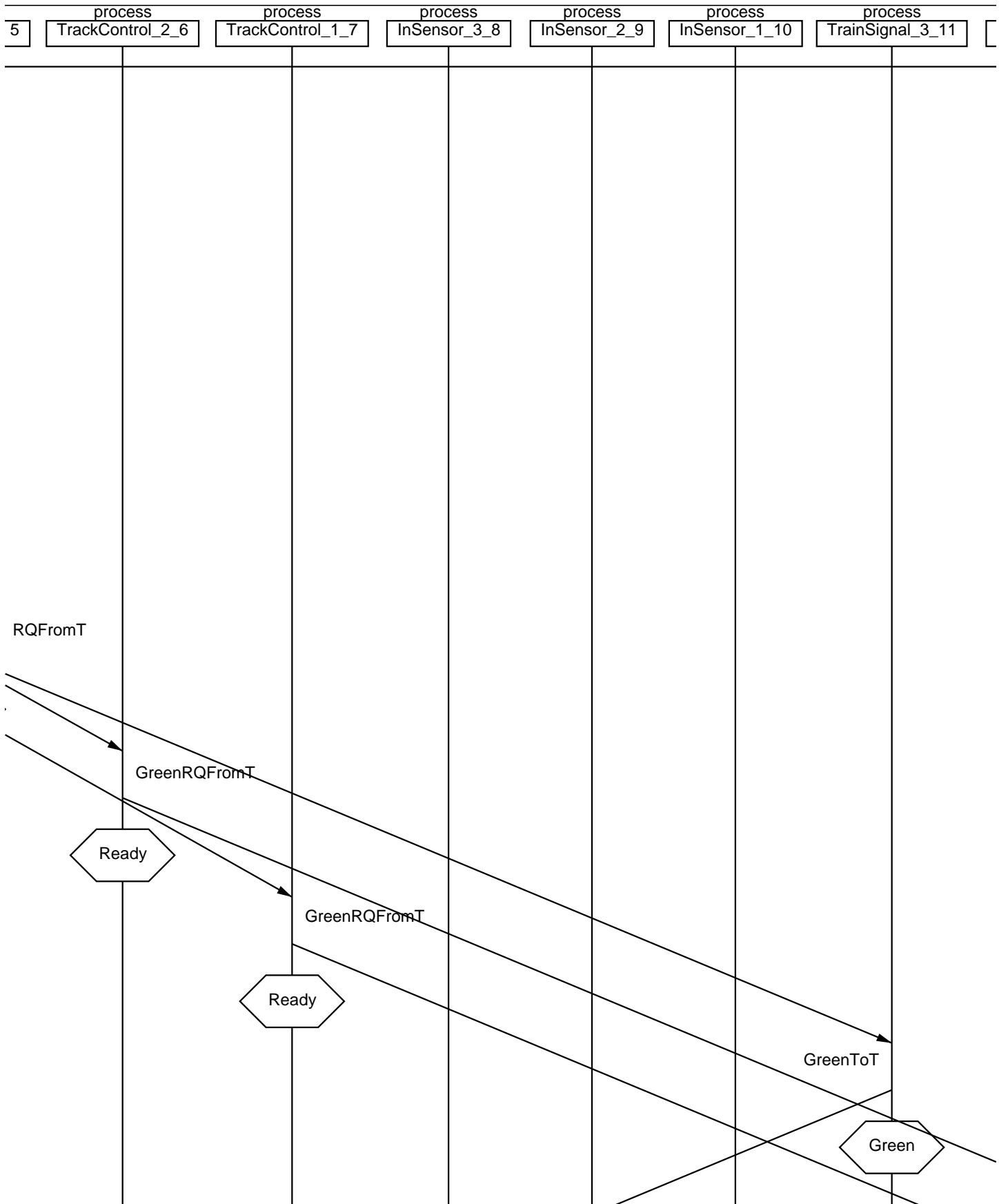


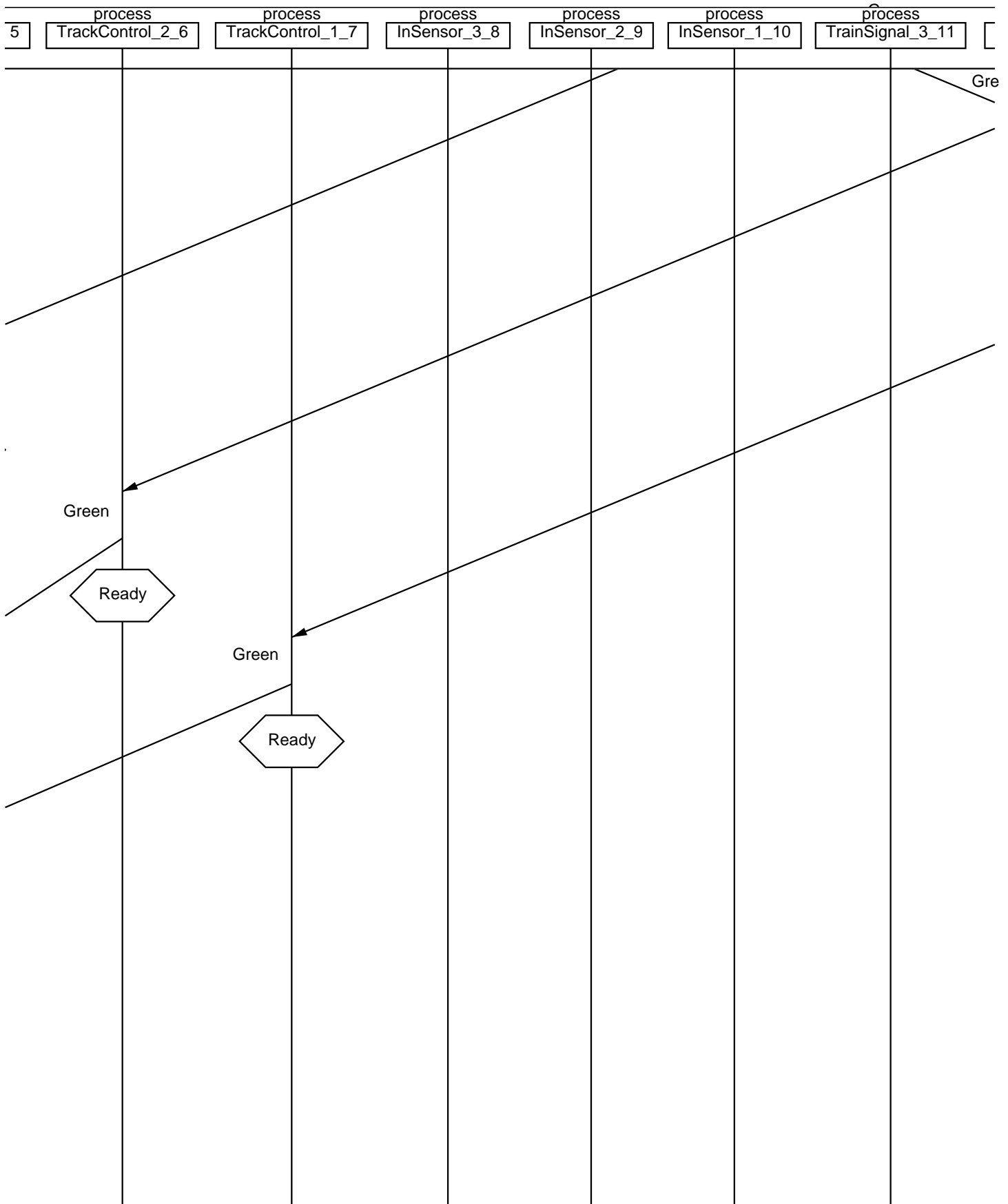


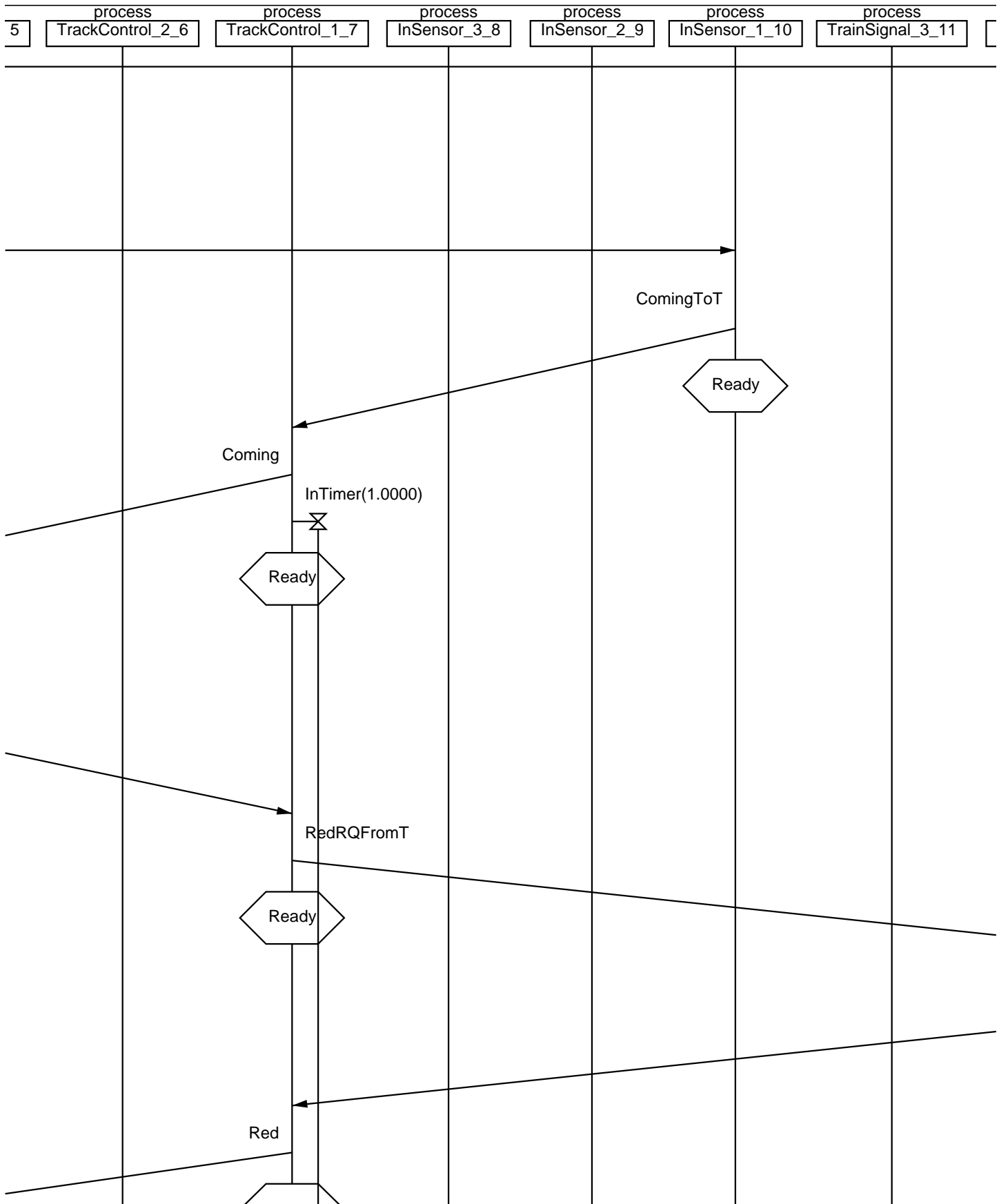


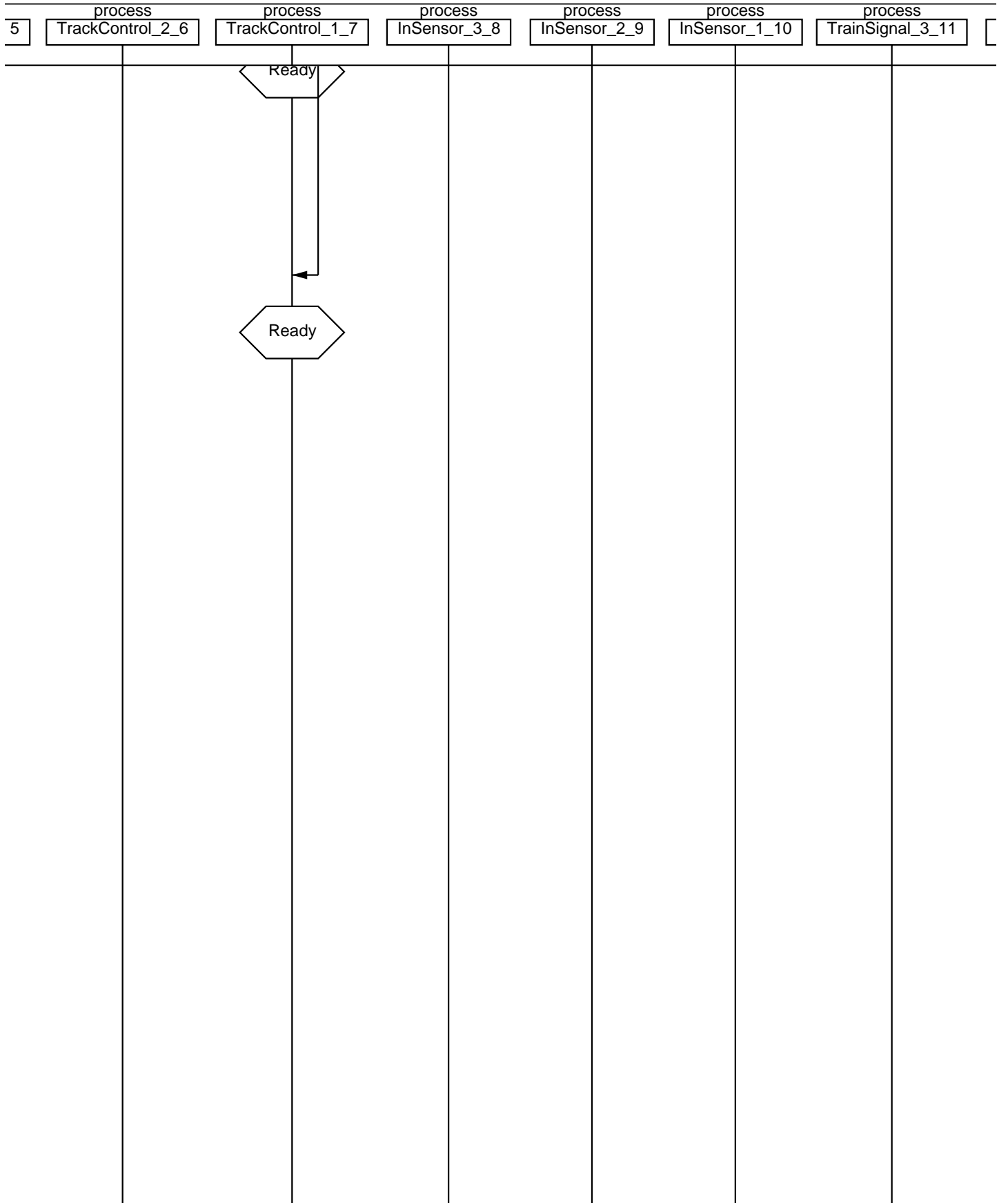


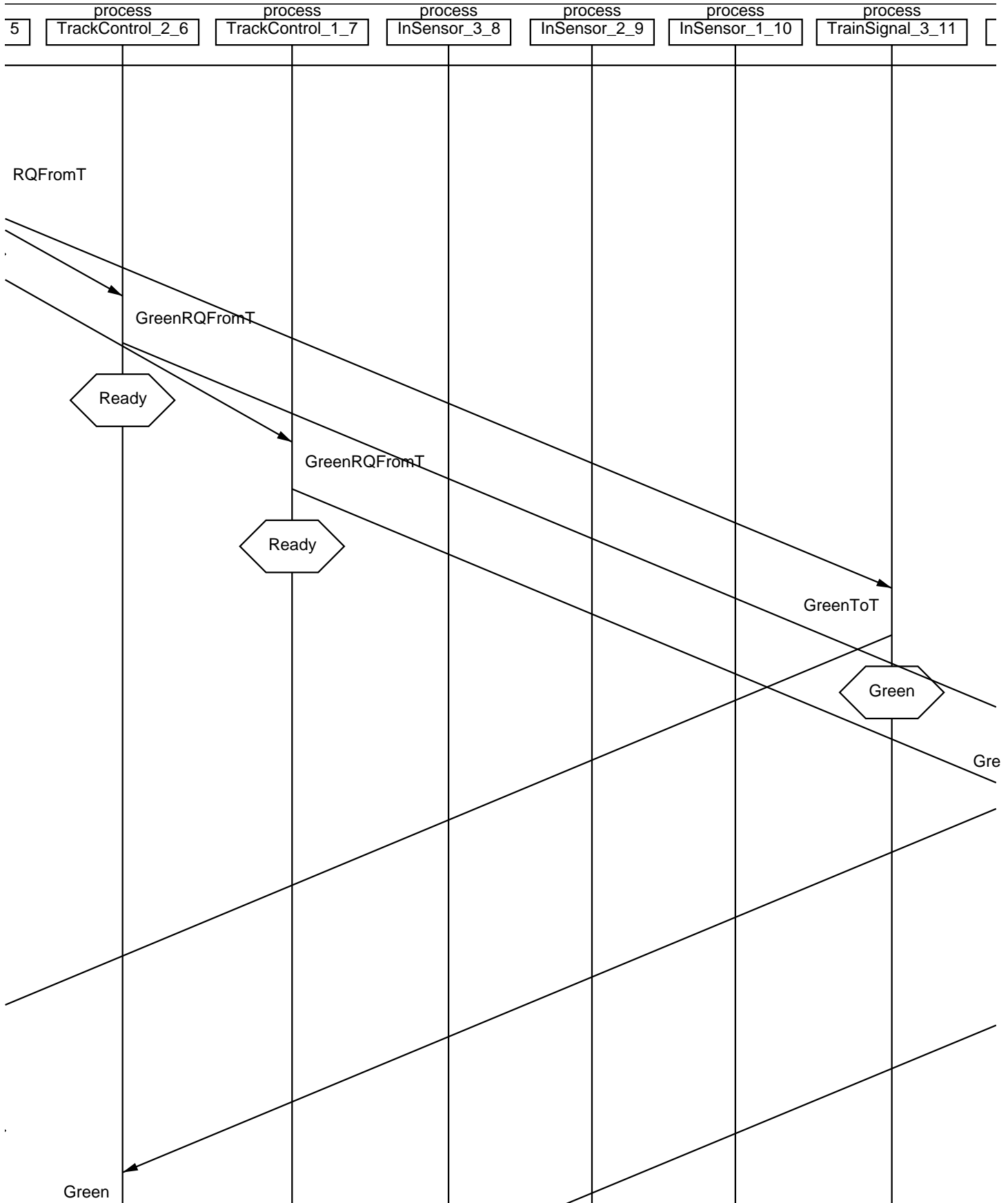


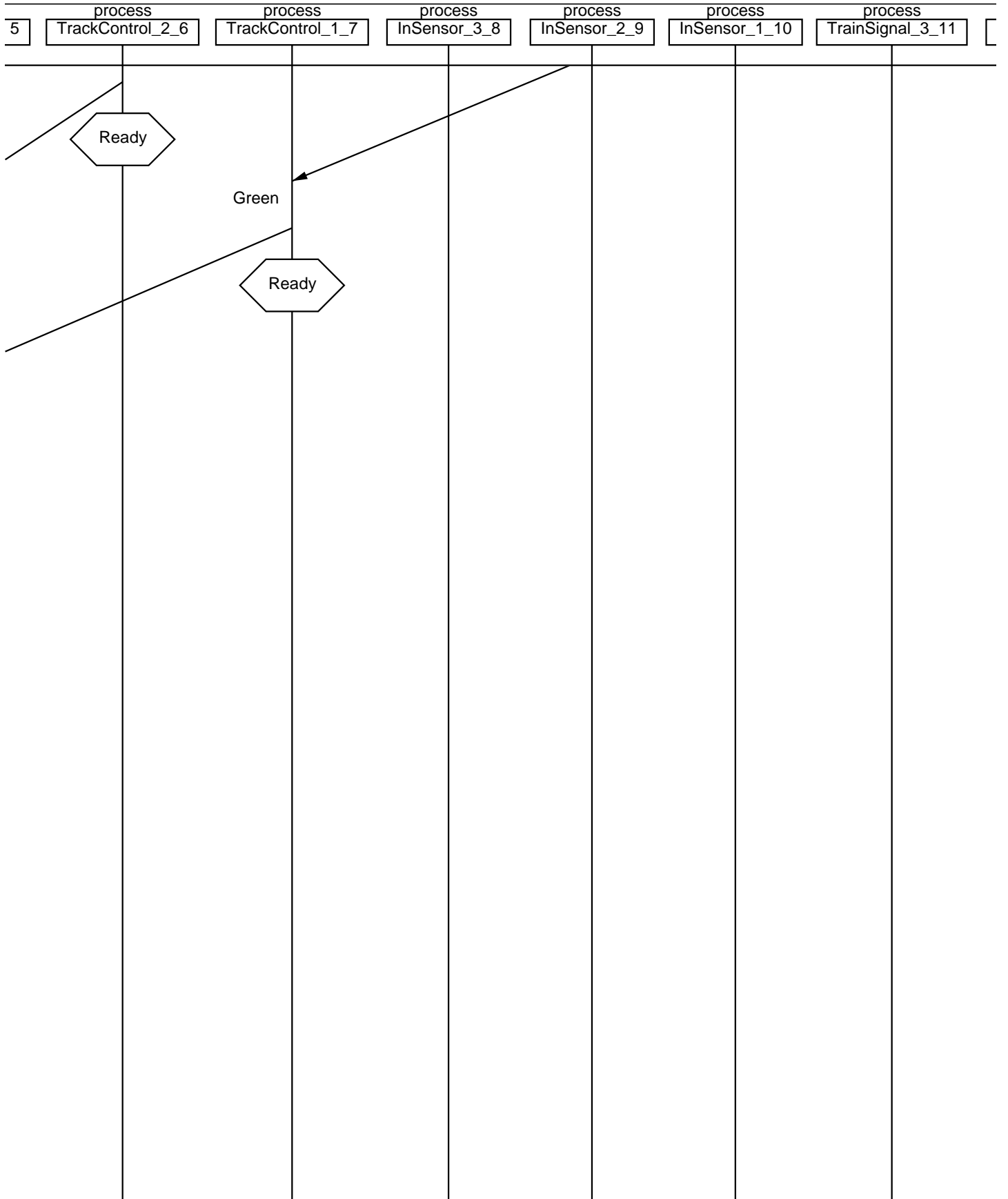


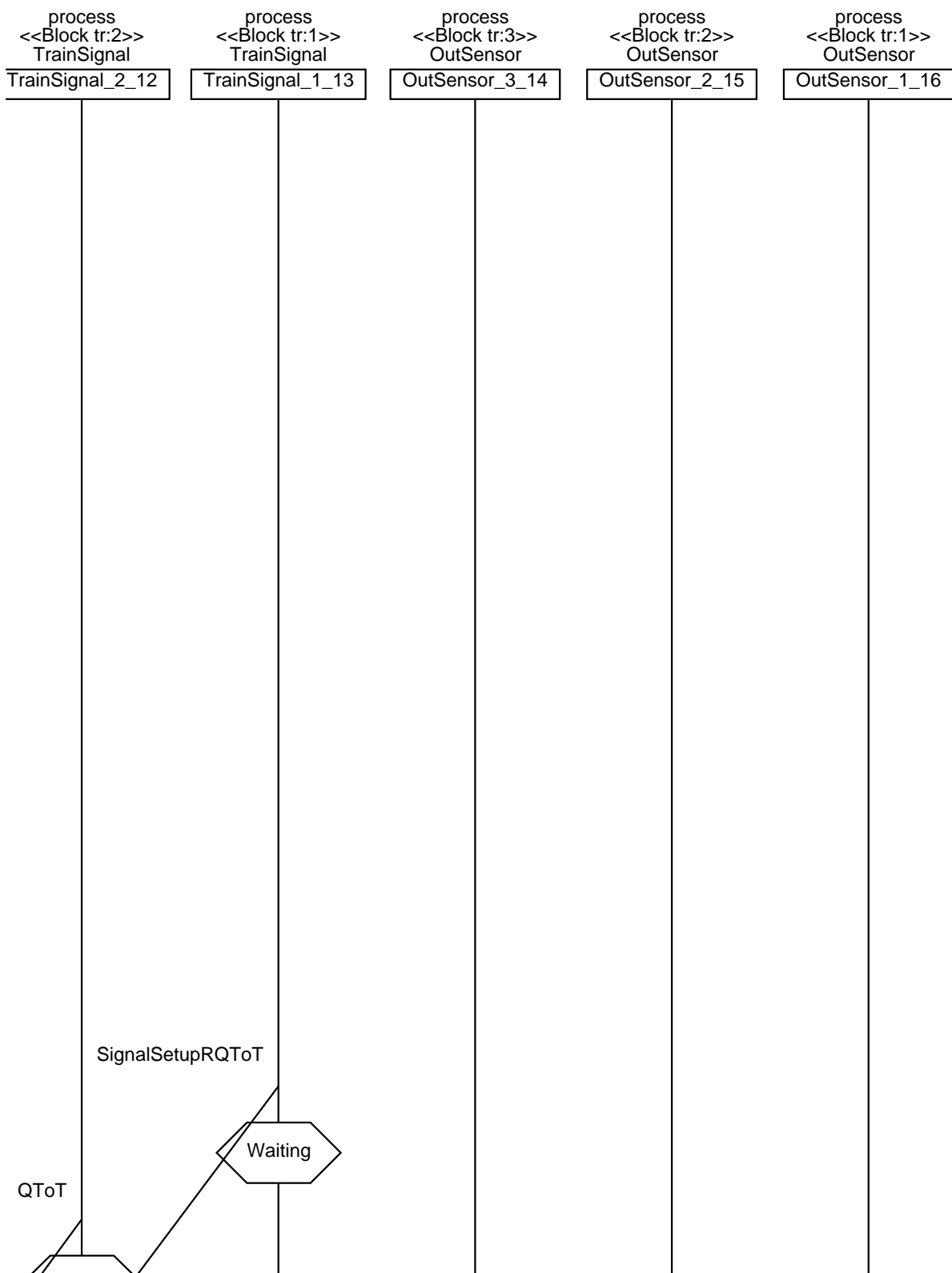


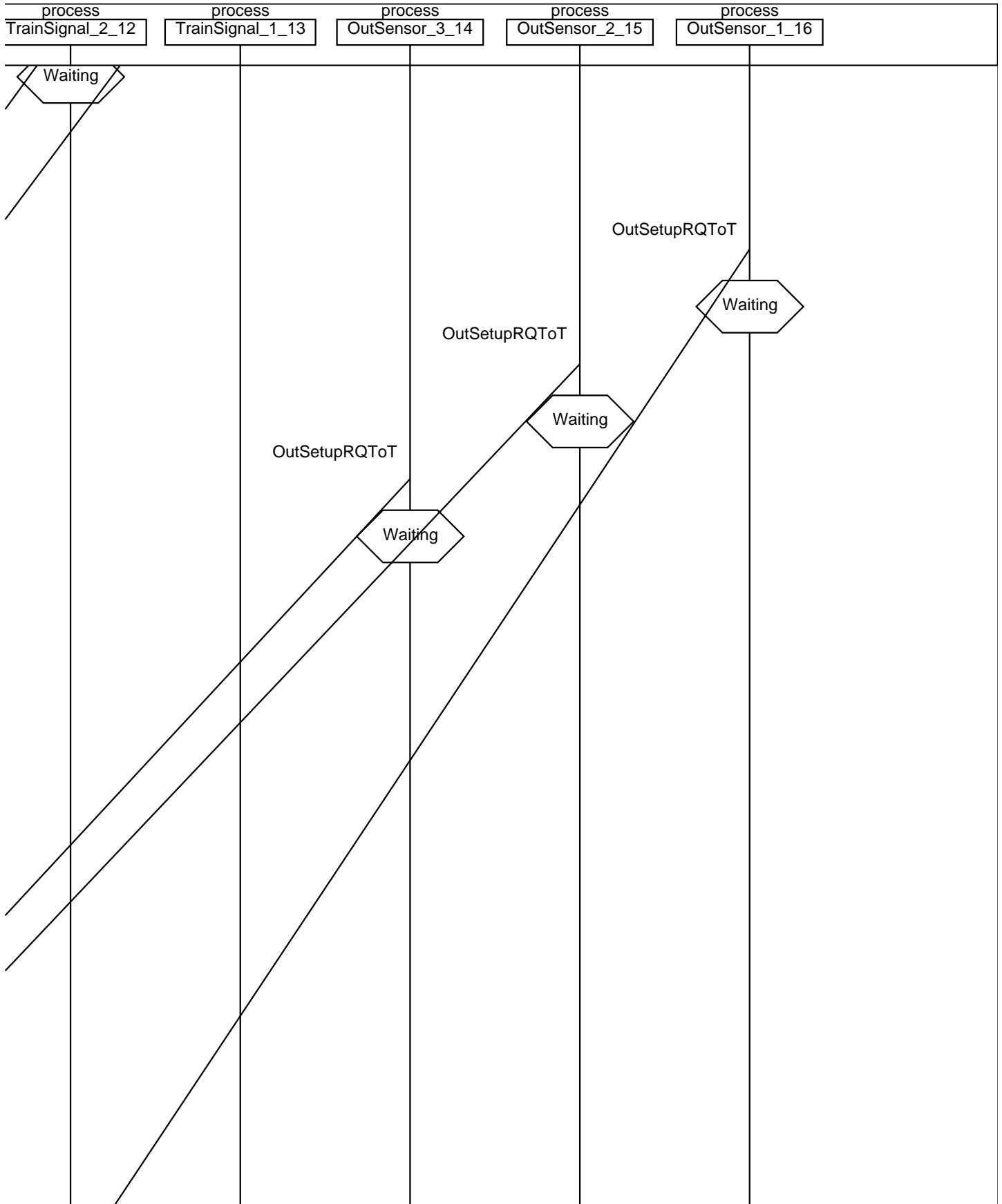




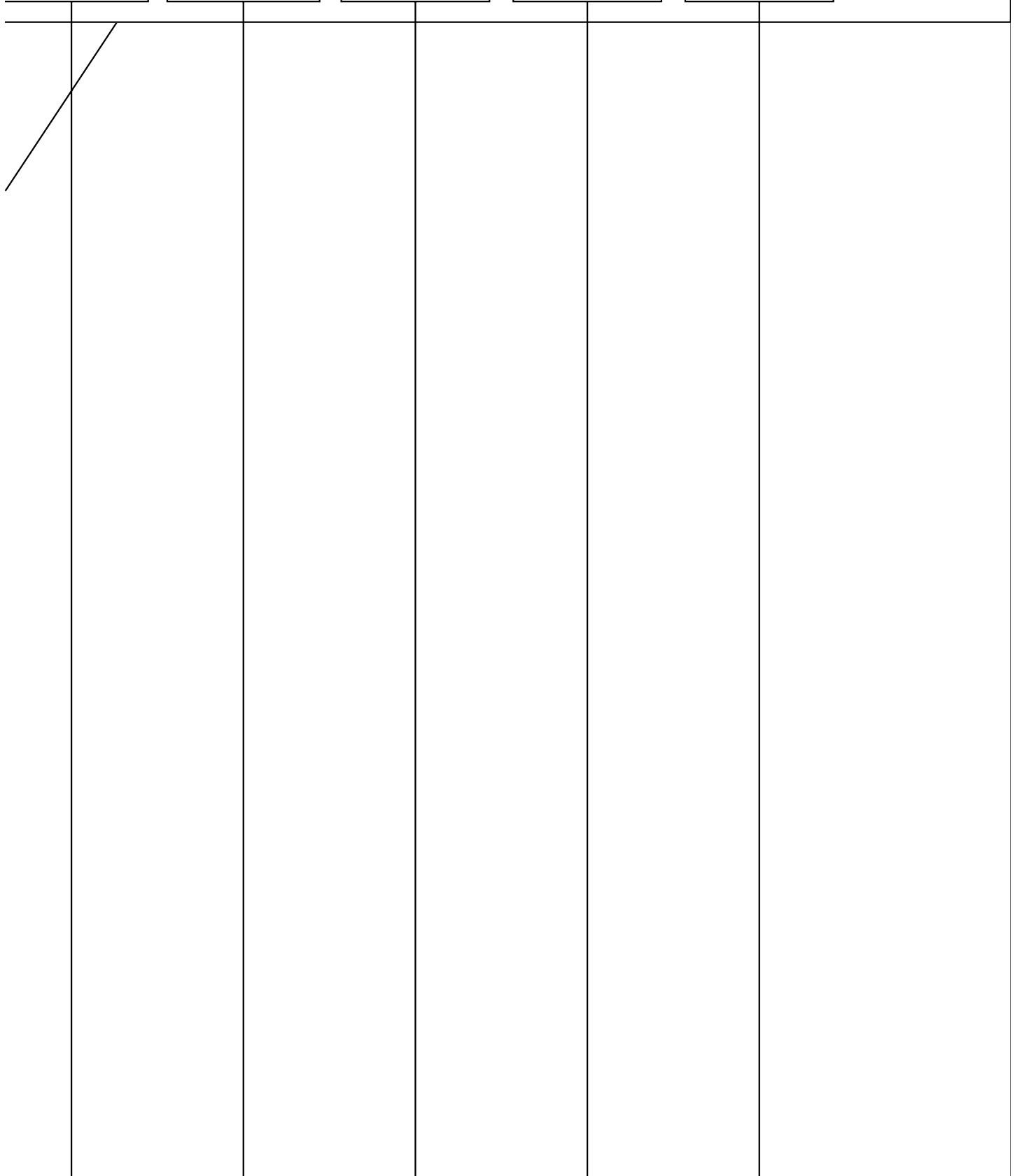




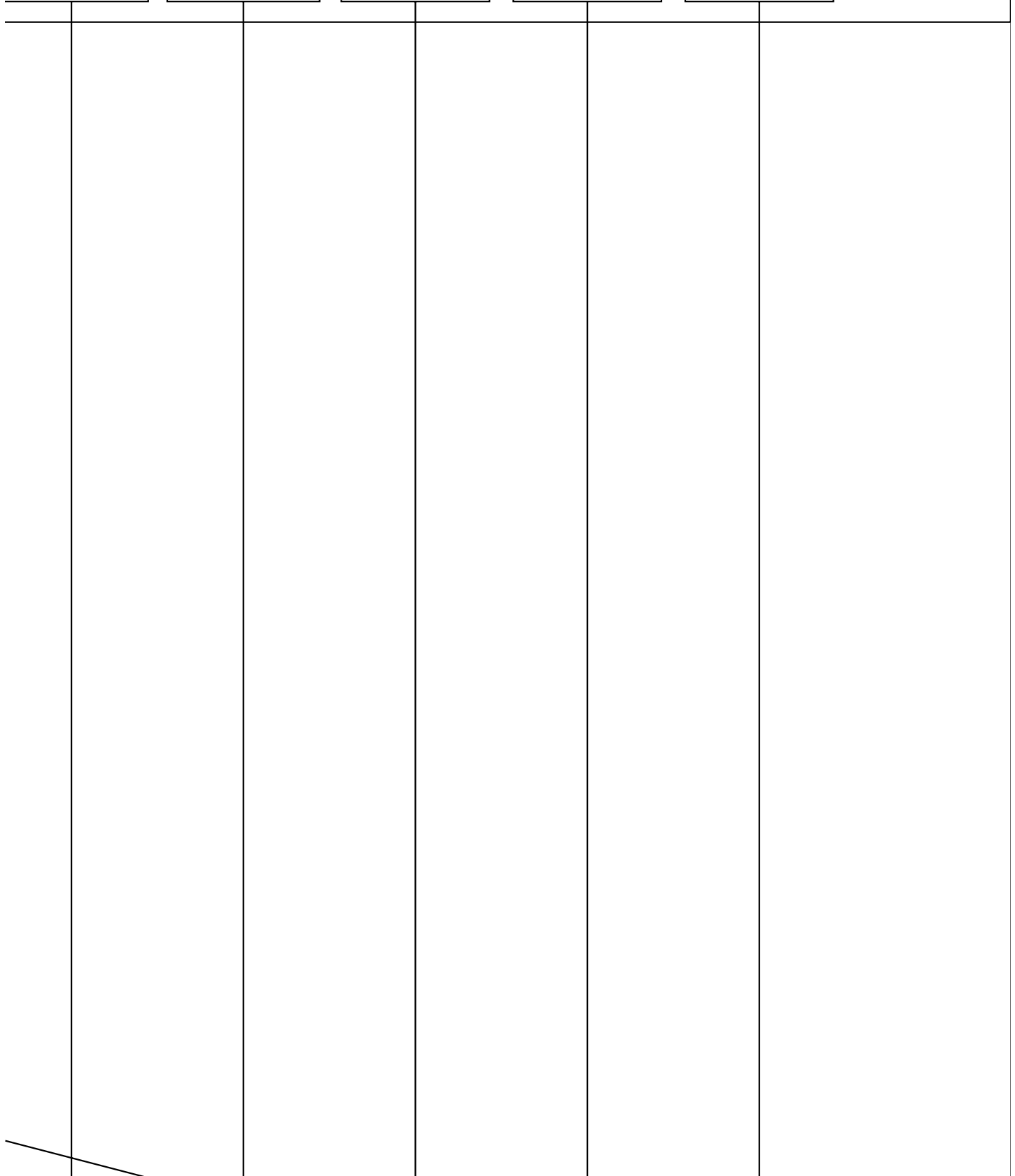


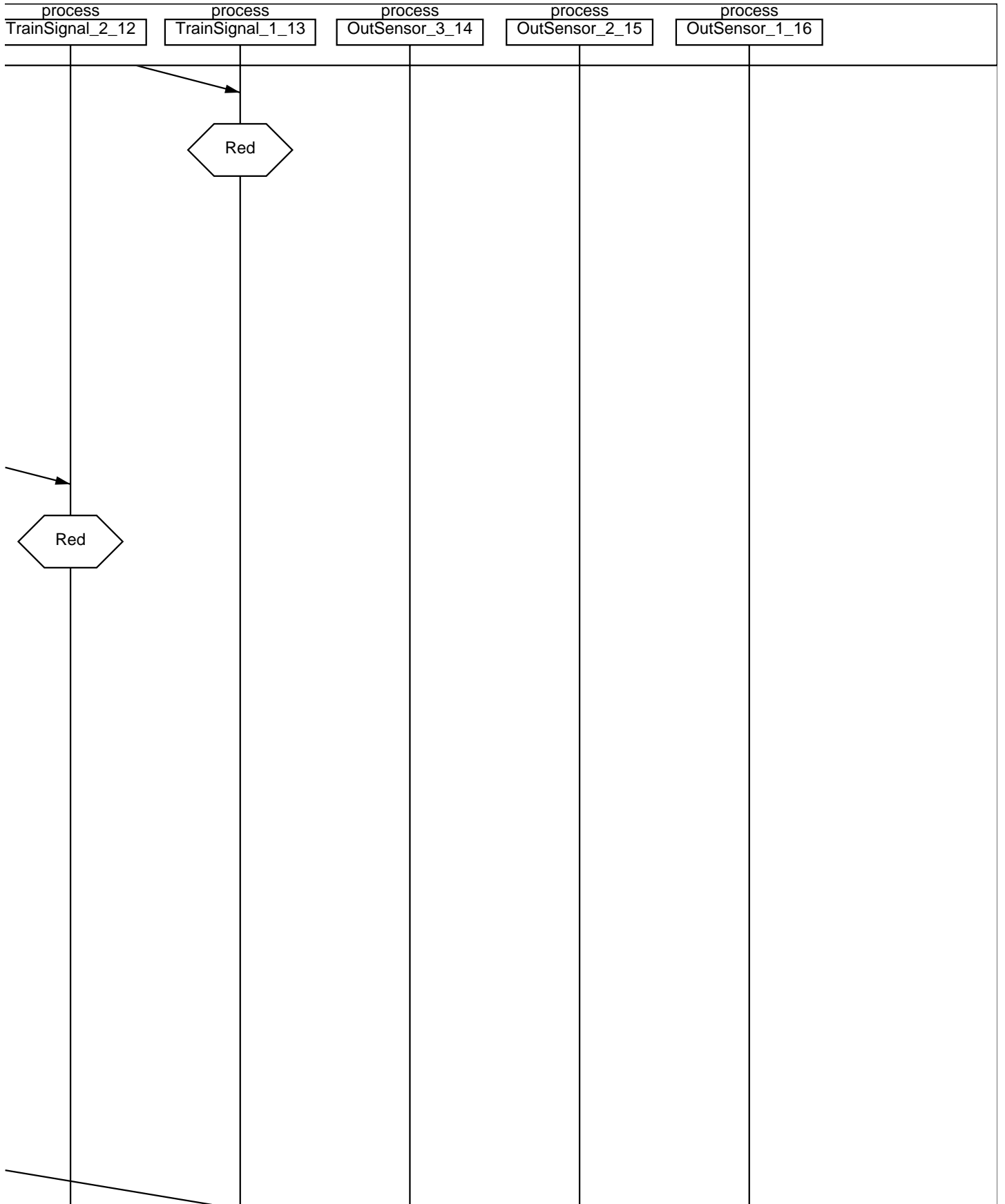


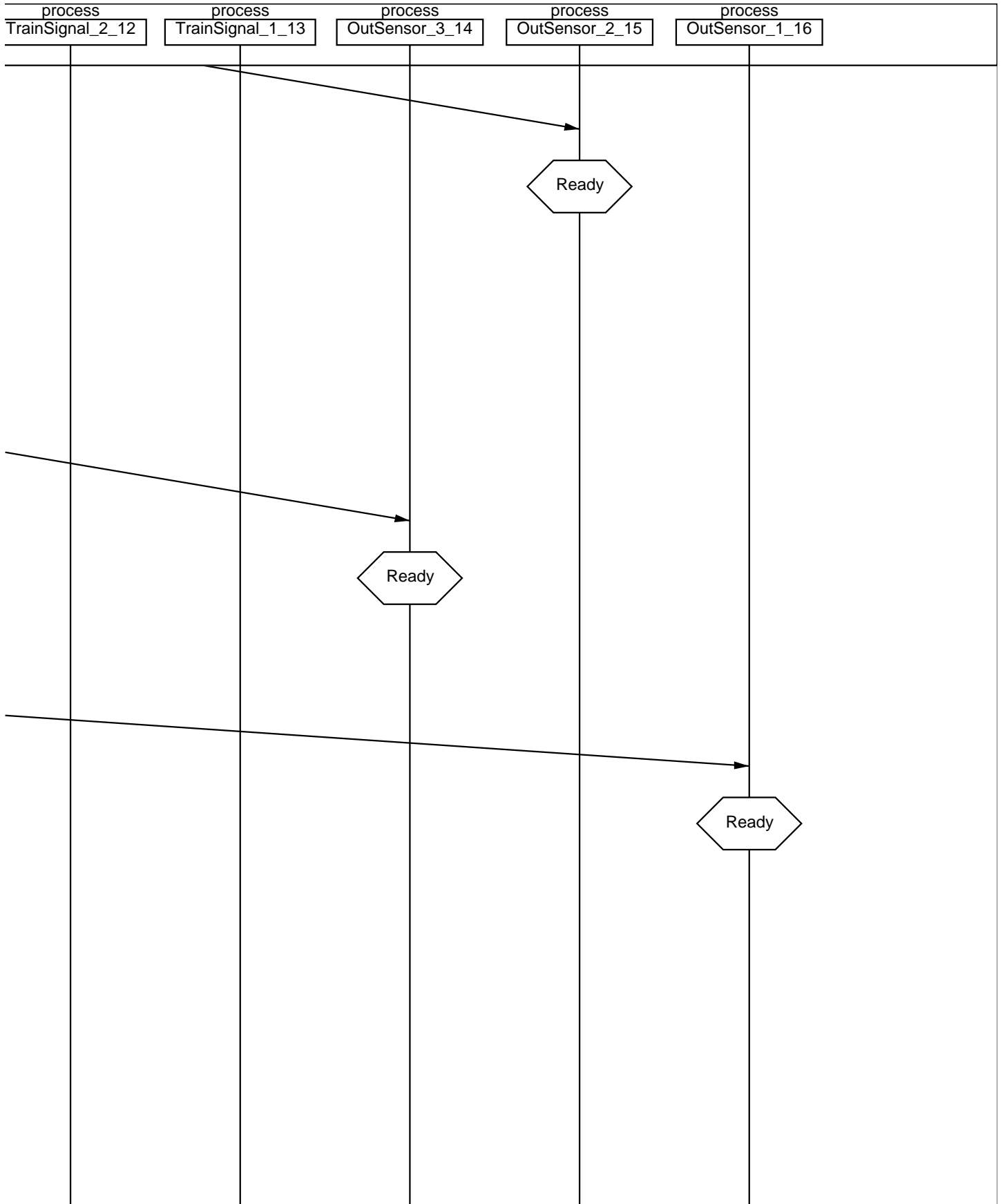
process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------



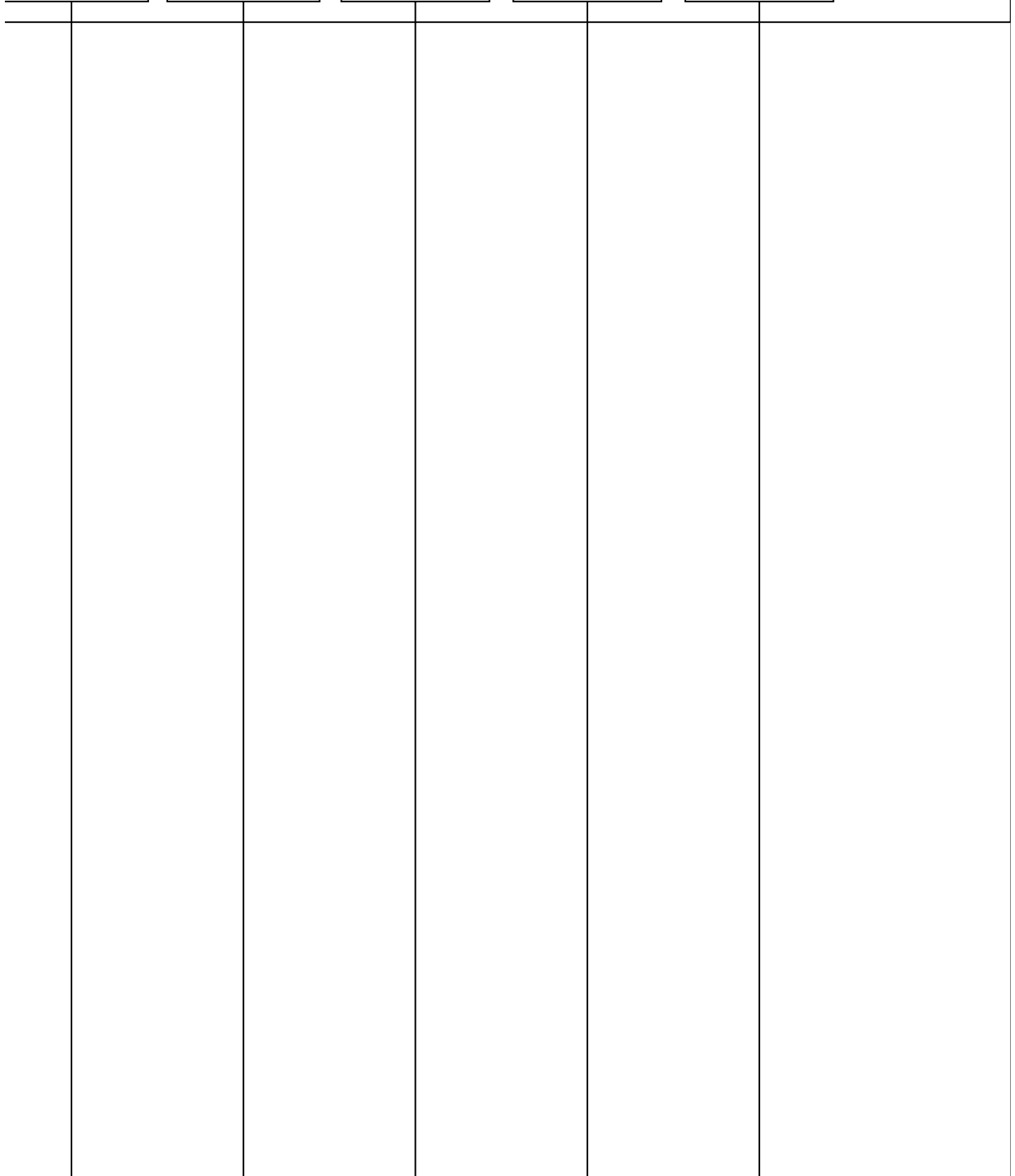
process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------



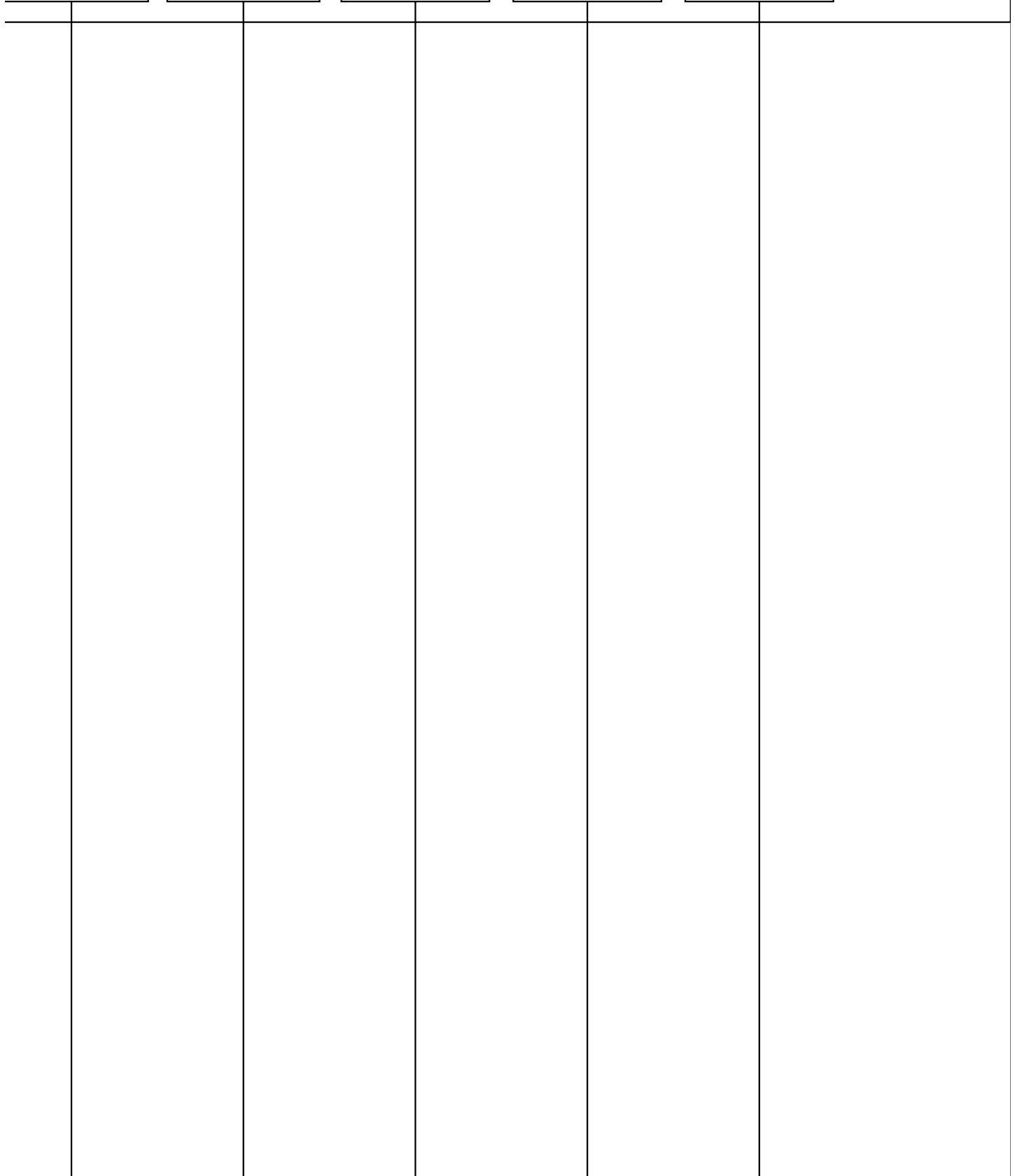




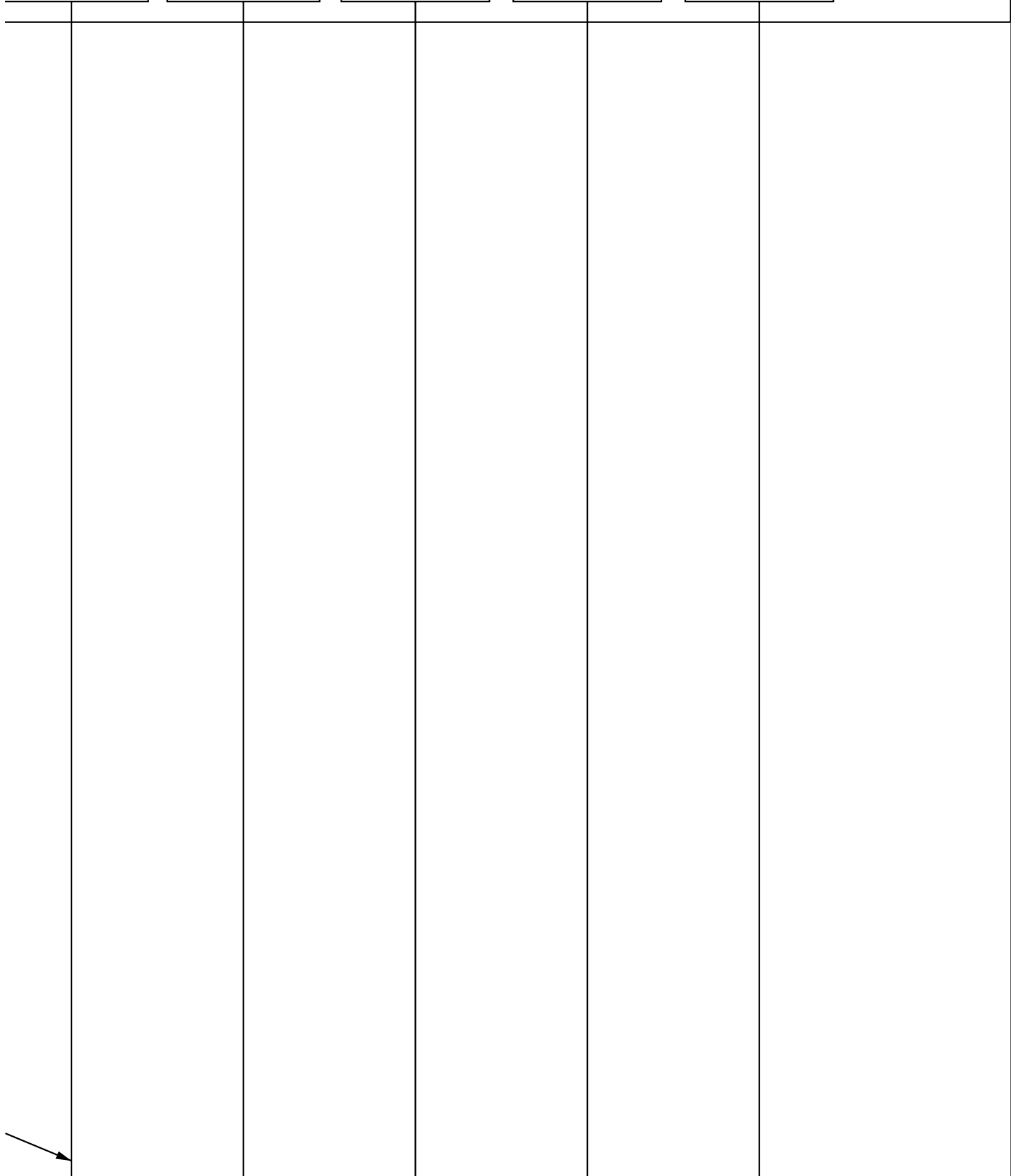
process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------

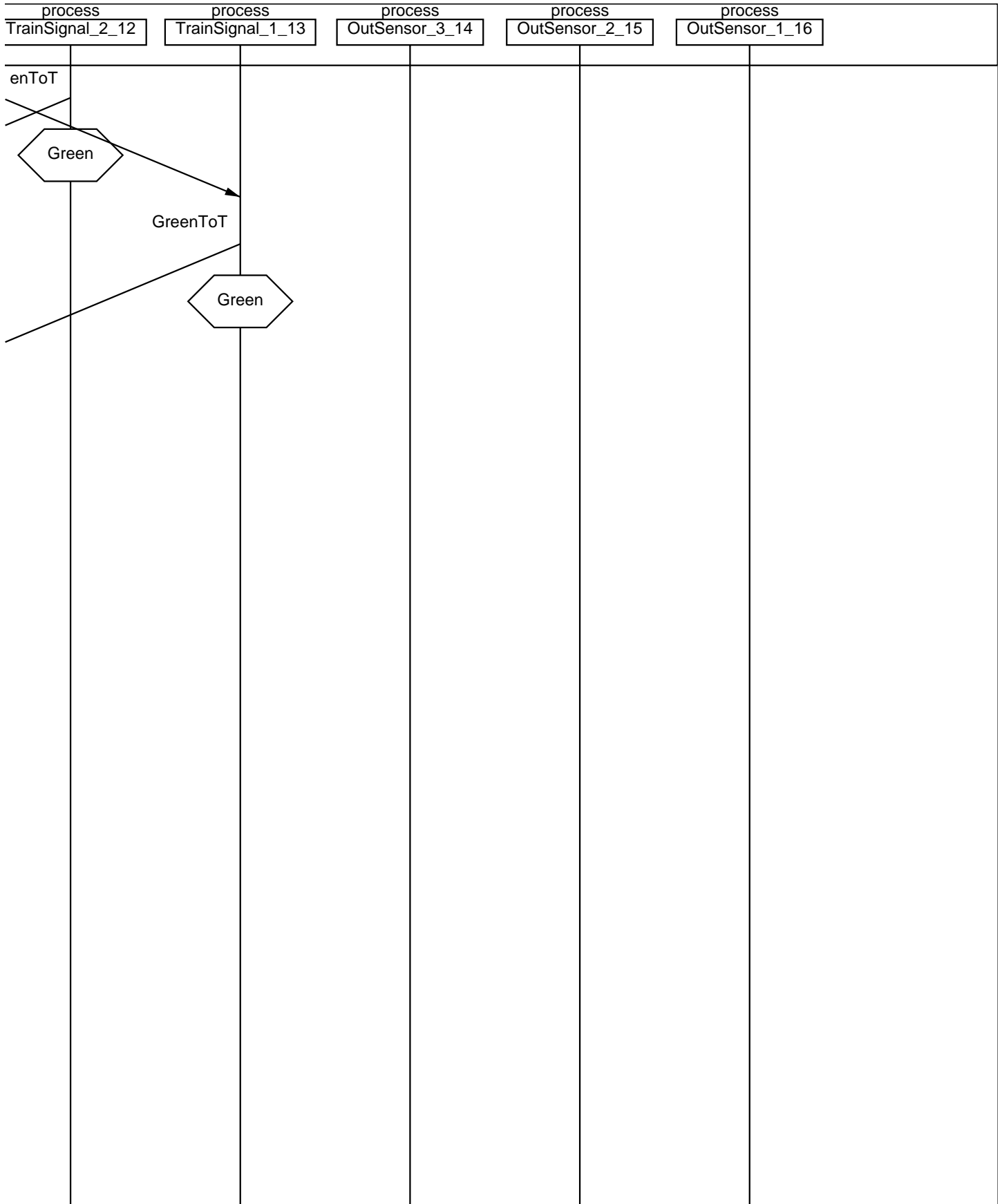


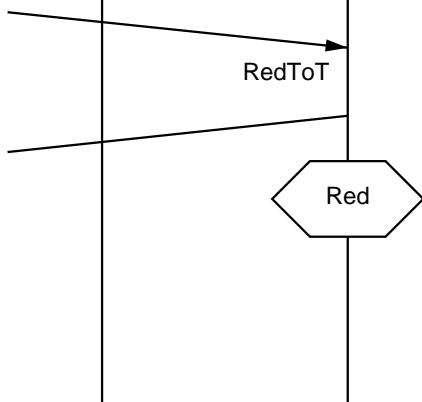
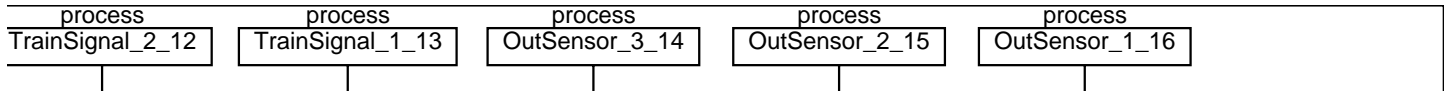
process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------



process TrainSignal_2_12	process TrainSignal_1_13	process OutSensor_3_14	process OutSensor_2_15	process OutSensor_1_16
-----------------------------	-----------------------------	---------------------------	---------------------------	---------------------------







process	process	process	process	process
---------	---------	---------	---------	---------

TrainSignal_2_12				
------------------	--	--	--	--

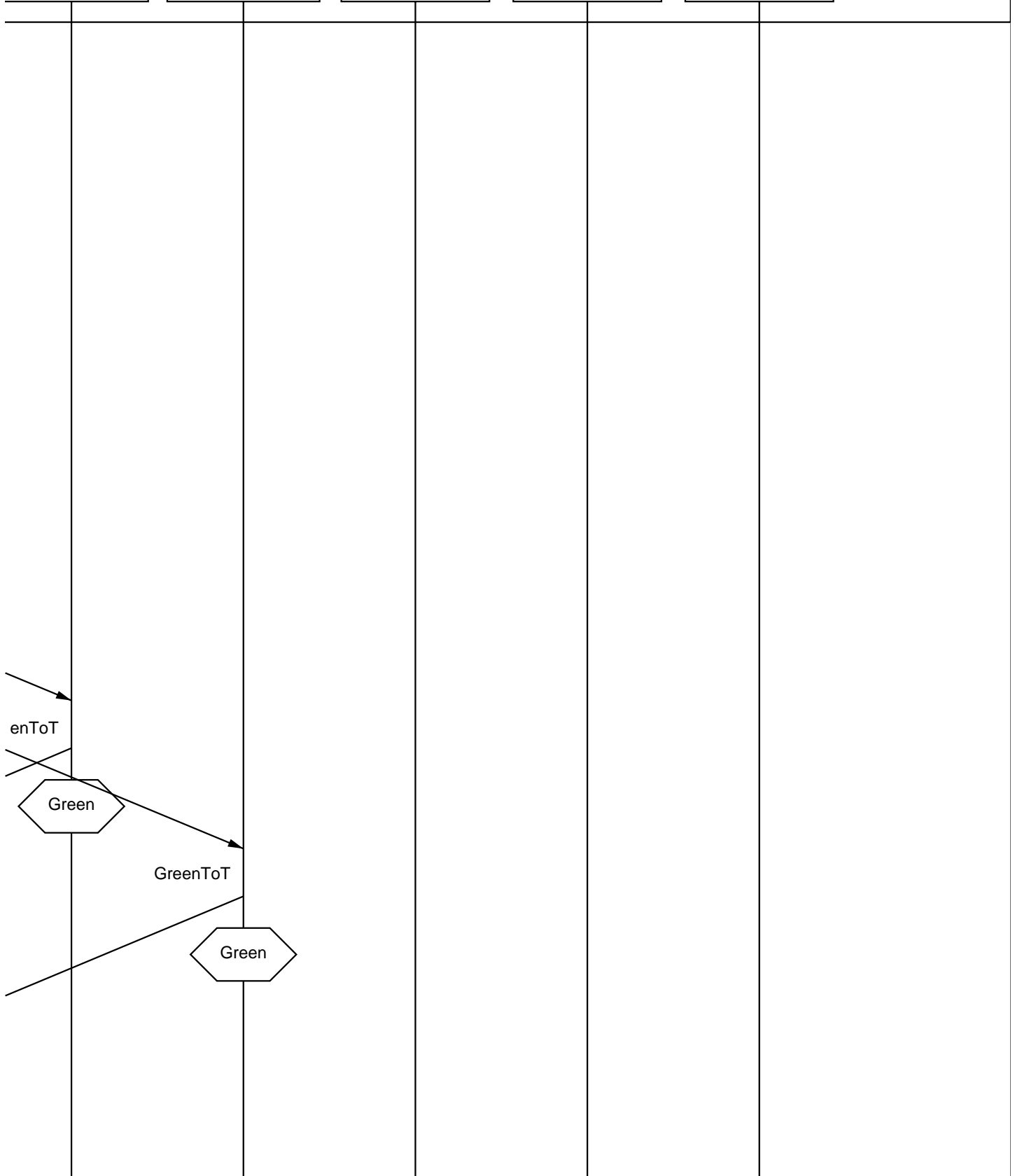
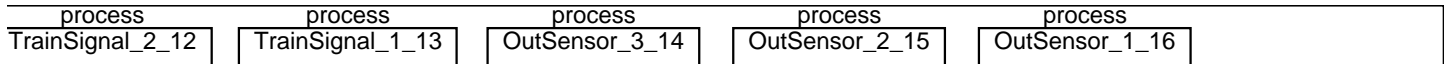
TrainSignal_1_13				
------------------	--	--	--	--

OutSensor_3_14				
----------------	--	--	--	--

OutSensor_2_15				
----------------	--	--	--	--

OutSensor_1_16				
----------------	--	--	--	--

--	--	--	--	--	--	--



process	process	process	process	process
---------	---------	---------	---------	---------

TrainSignal_2_12					
------------------	--	--	--	--	--

TrainSignal_1_13					
------------------	--	--	--	--	--

OutSensor_3_14					
----------------	--	--	--	--	--

OutSensor_2_15					
----------------	--	--	--	--	--

OutSensor_1_16					
----------------	--	--	--	--	--

--	--	--	--	--	--